GAL20V8/883

High Performance E²CMOS PLD Generic Array Logic™

Features

- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - **— 10 ns Maximum Propagation Delay**
  - **— Fmax = 62.5 MHz**
  - **— 7 ns Maximum from Clock Input to Data Output**
  - **— TTL Compatible 12 mA Outputs**
  - **— UltraMOS® Advanced CMOS Technology**
- **50% REDUCTION IN POWER FROM BIPOLAR**
  - **— 75mA Typ Icc on Low Power Device**
- **E² CELL TECHNOLOGY**
  - **— Reconfigurable Logic**
  - **— Reprogrammable Cells**
  - **— 100% Tested/100% Yields**
  - **— High Speed Electrical Erasure (<100ms)**
  - **— 20 Year Data Retention**
- **EIGHT OUTPUT LOGIC MACROCELLS**
  - **— Maximum Flexibility for Complex Logic Designs**
  - **— Programmable Output Polarity**
  - **— Also Emulates 24-pin PAL® Devices with Full Function/ Fuse Map/Parametric Compatibility**
- **PRELOAD AND POWER-ON RESET OF ALL REGISTERS**
  - **— 100% Functional Testability**
- **APPLICATIONS INCLUDE:**
  - **— DMA Control**
  - **— State Machine Control**
  - **— High Speed Graphics Processing**
  - **— Standard Logic Speed Upgrade**
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

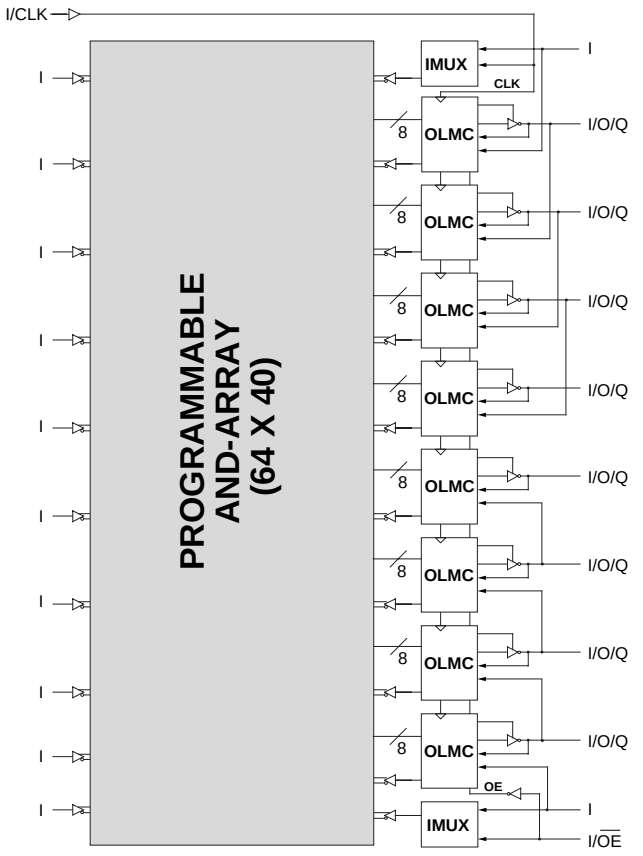
Description

The GAL20V8/883 is a high performance E²CMOS programmable logic devices processed in full compliance to MIL-STD-883. This military grade device combines a high performance CMOS process with Electrically Erasable (E²) floating gate technology to provide the highest speed/power performance available in the 883 qualified PLD market.

The generic GAL architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. The GAL20V8/883 is capable of emulating all standard 24-pin PAL® devices with full function/fuse map/parametric compatibility.

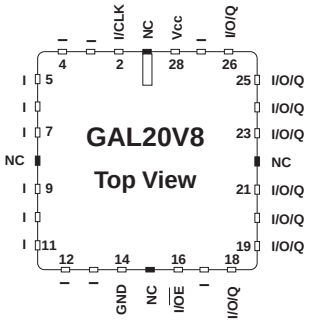
Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. Therefore, Lattice Semiconductor delivers 100% field programmability and functionality of all GAL products. In addition, 100 erase/write cycles and data retention in excess of 20 years are specified.

Functional Block Diagram

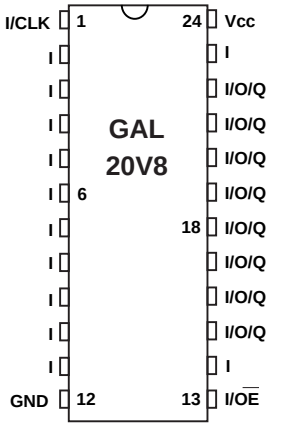


Pin Configuration

LCC



CERDIP



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Absolute Maximum Ratings(1)

Supply voltage V_{CC} ..... –0.5 to +7V
Input voltage applied ..... –2.5 to V_{CC} +1.0V
Off-state output voltage applied ..... –2.5 to V_{CC} +1.0V
Storage Temperature ..... –65 to 150°C
Case Temperature with
Power Applied ..... –55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

Recommended Operating Conditions

CaseTemperature (T_C) ..... –55 to 125°C
Supply voltage (V_{CC})
with Respect to Ground ..... +4.50 to +5.50V

DC Electrical Characteristics

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION		MIN.	TYP.[3]	MAX.	UNITS
V_{IL}	Input Low Voltage			Vss – 0.5	—	0.8	V
V_{IH}	Input High Voltage			2.0	—	Vcc+1	V
I_{IL}	Input or I/O Low Leakage Current for -10 Speed Grade[1]	$0V \le V_{IN} \le V_{IL}$ (MAX.)		—	—	-100	µA
	Input or I/O Low Leakage Current for -15 and -20 Speed Grades	$0V \le V_{IN} \le V_{IL}$ (MAX.)		—	—	-10	µA
I_{IH}	Input or I/O High Leakage Current	$3.5V_{IH} \le V_{IN} \le V_{CC}$		—	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = MAX. Vin = V_{IL} or V_{IH}		—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = MAX. Vin = V_{IL} or V_{IH}		2.4	—	—	V
I_{OL}	Low Level Output Current			—	—	12	mA
I_{OH}	High Level Output Current			—	—	–2.0	mA
I_{OS}[2]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T_A = 25°C		–30	—	–150	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz Outputs Open	L -10/-15/-20	—	75	130	mA

1) The leakage current is due to the internal pull-up on all pins. See Input Buffer section for more information.
2) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems caused by tester ground degradation. Characterized but not 100% tested.
3) Typical values are at Vcc = 5V and TA = 25 °C

AC Switching Characteristics

Over Recommended Operating Conditions

PARAMETER	TEST COND[1].	DESCRIPTION	-10		-15		-20		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
tpd	A	Input or I/O to Combinational Output	2	10	2	15	2	20	ns
tco	A	Clock to Output Delay	1	7	1	12	1	15	ns
tcf[2]	—	Clock to Feedback Delay	—	7	—	12	—	15	ns
tsu	—	Setup Time, Input or Feedback before Clock↑	10	—	12	—	15	—	ns
th	—	Hold Time, Input or Feedback after Clock↑	0	—	0	—	0	—	ns
fmax[3]	A	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)	58.8	—	41.6	—	33.3	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)	58.8	—	41.6	—	33.3	—	MHz
	A	Maximum Clock Frequency with No Feedback	62.5	—	50	—	41.6	—	MHz
twh	—	Clock Pulse Duration, High	8	—	10	—	12	—	ns
twl	—	Clock Pulse Duration, Low	8	—	10	—	12	—	ns
ten	B	Input or I/O to Output Enabled	—	10	—	15	—	20	ns
	B	$\overline{OE}$ to Output Enabled	—	10	—	15	—	18	ns
tdis	C	Input or I/O to Output Disabled	—	10	—	15	—	20	ns
	C	$\overline{OE}$ to Output Disabled	—	10	—	15	—	18	ns

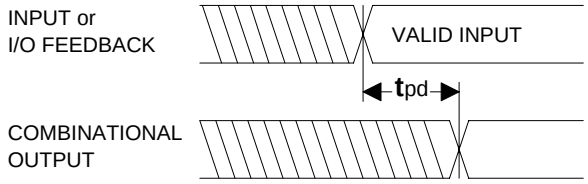
1) Refer to **Switching Test Conditions** section.
2) Calculated from **f**max with internal feedback. Refer to **fmax Descriptions** section.
3) Refer to **fmax Descriptions** section.

Capacitance (TA = 25°C, f = 1.0 MHz)

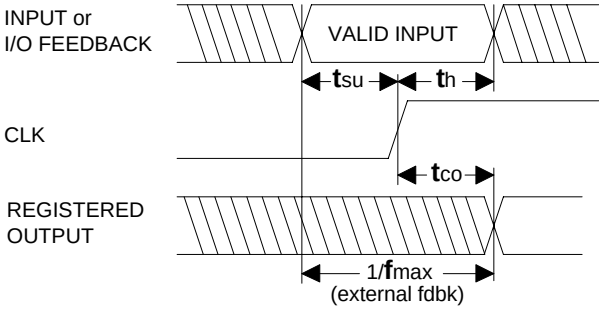
SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	10	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O}$	I/O Capacitance	10	pF	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V

*Characterized but not 100% tested.

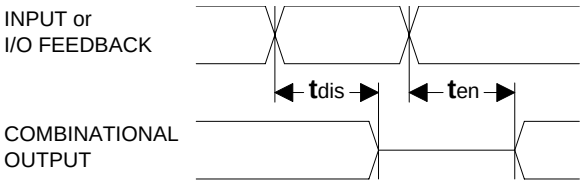
Switching Waveforms



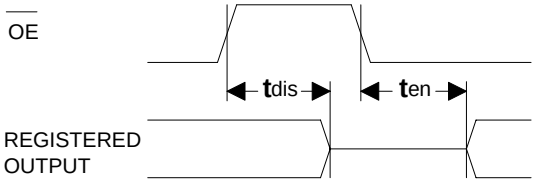
Combinatorial Output



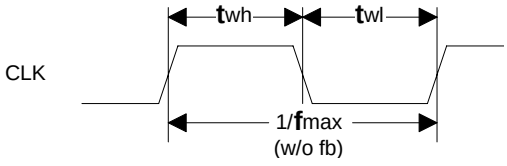
Registered Output



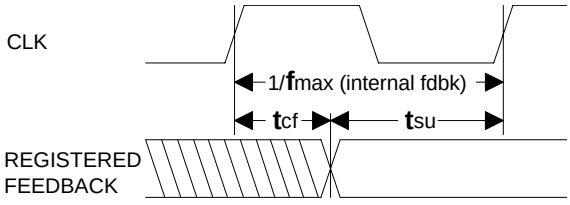
Input or I/O to Output Enable/Disable



$\overline{OE}$ to Output Enable/Disable

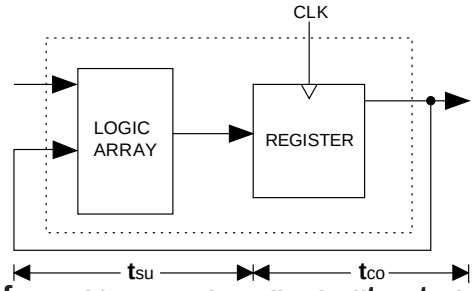


Clock Width



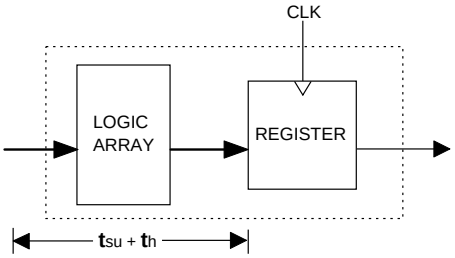
fmax with Feedback

fmax Descriptions



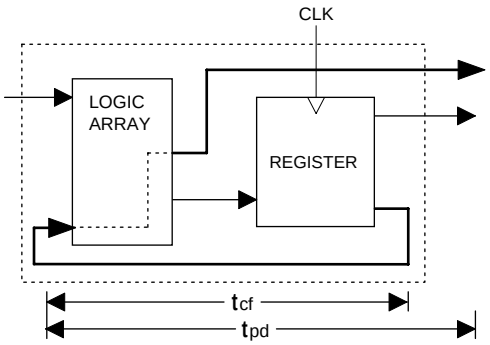
fmax with External Feedback 1/(tsu+tco)

Note: **f**max with external feedback is calculated from measured **t**su and **t**co.



fmax with No Feedback

Note: **f**max with no feedback may be less than 1/(**t**wh + **t**wl). This is to allow for a clock duty cycle of other than 50%.



fmax with Internal Feedback 1/(tsu+tcf)

Note: **t**cf is a calculated value, derived by subtracting **t**su from the period of fmax w/internal feedback (**t**cf = 1/**f**max - **t**su). The value of **t**cf is used primarily when calculating the delay from clocking a register to a combinatorial output (through registered feedback), as shown above. For example, the timing from clock to a combinatorial output is equal to **t**cf + **t**pd.

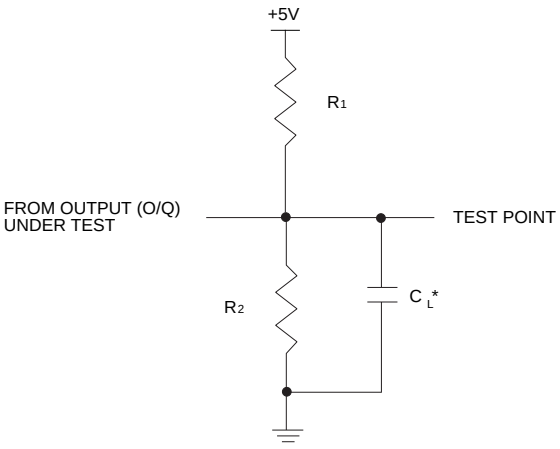
Switching Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure)

Test Condition		R_1	R_2	C_L
A		390Ω	750Ω	50pF
B	Active High	∞	750Ω	50pF
	Active Low	390Ω	750Ω	50pF
C	Active High	∞	750Ω	5pF
	Active Low	390Ω	750Ω	5pF



*C_L INCLUDES TEST FIXTURE AND PROBE CAPACITANCE

GAL20V8 Ordering Information (MIL-STD-883 and SMD)

					Ordering #	
Tpd (ns)	**Tsu (ns)**	**Tco (ns)**	**Icc (mA)**	**Package**	**MIL-STD-883**	**SMD #**
10	10	7	130	24-Pin CERDIP	GAL20V8B-10LD/883	5962-8984004LA
			130	28-Pin LCC	GAL20V8B-10LR/883	5962-89840043A
15	12	12	130	24-Pin CERDIP	GAL20V8B-15LD/883	5962-8984003LA
			130	28-Pin LCC	GAL20V8B-15LR/883	5962-89840033A
20	15	15	130	24-Pin CERDIP	GAL20V8B-20LD/883	5962-8984002LA
			130	28-Pin LCC	GAL20V8B-20LR/883	5962-89840023A

Note: Lattice Semiconductor recognizes the trend in military device procurement towards using SMD compliant devices, as such, ordering by this number is recommended.

Part Number Description