HT82V14

14-Bit CCD/CIS Analog Signal Processor

Features

- Low power CMOS : 350 mW
- 9 ADC clock latency for digital data output
- 14-bit 6 MSPS A/D converter
- 3-channel correlated double sampler
- 1~6 programmable gain
- Input clamp circuitry for CDS-mode
- Internal/external circuitfor CIS
- Internal/external voltage reference
- Internal MUX for channel operation
- 1 or 3-channel operation
- Pixel-rate or line-rate switch operation
- Programmable 3-wire serial interface
- +5V digital I/O compatibility
- 28-pin SOP/SOJ package

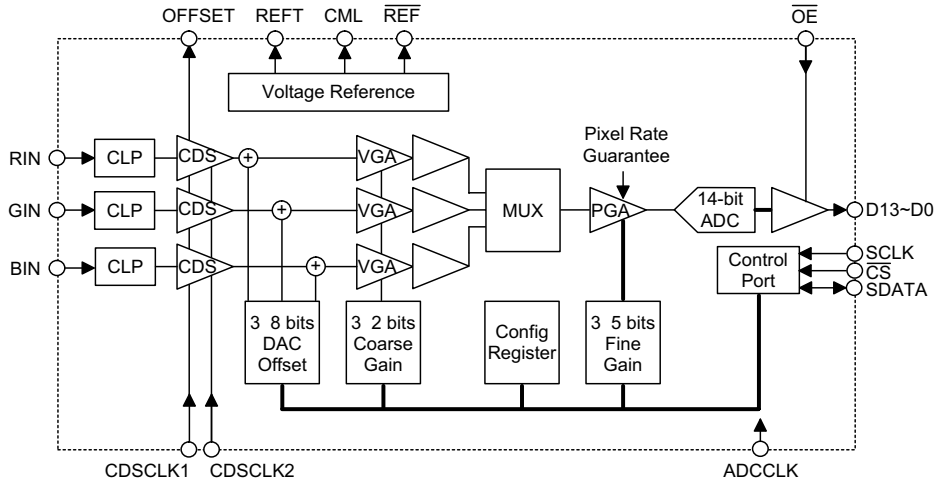
General Description

The HT82V14 is a complete analog signal processor for CCD imaging applications. It features a 3-channel architecture designed to sample and condition the outputs of the trilinear color CCD arrays. Each channel consists of an input clamp, Correlated Double Sampler (CDS), offset DAC and Programmable Gain Amplifier (PGA), multiplexed to a high performance 14-bit A/D converter.

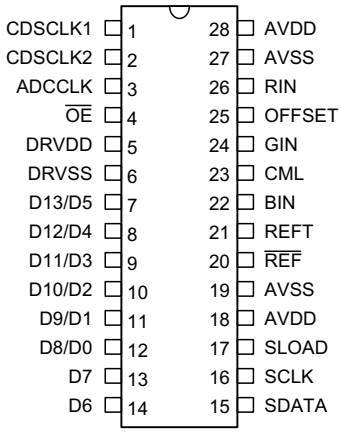
The CDS amplifiers may be disabled for use with sensors such as Contact Image Sensors (CIS) and CMOS active pixel sensors, which do not require CDS.

The 14-bit digital output is multiplexed into an 8-bit output word that is accessed using two read cycles. The internal registers are programmed through a 3-wire serial interface, which provides gain, offset, and operating mode adjustments.

Block Diagram



Pin Assignment



HT82V14
– 28 SOP/SOJ

Pin Description

Pin No.	Pin Name	I/O	Description
1	CDSCLK1	DI	CDS reset clock pulse input
2	CDSCLK2	DI	CDS data clock pulse input
3	ADCCLK	DI	A/D sample clock input for 3-channels mode
4	$\overline{OE}$	DI	Output enable
5	DRVDD	—	Digital driver power
6	DRVSS	—	Digital driver ground
14~7	D0~D13	DO	Digital data output
15	SDATA	DIO	Serial data input/output
16	SCLK	DI	Clock input for serial interface
17	$\overline{CS}$	DI	Chip select
18, 27	AVSS	—	Analog ground
19, 28	AVDD	—	+5V analog supply
20	$\overline{REF}$	AO	Reference decoupling
21	REFT	AO	Reference decoupling
22	BIN	AI	Analog Input, blue
23	CML	AO	Internal reference output
24	GIN	AI	Analog Input, green
25	OFFSET	AO	CIS reference decoupling
26	RIN	AI	Analog input, red

Absolute Maximum Ratings

Supply Voltage .....–0.3V to 5.5V
Input Voltage .....V_{SS}–0.3V to V_{DD}+0.3V
Storage Temperature .....0°C to 70°C
Operating Temperature .....25°C to 50°C

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

Electrical Characteristics

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
Conversion Rate							
	3-channel Mode with CDS	5V±10%	—	—	—	6	MSPS
	1-channel Mode with CDS	5V±10%	—	—	—	5	MSPS
A/D Converter							
	Resolution	5V±10%	—	—	14	—	BIT
	Integral Nonlinearity (INL)	5V±10%	—	—	±4.5	—	LSB
	Differential Nonlinearity (DNL)	5V±10%	—	–0.5	—	1.2	LSB
Analog Inputs							
	Full-scale Input Range	5V±10%	—	—	4	—	Vp-p
	Input Limits	5V±10%	—	AV_{DD}–0.3	—	AV_{DD}+0.3	V
	Input Capacitance	5V±10%	—	—	TBD	—	pF
	Input Current	5V±10%	—	—	TBD	—	μA
Amplifiers							
	Coarse Gain Range	5V±10%	—	1	—	3	V/V
	Coarse Gain Resolution	5V±10%	—	—	2	—	Bits
	PGA Gain Range	5V±10%	—	1	—	2	V/V
	PGA Gain Resolution	5V±10%	—	—	5	—	Bits
	Offset Range	5V±10%	—	–200	—	200	mV
	Offset Resolution	5V±10%	—	—	8	—	Bits

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
Power Supplies							
	AVDD	5V±10%	—	4.75	—	5.25	V
	DRVDD	5V±10%	—	4.75	—	5.25	V
Power Consumption							
	Power Consumption	5V±10%	—	—	350	—	mW

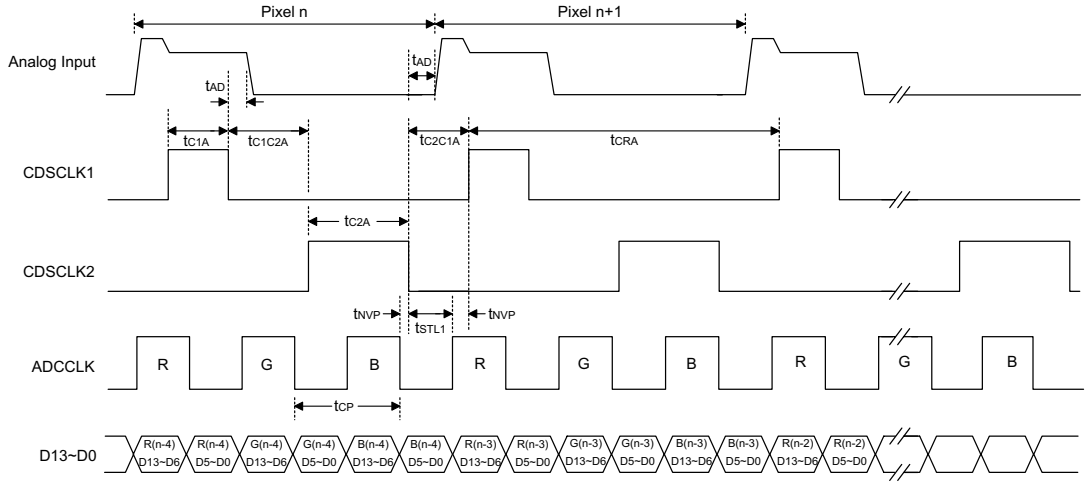
Digital Specifications

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
Logic Inputs							
V_{IH}	High Level Input Voltage	3.3V~5V	—	2.0	—	—	V
V_{IL}	Low Level Input Voltage	3.3V~5V	—	—	—	0.8	V
I_{IH}	High Level Input Current	3.3V~5V	—	—	10	—	μA
I_{IL}	Low Level Input Current	3.3V~5V	—	—	10	—	μA
C_{IN}	Input Capacitance	3.3V~5V	—	—	10	—	pF
Logic Outputs							
V_{OH}	High Level Output Voltage	3.3V~5V	I_{OH}=50μA	4.5	4.9	—	V
V_{OH}	High Level Output Voltage	3.3V~5V	I_{OH}=0.5mA	2.4	—	—	V
V_{OL}	Low Level Output Voltage	3.3V~5V	I_{OL}=–50μA	—	—	0.1	V
V_{OL}	Low Level Output Voltage	3.3V~5V	I_{OL}=–0.6mA	—	—	0.4	V
C_{OUT}	Output Capacitance	3.3V~5V	—	—	5	—	pF

Timing Diagrams

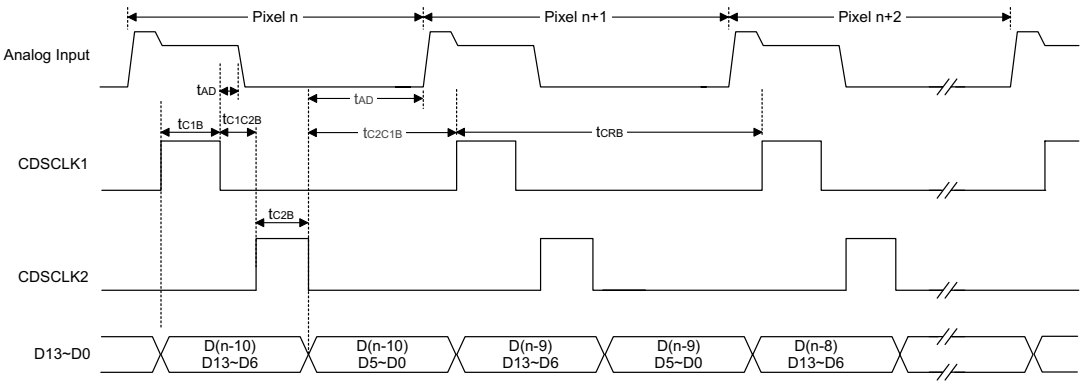
Timing Mode	Sensor Mode	Channel Mode
A	CDS	3-channel internally-defined and pixel-rate mux (00)
B	CDS	1-channel internally-defined mux (01)
C	CIS/SHA	3-channel internally-defined and pixel-rate mux (00)
D	CIS/SHA	1-channel internally-defined mux (01)

Mode A

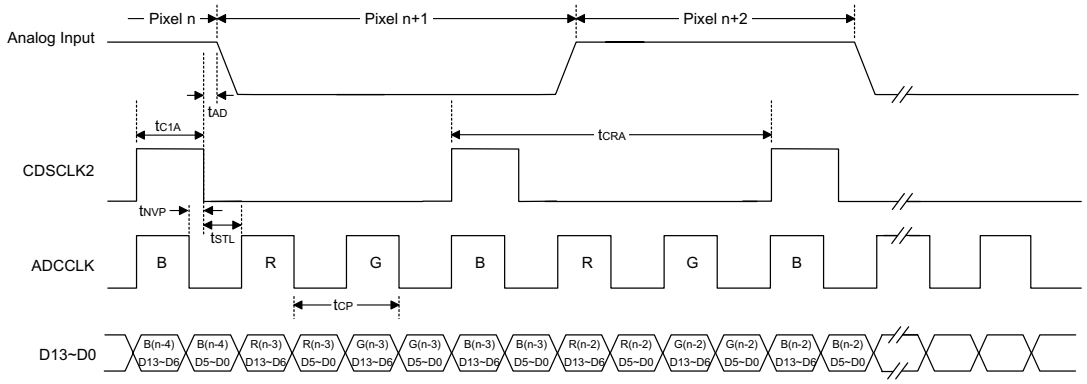


Note: DATA timing from pixel to pixel is decided by the first rising edge of ADCCLK when CDSCLK2 is from high to low.

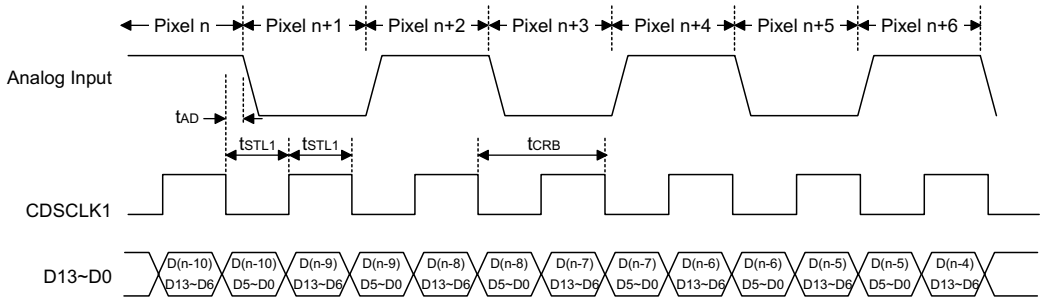
Mode B



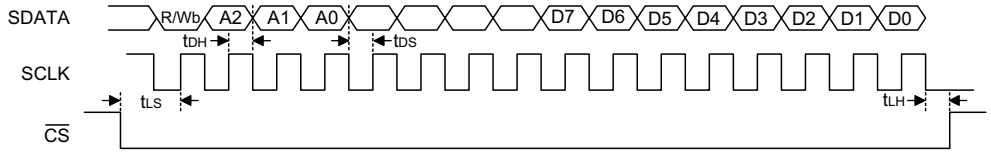
Mode C



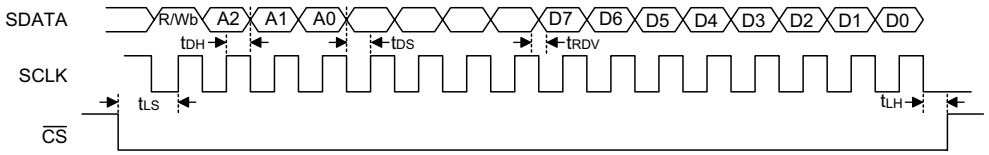
Mode D



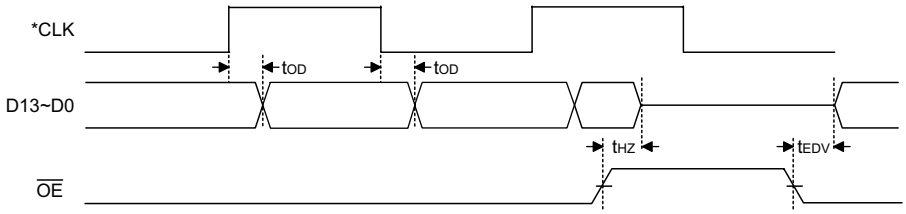
Interface Timing



I/O write operation timing



I/O read operation timing



Note: *CLK: Mode A,C reference ADCCLK
Mode B reference from the vising edge of CDSCLK1 to the falling edge of CDSCLK2
Mode D reference CDSCLK1

Digital output timing

Analog Timing Specification

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{CRA}	3-channel Conversion Rate	—	500	—	ns
t_{CRB}	1-channel Conversion Rate	—	200	—	ns
t_{C1A}	CDSCLK1 Pulse Width	—	50	—	ns
t_{C1B}	CDSCLK1 Pulse Width	—	50	—	ns
t_{C2A}	CDSCLK2 Pulse Width	—	50	—	ns
t_{C2B}	CDSCLK2 Pulse Width	—	50	—	ns
t_{C2C1A}	CDSCLK2 Falling to CDSCLK1 Rising	—	85	—	ns
t_{C2C1B}	CDSCLK2 Falling to CDSCLK1 Rising	—	80	—	ns
t_{C1C2A}	CDSCLK1 Falling to CDSCLK2 Rising	—	20	—	ns
t_{C1C2B}	CDSCLK1 Falling to CDSCLK2 Rising	—	20	—	ns
t_{CP}	ADCCLK Period	—	166	—	ns
t_{STL1}	3-Channel Settling Time	—	80	—	ns
t_{AD}	Aperture Delay	—	10	—	ns
t_{NVP}	Non-overlapping Space	—	5	—	ns

Digital Timing Specification

Symbol	Parameter	Min.	Typ.	Max.	Unit
Data Output					
t_{OD}	Output Delay	—	25	—	ns
t_{EDV}	3-state to Data Valid	15	—	—	ns
t_{HZ}	Output Enable High to 3-state	5	—	—	ns
	Latency	—	9	—	ADCCLK Cycles
Interface Timing					
t_{DS}	Data Setup Time	—	5	—	ns
t_{DH}	Data Hold Time	—	5	—	ns
t_{LS}	Enable Setup Time	—	5	—	ns
t_{LH}	Enable Hold Time	—	5	—	ns
t_{RDV}	Read Data Valid Time	—	3	—	ns

Register Overview

A2	A1	A0	Register
0	0	0	Configuration Register
0	0	1	Red Gain Register
0	1	0	Green Gain Register
0	1	1	Blue Gain Register
1	0	0	Red Offset Register
1	0	1	Green Offset Register
1	1	0	Blue Offset Register
1	1	1	Color Index Register

• Configuration register

Bit	Function
7	Sensor mode
6	Sensor mode
5	Clamp mode
4	Clamp mode
3	External VREF
2	Channel mode
1	Channel mode
0	External CIS reference

• Description of configuration register

7	6	Mode	Function
0	0	CDS	For CCD
0	1	CIS	For CIS dark reference: 1.4V
1	0	SHA	For CIS dark reference: 0V
1	1	Reserved	
5	**4**	**Mode**	**Function**
0	0	Reserved	
0	1	Pixel Clamp	For CDS pixel-by-pixel clamp
1	0	No Clamp	For CDS reset reference<5V
1	1	Reserved	
2	**1**	**Mode**	**Function**
0	0	0	3-channel pixel-rate mux
0	1	1	1-channel for internal define

Gain registers for R, G and B

Bit	Function
7	MSB of Coarse Gain (VGA)
6	LSB of Coarse Gain (VGA)
5	Reserved
4	MSB of Fine Gain (PGA)
3	
2	
1	
0	LSB of Fine Gain (PGA)

Note: VGA: Variable Gain Amplifier, formula: $gain=1+\frac{x}{1.5}$ where x=0~3

PGA: Programmable Gain Amplifier (PGA): specifies R, G, B sequence by color index register, formula: $gain=1+\frac{x}{31}$ where x=0~31

Offset registers for R, G and B

Bit	Function
7	MSB of Offset word
6	
5	
4	
3	
2	
1	
0	LSB of Offset word

Note: Offset range from –200mV to +200mV, 8-bit, 256 levels; (00.....0) equal to –200mV, (100.....0) equal to 0mV, and (11.....1) equal to +198.4mV.

Color index register

Bit7	Reserved
Bit6	Reserved
Bit5	Reserve
Bit4	Index for 3 channel mode
Bit3	Index for 3 channel mode
Bit2	Index for 3 channel mode
Bit1	Index for 1 channel mode
Bit0	Index for 1 channel mode

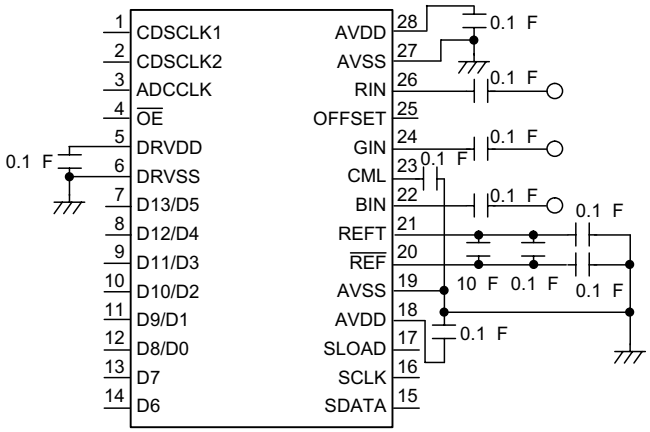
• Truth table for 1 channel index mode

Bit1	Bit0	
0	0	R channel
0	1	G channel
1	0	B channel
1	1	Reserved

• Truth table for 3 channel index mode

Bit4	Bit3	Bit2	
0	0	0	R→G→B
0	0	1	R→B→G
0	1	0	G→R→B
0	1	1	G→B→R
1	0	0	B→R→G
1	0	1	B→G→R
1	1	0	Reserved
1	1	1	Reserved

Application Circuits



HT82V14

Note: Decoupling capacitor of RIN, GIN, BIN may change its value from 300pF to 0.1μF depending on the system environment.

Holtek Semiconductor Inc. (Headquarters)
No.3 Creation Rd. II, Science-based Industrial Park, Hsinchu, Taiwan, R.O.C.
Tel: 886-3-563-1999
Fax: 886-3-563-1189

Holtek Semiconductor Inc. (Taipei Office)
5F, No.576, Sec.7 Chung Hsiao E. Rd., Taipei, Taiwan, R.O.C.
Tel: 886-2-2782-9635
Fax: 886-2-2782-9636
Fax: 886-2-2782-7128 (International sales hotline)

Holtek Semiconductor (Hong Kong) Ltd.
RM.711, Tower 2, Cheung Sha Wan Plaza, 833 Cheung Sha Wan Rd., Kowloon, Hong Kong
Tel: 852-2-745-8288
Fax: 852-2-742-8657