iC-WD A/B/C

SWITCHED-MODE DUAL VOLTAGE REGULATOR

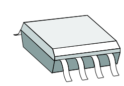
FEATURES

- Input voltage 8 to 36 Vdc
- Highly efficient down converter
- Switching transistor and free-wheeling diode integrated
- Adjustment of the regulator cut-off current with external resistor
- Integrated 100 kHz oscillator without external components
- Switching frequency above the audible range
- Two downstream linear regulators with 200 mA/25 mA output current
- Three different output voltage combinations of 3.3 V version available (see Block Diagram)
- Small residual ripple with low capacitances in the µF range
- Fault message at overtemperature and undervoltage at current-limited open-collector output
- Shutdown of switching regulator at overtemperature
- Internal reference voltages
- ESD protection
- Low space requirement with SO8 resp. tiny DFN10 package
- **Option**: enhanced temperature range of -40 to 85 °C

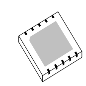
APPLICATIONS

- 5 V resp. 3.3 V supply e.g. from 24 V industrial network

PACKAGES

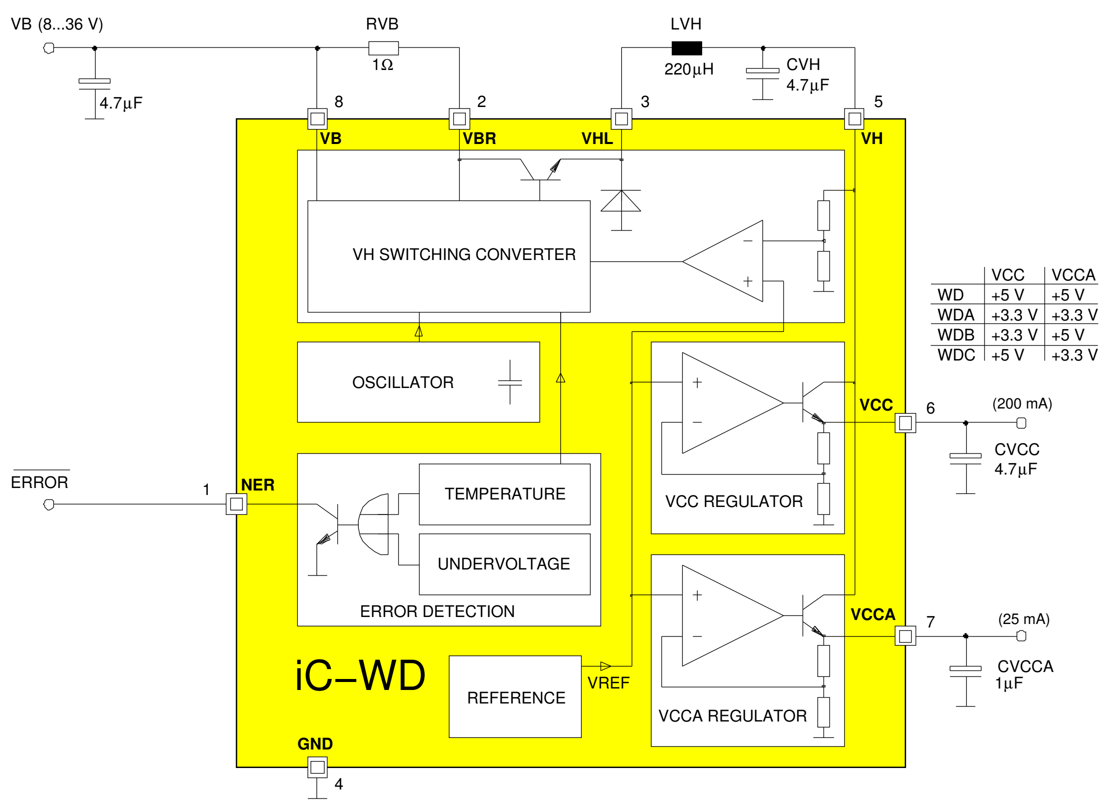


SO8
(optional with thermal pad)



DFN10

BLOCK DIAGRAM



	VCC	VCCA
WD	+5 V	+5 V
WDA	+3.3 V	+3.3 V
WDB	+3.3 V	+5 V
WDC	+5 V	+3.3 V

Pin numbers for SO8 package

DESCRIPTION

The device iC-WD is a monolithic switching regulator with two downstream 5 V resp. 3.3 V linear regulators. In view of the high efficiency of the down converter for an input voltage range of 8 to 36 V, the iC-WD family is well-suited for industrial applications which require a stabilised 5 V resp. 3.3 V power supply with minimal power dissipation and few components.

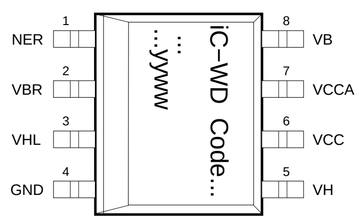
Switching transistor, free-wheeling diode and oscillator are integrated, limiting the necessary external elements for the switching regulator to the inductor, the back-up capacitor and one resistor. This resistor determines the regulator's cut-off current and thus its efficiency in the particular application at hand.

The downstream linear regulators feature a low residual ripple even with relatively small smoothing capacitors in the µF range. The output voltages have an internal reference and are specified ±5% in the entire operating and temperature range. The use of two mutually independent linear regulators makes it possible to isolate the voltage supply of sensitive analogue circuits or sensors from the supply for digital and driver devices.

The chip temperature and the output voltages are monitored. A fault is signalled via the current-limited open-collector output NER, for example by an LED display or a logical link with other error signals from the system. In the event of overtemperature, the switching regulator is disabled to reduce the power dissipation of the chip.

PACKAGES SO8, SO8tp, DFN10 to JEDEC Standard

PIN CONFIGURATION SO8, SO8tp
(top view)

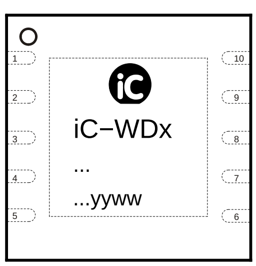


PIN FUNCTIONS

No.	Name	Function
1	NER	Error Output
2	VBR	Pin for shunt
3	VHL	Pin for inductor
4	GND	Ground (reference voltage)
5	VH	Intermediate Voltage
6	VCC	Output (200 mA)
7	VCCA	Output (25 mA)
8	VB	Supply Voltage

The *Thermal Pad* (optional) is to be connected to a Ground Plane on the PCB.

PIN CONFIGURATION DFN10
(top view)



PIN FUNCTIONS

No.	Name	Function
1	NER	Error Output
2	n.c.	
3	VBR	Pin for shunt
4	VHL	Pin for inductor
5	GND	Ground (reference voltage)
6	GND	Ground (reference voltage)
7	VH	Intermediate Voltage
8	VCC	Output (200 mA)
9	VCCA	Output (25 mA)
10	VB	Supply Voltage

The *Thermal Pad* is to be connected to a Ground Plane on the PCB.
Orientation of the package label (iC *WDx ...yyww*) may vary.

ABSOLUTE MAXIMUM RATINGS

Values beyond which damage may occur; device operation is not guaranteed.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
G001	VB	Supply Voltage		-0.3	38	V
G002	V(VBR)	Voltage at VBR		-0.3	38	V
G003	I(VHL)	Current in VHL	Peak duration $\leq$ 50 µs	-800	800	mA
G004	V(VH)	Voltage at VH		-0.3	8	V
G005	I(VCC)	Current in VCC		-500	4	mA
G006	I(VCCA)	Current in VCCA		-100	4	mA
G007	V(NER)	Voltage at NER		-0.3	38	V
G008	Vd()	ESD Susceptibility at all pins	HBM, 100 pF discharged through 1.5 kΩ **WDB, WDC**		2 1.5	kV kV
G009	Tj	Junction Temperature		-40	150	°C
G010	Ts	Storage Temperature		-40	150	°C

THERMAL DATA

Operating Conditions: VB = 8...36 V, L_{VH} = 220 µH, Ri(L_{VH}) $<$ 2 Ω, C_{VH} = 4.7 µF, R_{VB} = 1 Ω

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T01	Ta	Operating Ambient Temperature Range (extended temperature range on request)		-25		70	°C
T02	Rthja	Thermal Resistance Chip to Ambient	SMD mounting on PCB, without additional cooling			170	K/W
T03	Rthja	Thermal Resistance Chip to Ambient	SMD mounting on PCB, with approx. 3 cm² cooling surface (see Evaluation Board)			100	K/W
T04	Rthja	Thermal Resistance Chip to Ambient	SMD mounting on PCB, therm. pad soldered to approx. 2 cm² cooling area		30	60	K/W

All voltages are referenced to ground unless otherwise stated.
All currents into the device pins are positive; all currents out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Operating Conditions: VB = 8...36 V, LVH = 220 µH, Ri(LVH) < 2 Ω, CVH = 4.7 µF, RVB = 1 Ω, Tj = -40...125 °C, unless otherwise noted

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Total Device							
001	VB	Permissible Supply Voltage Range		8		36	V
Linear Regulator VCC (200 mA)							
101	VCC_{nom}	Output Voltage	I(VCC) = -200...0 mA; **WD**, **WDC** **WDA**, **WDB**	 4.75 3.135	 5.00 3.30	 5.25 3.465	 V V
102	I(VCC)	Permissible Load Current		-200		0	mA
103	C_{VCC}	Min. Output Capacity for Stability		4.7			µF
104	VCC_{rip}	Residual Ripple	Evaluation Board (see Fig. 8), Tj = 27 °C: I(VCC) = -200 mA, I(VCCA) = -20 mA		35		mVss
Linear Regulator VCCA (25 mA)							
201	$VCCA_{nom}$	Output Voltage	I(VCCA) = -25...0 mA; **WD**, **WDB** **WDA**, **WDC**	 4.75 3.135	 5.00 3.30	 5.25 3.465	 V V
202	I(VCCA)	Permissible Load Current		-25		0	mA
203	C_{VCCA}	Min. Output Capacity for Stability		1			µF
204	$VCCA_{rip}$	Residual Ripple	Evaluation Board (see Fig. 8), Tj = 27 °C: I(VCC) = -200 mA, I(VCCA) = -20 mA		30		mVss
Switching Regulator VB, VBR, VHL, VH							
301	I0(VB)	Quiescent Current in VB	I(VCC) = 0, I(VCCA) = 0, Tj = 25 °C; VB = 12 V VB = 24 V VB = 30 V		 4.5 3.0 2.5		 mA mA mA
302	I(VB)	Current in VB with partial load	I(VCC) + I(VCCA) = -100 mA, Tj = 25 °C, **WD**, **WDB**, **WDC**; VB = 12 V VB = 24 V VB = 30 V		 72 37 30		 mA mA mA
303	I(VB)	Current in VB with partial load	I(VCC) + I(VCCA) = -100 mA, Tj = 25 °C, **WDA**; VB = 12 V VB = 24 V VB = 30 V		 61 33 24		 mA mA mA
304	I(VB)	Current in VB with full load	I(VCC) + I(VCCA) = -200 mA, Tj = 25 °C, **WD**, **WDB**, **WDC**; VB = 12 V VB = 24 V VB = 30 V		 132 69 55		 mA mA mA
305	I(VB)	Current in VB with full load	I(VCC) + I(VCCA) = -200 mA, Tj = 25 °C, **WDA**; VB = 12 V VB = 24 V VB = 30 V		 116 62 43		 mA mA mA
306	C_{VH}	Charging Capacitor at VH		4.7			µF
307	$R(C_{VH})$	Series Resistance of C_{VH} for stability				12	Ω
308	f0(VHL)	Switching Frequency with no load	I(VCC) = 0, I(VCCA) = 0	20			kHz
309	fl(VHL)	Switching Frequency with load	I(VCC) + I(VCCA) = -200 mA Tj = 27 °C	60	 90	120	kHz kHz
310	V0(VH)	No-load Voltage VH	**WD**, **WDB**, **WDC**; I(VCC) = 0, I(VCCA) = 0, VB = 36 V Tj = 27 °C		 7	 7.5	 V V
311	V0(VH)	No-load Voltage VH	**WDA**; I(VCC) = 0, I(VCCA) = 0, VB = 36 V Tj = 27 °C		 5.4	 5.8	 V V
312	Vl(VH)	Voltage VH with load	**WD**, **WDB**, **WDC**; I(VCC) + I(VCCA) = -200 mA, VB = 8 V Tj = 27 °C	 6	 6.3		 V V

ELECTRICAL CHARACTERISTICS

Operating Conditions: VB = 8...36 V, LVH = 220 µH, Ri(LVH) < 2 Ω, CVH = 4.7 µF, RVB = 1 Ω, Tj = -40...125 °C, unless otherwise noted

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
313	VI(VH)	Voltage VH with load	**WDA**; I(VCC) + I(VCCA) = -200 mA, VB = 8 V Tj = 27 °C	 4.5	 5.0		 V V
314	I_{off}	Max. Cut-off Current in VHL	VH < VI(VH), R_{VB} = 1 Ω	-500	-460	-400	mA
Error Detection NER							
401	Toff	Thermal Shutdown Threshold		130		150	°C
402	Thys	Thermal Shutdown Hysteresis		3		15	°C
403	ΔVCC ΔVCCA	Relative Undervoltage Threshold at VCC, VCCA referenced to VCC_{nom}, $VCCA_{nom}$		8	12	16	%
404	VCChys VCCAhys	Undervoltage Hysteresis referenced to VCC_{nom}, $VCCA_{nom}$		2	4	7	%
405	Vs(NER)	Saturation Voltage lo at NER	I(NER) = 5 mA			0.7	V
406	Isc(NER)	Short-Circuit Current lo in NER	V(NER) = 1...36 V Tj = -40 °C Tj = 27 °C Tj = 70 °C Tj = 125 °C	5	 15 12 10 8	21	mA mA mA mA mA
407	I0(NER)	Collector Off-State Current in NER	NER = off, V(NER) = 0...36 V	0		10	µA

DESCRIPTION OF FUNCTIONS

Fig. 1 illustrates the operating principle of the switching converter in simplified form. When the switch S closes in steady-state condition, a linearly increasing charging current for the capacitor C_{VH} flows through the coil L_{VH} in addition to the load current in R_L. The energy from the supply VB is stored in the coil's magnetic field. When the switch opens, the current flows via the diode through the coil; its energy content is supplied to capacitor and load.

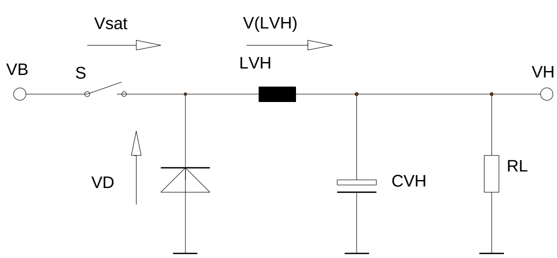


Figure 1: Principle of operation

The block diagram on page 1 shows the iC-WD with typical wiring. The internally generated clock pulse closes the switch between VBR and VHL and the current in the coil rises (charging phase). A control variable, ΔV_R in accordance with the regulating characteristic in Fig. 2, is obtained from the voltage VH and the internal reference voltage and is compared to the voltage at shunt R_{VB}. When the cut-off current $I_{off} = \Delta V_R / R_{VB}$ is reached, the switch opens and the coil current runs free via the integrated power diode (discharge phase). When the next clock signal occurs, this charging and discharging process is repeated. Fig. 6 shows the resulting current and voltage characteristics.

The current rise (t_r) and fall times (t_f) depend on the voltage VH at the inductor. The following approximation applies:

$$t_r = L_{VH} \frac{I_{off}}{VB - V_{sat} - VH} \qquad t_f = L_{VH} \frac{I_{off}}{VH + V_D} \qquad (1)$$

$V_{sat} = VB - VHL$**:** Saturation voltage of the switching transistor plus voltage drop at R_{VB}

V_D**:** Forward voltage of the free-wheeling diode

The current dependencies of the saturation and diode forward voltage (Fig. 3 and 4) are ignored here, as are the losses due to the internal resistance of the coil.

The regulator operates at a constant frequency under load. To prevent VH from rising without load, the oscillator frequency is reduced as the level of voltage VH rises (Fig. 5).

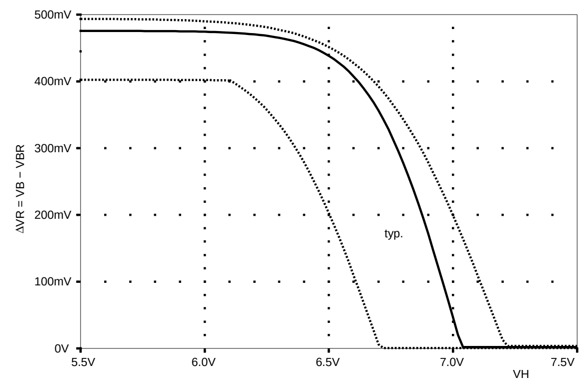


Figure 2: Regulating characteristic $\Delta V_R = f(VH)$

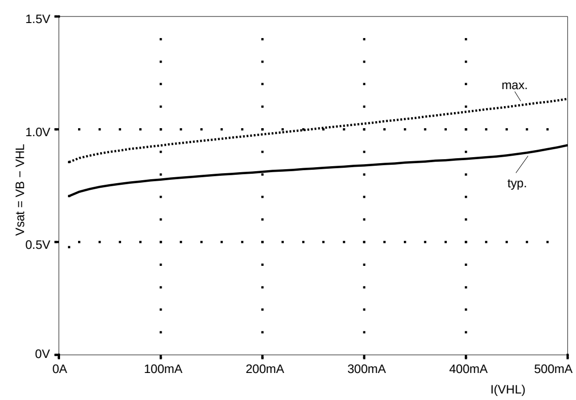


Figure 3: Saturation voltage of switching transistor

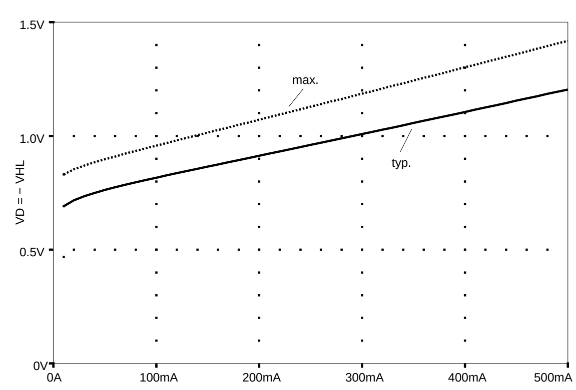


Figure 4: Forward voltage of free-wheeling diode

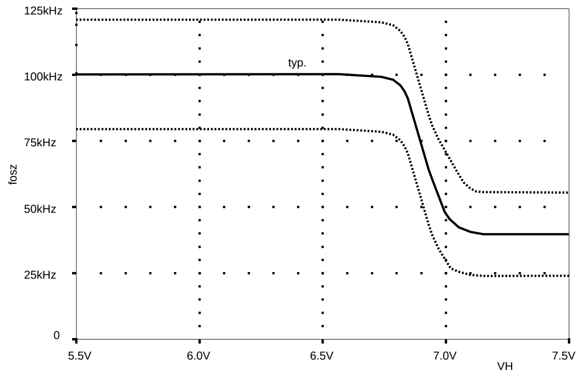


Figure 5: Oscillator Frequency

The following three operating states of the regulator are described as a function of the supply voltage and the load current:

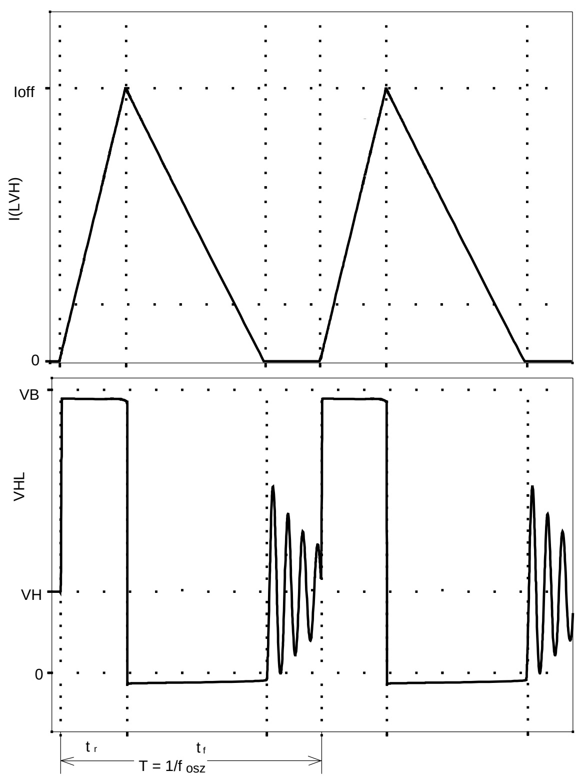


Figure 6: Intermittent flow

SWITCHING REGULATOR: Intermittent flow
When charging and discharging operation are concluded within a single clock pulse period ($t_r + t_f < T$) and the coil current drops to zero, *intermittent flow* prevails (Fig. 6). This is the case when the supply voltage is sufficiently high or the load current sufficiently low. The current-carrying capacity and power consumption of the regulator can be easily specified for this operating mode. Since both the charging and the discharging current flow in VH, the initial approximation of the mean current-carrying capacity of VH is:

$$I_L(VH) = \frac{1}{2} I_{off} \frac{t_r + t_f}{T} \qquad (2)$$

$T = 1/f_{osz}$**:** Period of internal oscillator (Fig. 5)

For load current I_L at output VH, the iC-WD adjusts the cut-off current I_{off} to the following value ($VB > VH + V_{sat}$):

$$I_{off} = \sqrt{2 \cdot I_L(VH) \frac{T}{L_{VH}} \frac{1}{\frac{1}{VB - V_{sat} - VH} + \frac{1}{VH + V_D}}} \qquad (3)$$

Since only during the charging phase current is drawn from supply voltage VB, the mean current consumption is: ($VB > VH + V_{sat}$):

$$I(VB) = I_{off} \frac{t_r}{T} + I_0(VB) \qquad (4)$$

$I_0(VB)$**:** current consumption without load at VCC, VCCA (no-load operation)

SWITCHING REGULATOR: Continuous flow
If the inductor receives recharge with the next clock signal before the coil current has run free, no gap is created in the current. Such *continuous flow* (Fig. 7) occurs when the supply voltage is too low or the load current too high. Since the charging process begins at various current levels not equal to zero, the timing and the required cut-off current are difficult to express. In general, fluctuations occur in the clock frequency at the time constants of the charging and discharging phase, which in turn depend on the of supply voltage and the load current. Since no current gap occurs, the cut-off current may be lower than during intermittent flow (at the same load). The losses in the switching transistor, in the free-wheeling diode and due to the internal resistance of the inductor are consequently lower; the efficiency of the regulator is thus higher. In addition, interference due to the internal resistance of supply voltage source and standby capacitor C_{VH} is lower. Depending on the model and quality of the coil, however, the low frequent fluctuations may be audible.

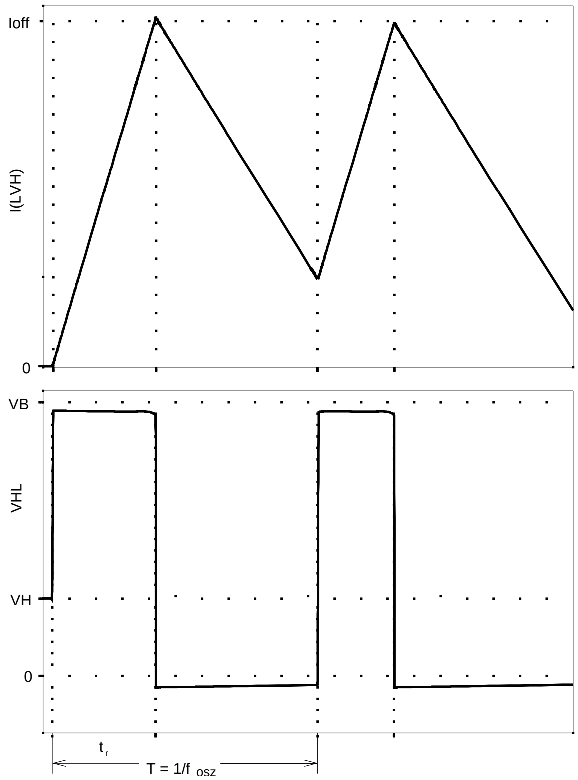


Figure 7: Continous flow

SWITCHING REGULATOR: Operation at low supply voltage

A third operating state occurs when the supply voltage VB is scarcely higher than VH. The cut-off current can no longer be reached in this case since: $(VB - VH - V_{sat})/R_{LVH} < I_{off}$. The switching transistor is switched on continuously and VH reaches: $VH = VB - V_{sat} - I(VH) \times R_{LVH}$. Factoring in this special feature makes it possible to operate the iC-WD even at low supply voltage. Operability is still guaranteed at VB $\approx$ 7.6 V. Nonetheless, the maximum current-carrying capacity depends on the coil's internal resistance and supply voltage VB. The transition from regulator mode to continuously activated transistor is fluid. To avoid feedback of interference voltage from VH to VCC or VCCA the size of standby capacitor C_{VH} should be increased for this type of operation (e.g. 22 µF).

SERIES REGULATORS VCC and VCCA

To obtain the lowest possible interference voltage even with the small smoothing capacitor C_{VH}, two independent series regulators with a NPN emitter follower stage are connected downstream of intermediate voltage VH. The Output voltages VCC or VCCA are constant ±5%. The suppression of interference voltage for the output voltages is best when VH is also no lower than 6.0 V dynamically (iC-WDA: 4.3 V).

The series regulators are compensated internally, hence they are stable during no-load operation, without external capacitance. Stability over the entire load range is ensured by the minimum capacitance values for C_{VCC} and C_{VCCA} given in the electrical characteristics. Current-limited outputs are used as protection against destruction in the event of a short circuit.

FAULT EVALUATION

The two output voltages VCC and VCCA are monitored. When the voltage drops below the undervoltage threshold (due to overload, etc.), a message is sent to the current-limited open-collector output NER (active low). The chip temperature is also monitored. In the event of overtemperature the switching regulator is turned off and it is not enabled against until the chip temperature has decreased. This thermal shutdown of the regulator is indicated by NER = low. Since the fault output NER is current-limited, an LED can be connected directly for the optical message display, however the additional power dissipation which occurs

$$P_v = I(NER) \times (VB - V_{fw}(LED)) \qquad (5)$$

must be taken into account. A resistor R_{LED} in series with the LED can reduce the additional chip power dissipation in the event of a fault. CMOS- or TTL-compatible logic inputs can be activated with a pull-up resistor at NER.

APPLICATIONS INFORMATION

DIMENSIONING

The size of shunt R_{VB} determines the cut-off current I_{off}. By varying this in combination with the value for the inductor L_{VH}, the power input, the efficiency and the timing can be adapted to the application.

Normally the supply voltage range and the maximum output current for VCC and VCCA is specified. Define whether or not only intermittent flow is desired. The maximum inductance L_{VH} can be estimated on the following basis: In the worst situation, charging and discharging process last exactly one period, which is the case at minimum supply power. The cut-off current adjusts to $I_{off} = 2 \times I_{L_{max}}(VH)$. From equation (1) it follows that:

$$L_{VH_{max}} = \frac{T_{min}}{2 I_{L_{max}}(VH)} \times \frac{1}{\frac{1}{VB_{min} - V_{sat} - VH} + \frac{1}{VH + V_D}}$$

Using equation (3) it is possible to determine the maximum cut-off current for intermittent flow. The maximum value for VB must be inserted:

$$I_{off_{max}} = \sqrt{2 \cdot I_{L_{max}}(VH) \frac{T_{max}}{L_{VH}} \cdot \frac{1}{\frac{1}{VB_{max} - V_{sat} - VH} + \frac{1}{VH + V_D}}}$$

The shunt R_{VB} can be dimensioned with this information. ΔVR_{max} can be obtained from Fig. 2:

$$R_{VB} = \frac{\Delta V_{R_{max}}}{I_{off_{max}}}$$

EXAMPLE

Specified are: VB = 18...36 V, $I_{L_{max}}$ = 100 mA; the maximum inductance can be estimated to:

$$L_{VH_{max}} = \frac{1/125\,kHz}{200\,mA} \cdot \frac{1}{\frac{1}{18\,V - 1.1\,V - 7.0\,V} + \frac{1}{7.0\,V + 1.1\,V}} = 178\,\mu H$$

The inductance selected is 150 µH, for example. Consequently, the maximum required cut-off current and the shunt are found to be:

$$I_{off_{max}} = \sqrt{2 \cdot 100\,mA \frac{1/75\,kHz}{150\,\mu H} \cdot \frac{1}{\frac{1}{30\,V - 1.1\,V - 7\,V} + \frac{1}{7\,V + 1.1\,V}}} = 324\,mA$$

$$\Rightarrow R_{VB} = \frac{400\,mV}{324\,mA} \approx 1.2\,\Omega$$

It is not always possible to dimension the circuit for intermittent flow, particularly not when high output currents are required with a low supply voltage. Permitting continuous flow may prove conducive to higher efficiency and less interference. The inductance selected is to be higher than in the above formula; the equations for maximum cut-off current and the shunt can be used with the selected coil.

It is simplest to ascertain the correct dimensioning by experiment in a test set-up (Evaluation Board). The dimensioning shown in the block diagram (L_{VH} = 220 µH, R_{VB} = 1 Ω is suitable for maximum performance throughout the entire specification range.

SELECTING THE COMPONENTS

Since the coil must not to become saturated, it should be designed for maximum cut-off current. This can be checked by testing the coil current with a current probe: In the event of saturation the current rises much more sharply than with low currents. A low internal resistance of the coil reduces the losses and increases the regulator's efficiency. When the supply voltage is low, this internal resistance can determine the maximum available output current (equation 4).

The EMI (electromagnetic interference) caused by the coil should be taken into account. Toroidal core coils have little noise radiation but are expensive and difficult to install. Bar cores are reasonably priced and easy to handle but emit higher radiation. Reasonably priced RF chokes in the range of a few tens to a few hundreds µH are suitable for modest EMI requirements.*

Additional interference may be caused by decaying of the voltage at VHL when the coil current drops to zero (Fig. 6). Parasitic capacitances at VHL form an oscillating circuit with the coil. This undesirable oscillating circuit can be damped to an uncritical magnitude by installing a resistor ($> 10\,k\Omega$) parallel to the coil.

The selection of the backup capacitor C_{VH} is unproblematic. Due to the series regulators, the ripple of the intermediate voltage VH does not affect the output voltages VCC and VCCA. Therefore a low capacitance level without special demands on the internal resistance is sufficient. A combination of electrolytic and ceramic capacitor (e.g. 4.7 µF/100 nF) is recommended. Tantalum capacitors are also possible when they are allowed to operate at AC amplitudes like the residual ripple of voltage VH.

The stability of the series regulators is guaranteed for the entire load range when the values for C_{VCC} and C_{VCCA} given in the electrical characteristics are selected. The suppression of interference voltage is improved by small capacitor series resistors. The combination of tantalum and ceramic capacitors is also recommended in this case. If one of the two outputs remains open, its capacitor can be omitted.

To avoid feedback of interference from supply voltage VB onto output voltages VCC and VCCA, provide blocking directly at pin VB. A combination of tantalum and ceramic capacitors is also recommended in this case (several µF/100 nF).

PRINTED CIRCUIT BOARD LAYOUT

The GND path from the switching regulator and from each series regulator should be strictly separated to avoid cross couplings. The neutral point of all GND conductors is the GND connection at the iC-WD. It is possible and not critical, however, to route the GND of the supply VB and the base point of capacitor C_{VH} together to the neutral point. The capacitor C_{VH} should be very close to the pin VH however. To keep down the decay at the open end of the coil (pin VHL), the capacitance of this connection should be low, that means the connection should be short.

The blocking capacitors of supply voltage VB are to be placed as close as possible to pins VB and GND. The capacitors for the outputs VCC and VCCA should be placed directly by the load and not directly by the iC to also block interferences which are coupled via the wiring to the load. A ground plane should be cut out underneath the wiring of C_{VCC} and C_{VCCA}. The printed circuit conductor between VB, the shunt RVB, and VBR should have a low impedance, since voltage drops in the supply path change the effective size of the shunt and reduce the maximum cut-off current.

The *Thermal Pad* (optional with the SO8) should be connected to an appropriate copper area on the PCB. It has proven to be advantageous to use *thermal vias* directly underneath the iC to transfer the power dissipation to a different layer, e.g. a ground plane.

* e.g.: Siemens Matsushita B78108-S1224-J (220 µH/250 mA, axial leads), TDK series NLC565050T-... (SMD), TOKO series 10RF459-... (SMD shielded)

EVALUATION BOARD

For the iC-WD devices an Evaluation Board is available for test purpose. The following figures show the schematic as well as the layout of the Evaluation Board.

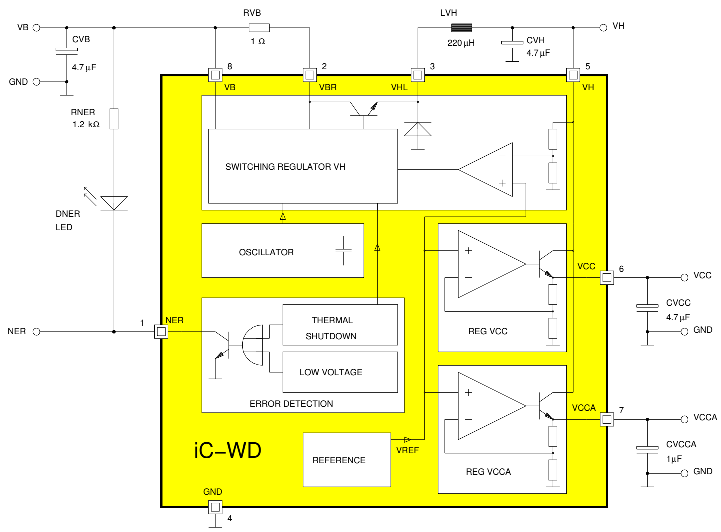


Figure 8: Schematic diagram of the Evaluation Board

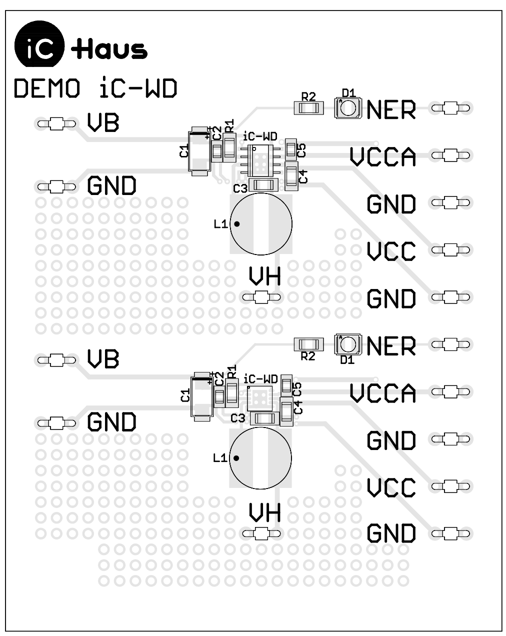


Figure 9: Evaluation Board (components side)

ORDERING INFORMATION

Typ (VCC/VCCA)	Package	Order Designation
iC-WD (5/5 V)	SO8 SO8 thermal pad DFN10 (on request)	iC-WD SO8 iC-WD SO8-TP iC-WD DFN10
Evaluation Board iC-WD	-	iC-WD EVAL WD2D
iC-WDA (3.3/3.3 V)	DFN10	iC-WDA DFN10
Evaluation Board iC-WDA	-	iC-WDA EVAL WD2D
iC-WDB (3.3/5 V)	DFN10	iC-WDB DFN10
Evaluation Board iC-WDB	-	iC-WDB EVAL WD2D
iC-WDC (5/3.3 V)	DFN10	iC-WDC DFN10
Evaluation Board iC-WDC	-	iC-WDC EVAL WD2D

For technical support, information about prices and terms of delivery please contact:

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Appointed local distributors: http://www.ichaus.de/support_distributors.php