

### GS2914 HD-LINX™ III Serial Digital DC Restorer for Fibre-Optic Receivers

### **Features**

- SMPTE 424M, SMPTE 292M, SMPTE 344M and SMPTE 259M compliant
- Automatic gain control
- DC restore for immunity to SDI pathological bit patterns
- Differential outputs with on-chip  $100\Omega$  differential data output termination
- Manual Bypass
- Supports DVB-ASI at 270Mb/s
- Programmable carrier detect threshold adjustment
- Single power supply operation at 3.3V
- 178mW power
- Operating temperature range: 0°C to +70°C
- Small footprint QFN package (4mm x 4mm)
- Pb-free and RoHS compliant

### **Applications**

 SMPTE 424M, SMPTE 292M, SMPTE 344M and SMPTE 259M Fibre-Optic Serial Digital Interfaces

### **Description**

The GS2914 is a high-speed BiCMOS integrated circuit designed to provide AGC and DC restoration of signals from an optical receiver.

The GS2914 is designed to support SMPTE 424M, SMPTE 292M, SMPTE 344M and SMPTE 259M, and is optimized for performance at 270Mb/s, 1.485Gb/s and 2.97Gb/s.

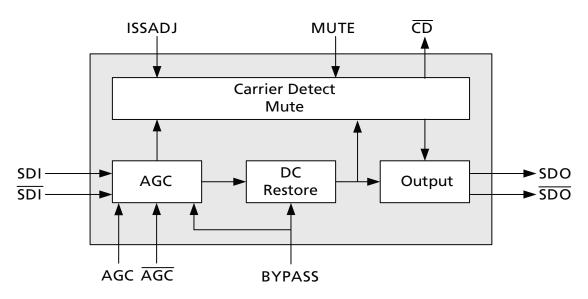
The GS2914 features DC restoration to compensate for the DC content of SMPTE pathological test patterns.

The carrier detect output pin  $(\overline{CD})$  indicates whether a valid input signal has been detected. It can be connected directly to the MUTE pin to mute the output on loss of carrier. A voltage programmable threshold (ISSADJ) forces  $\overline{CD}$  high when input signal strength is below this threshold. This allows the GS2914 to distinguish between low amplitude SDI signals and noise at the input of the device.

Power consumption is typically 178mW.

The GS2914 is Pb-free, and the encapsulation compound does not contain halogenated flame retardant.

This component and all homogeneous subcomponents are RoHS compliant.



**GS2914 Functional Block Diagram** 

## **Revision History**

Version	ECR	PCN	Date	Changes and/or Modifications
0	151229	-	February 2009	Converted to Data Sheet. Changes to ISSADJ DC Voltage and Range values in Table 2-1: DC Electrical Characteristics. Addition of Figure 4-1: ISSADJ Muting Characteristics.
С	151019	-	December 2008	Separation of Min/Max Input Voltage Swing to Table 2-2: AC Electrical Characteristics.
В	150985	-	November 2008	Converted to Preliminary Data Sheet.
Α	150285	-	August 2008	New Document.

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## 1. Pin Out

## 1.1 GS2914 Pin Assignment

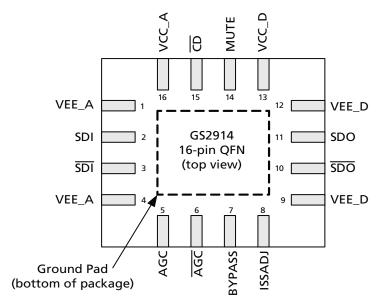


Figure 1-1: 16-Pin QFN

## 1.2 GS2914 Pin Descriptions

Table 1-1: GS2914 Pin Descriptions

Pin Number	Name	Timing	Туре	Description
1, 4	VEE_A	Analog	Power	Most negative power supply for analog circuitry.
				Connect to GND.
2, 3	SDI, <del>SDI</del>	Analog	Input	Serial digital differential input.
5, 6	AGC, $\overline{AGC}$	Analog	-	External AGC capacitor.
				Connect pin 5 and pin 6 together as shown in the Typical Application Circuit on page 10.
7	BYPASS	Not Synchronous	Input	Forces the amplification and DC RESTORE stages into bypass mode when HIGH. No amplification occurs in this mode.
8	ISSADJ	Analog	Input	Input Signal Strength Adjust.
				Adjusts the minimum input signal strength which will be restored. See Section 4.2. and Section 4.3
9, 12	VEE_D	Analog	Power	Most negative power supply for the digital circuitry and output buffer.
				Connect to GND.
10, 11	SDO, SDO	Analog	Output	Restored serial digital differential output.



Table 1-1: GS2914 Pin Descriptions (Continued)

Pin Number	Name	Timing	Туре	Description
13	VCC_D	Analog	Power	Most positive power supply for the digital I/O pins of the device. Connect to +3.3V DC.
14	MUTE	Not Synchronous	Input	CONTROL SIGNAL INPUT levels are LVCMOS/LVTTL compatible. (3.3V Tolerant) Controls output behaviour on SDO and SDO See Section 4.3.
15	CD	Not Synchronous	Output	STATUS SIGNAL OUTPUT Signal levels are LVCMOS/LVTTL compatible. Indicates the presence of a good input signal. See Section 4.3.
16	VCC_A	Analog	Power	Most positive power supply for the analog circuitry of the device. Connect to +3.3V DC.
-	Center Pad	-	Power	Internally bonded to VEE_A.



## 2. Electrical Characteristics

## 2.1 Absolute Maximum Ratings

Parameter	Value
Supply Voltage	-0.3V to +3.6 VDC
Input ESD Voltage	4kV
Storage Temperature Range	-50°C < T <sub>s</sub> < 125°C
Input Voltage Range (any input)	-0.3 to (V <sub>CC</sub> +0.3)V
Operating Temperature Range	0°C to 70°C
Solder Reflow Temperature	260°C

### 2.2 DC Electrical Characteristics

**Table 2-1: DC Electrical Characteristics** 

 $V_{CC}$  = 3.3V ±5%,  $T_A$  = 0°C to 70°C, unless otherwise shown

Parameter	Symbol	Conditions	Min	Тур	Max	Units	Notes
Supply Voltage	V <sub>CC</sub>	_	3.135	3.3	3.465	V	±5%
Power Consumption	P <sub>D</sub>	T <sub>A</sub> = 25°C	_	178	280	mW	_
Supply Current	I <sub>s</sub>	T <sub>A</sub> = 25°C	_	54	80	mA	_
Output Common Mode Voltage	V <sub>CMOUT</sub>	T <sub>A</sub> = 25°C	-	V <sub>CC</sub> - ΔV <sub>SDO</sub> /2	-	V	-
Input Common Mode Voltage	V <sub>CMIN</sub>	T <sub>A</sub> = 25°C	_	1.75	-	V	_
ISSADJ Range	-	T <sub>A</sub> = 25°C	-	2.3 - 3.3	_	V	-
CD Output Voltage	V <sub>CD(OH)</sub>	Carrier not present	2.4	-	-	V	-
	V <sub>CD(OL)</sub>	Carrier present	_	-	0.4	V	_
Mute Input Voltage Required to Force Outputs to Mute	$V_{Mute}$	Min to Mute	2.0	-	-	V	-
Mute Input Voltage Required to Force Outputs Active	$V_{Mute}$	Max to Activate	-	-	0.8	V	-



### 2.3 AC Electrical Characteristics

**Table 2-2: AC Electrical Characteristics** 

 $V_{CC}$  = 3.3V ±5%,  $T_A$  = 0°C to 70°C, unless otherwise shown

Parameter	Symbol	Conditions	Min	Тур	Max	Units	Notes
Serial input data rate	DR <sub>SDO</sub>	-	143	_	2970	Mb/s	_
Minimum Input Voltage Swing	$\Delta V_{SDIMIN}$	T <sub>A</sub> =25°C, differential	-	10	-	mV <sub>p-p</sub>	-
Input Voltage Swing	$\Delta V_{SDI}$	Differential	20	_	500	mV <sub>p-p</sub>	-
Output Voltage Swing	$\Delta V_{SDO}$	100Ω load, $T_A = 25$ °C, differential	550	750	1100	$mV_{p-p}$	-
Output Jitter		270Mb/s 500mV input	-	0.1	0.2	UI	1,3
		270Mb/s 10mV input	-	-	0.2	UI	2,3
	_	1.485Gb/s 500mV input	-	0.2	0.25	UI	1,3
		1.485Gb/s 10mV input	-	-	0.3	UI	2,3
	_	2.97Gb/s 500mV input	-	0.2	0.3	UI	1,3
		2.97Gb/s 10mV input	-	-	0.4	UI	2,3
Output Rise/Fall time	-	20% - 80%	40	80	220	ps	-
Mismatch in rise/fall time	-	_	-	_	30	ps	-
Duty cycle distortion	-	-	-	-	100	ps	-
Overshoot	-	-	-	_	10	%	-
Input Resistance	-	single ended	-	1.52	-	kΩ	-
Input Capacitance	-	single ended	-	1	-	pF	-
Output Resistance – single ended		single ended	_	50	-	Ω	-

### NOTES:



<sup>1.</sup> All parts production tested. In order to guarantee jitter over the full range of specification ( $V_{CC} = 3.3V \pm 5\%$ ,  $T_A = 0$ °C to 70°C, and input swing) the recommended applications circuit must be used.

<sup>2.</sup> Based on characterization data using the recommended applications circuit, at  $V_{CC} = 3.3V$ ,  $T_A = 25$ °C.

 $<sup>{\</sup>it 3. \ Pathological\ test\ signal\ was\ used}.$ 

# 3. Input/Output Circuits

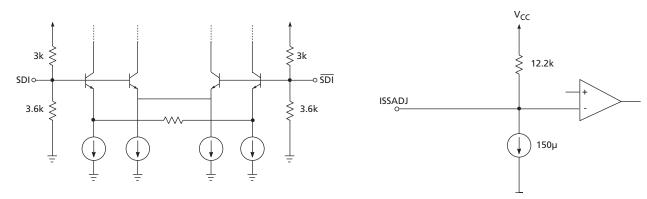


Figure 3-1: Input Equivalent Circuit

Figure 3-2: ISSADJ Equivalent Circuit

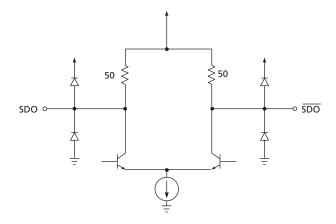


Figure 3-3: Output Circuit

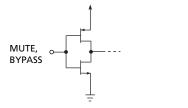


Figure 3-4: MUTE and BYPASS Circuits

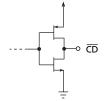


Figure 3-5: CD Circuit



## 4. Detailed Description

The GS2914 is a high speed BiCMOS IC designed to amplify and DC restore serial digital signals.

The GS2914 can DC restore serial digital signals, and will typically restore signals as low as 10mV. The GS2914 is powered from a single +3.3V power supply and consumes approximately 150mW of power.

## 4.1 Serial Digital Inputs

The serial data signal may be connected to the input pins ( $SDI/\overline{SDI}$ ) in either a differential or single-ended configuration. AC-coupling of the inputs is recommended, as the SDI and  $\overline{SDI}$  inputs are internally biased at approximately 1.8V.

## 4.2 Programmable Input Signal Strength Adjust (ISSADJ)

For SMPTE 259M inputs, the GS2914 incorporates a programmable Input Signal Strength Adjust (ISSADJ) threshold.

This feature can be useful in applications where there are multiple input channels using the GS2914 and the maximum gain can be limited to avoid crosstalk.

The ISSADJ pin acts to change the threshold of the Carrier Detect  $(\overline{CD})$  pin. When the input signal drops below a certain threshold, the  $\overline{CD}$  pin will be driven high, indicating that there is not a valid input signal. By increasing the voltage level at ISSADJ, the threshold at which the carrier is detected is increased, or  $\overline{CD}$  will be driven HIGH at a higher input amplitude level. Decreasing the voltage will decrease the threshold at which carrier is detected. In order to enable automatic muting of the output of the GS2914, the  $\overline{CD}$  pin should be connected directly to the MUTE pin. In applications where programmable input signal swing adjust is not required, the ISSADJ pin may be left unconnected.

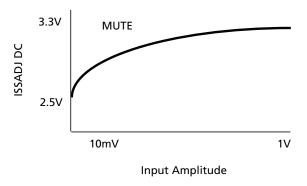


Figure 4-1: ISSADJ Muting Characteristics



### 4.3 Mute and Carrier Detect

The GS2914 includes a MUTE input pin that allows the application interface to mute the serial digital output at any time. Set the MUTE pin HIGH to mute SDO and  $\overline{\text{SDO}}$ . In this case, the outputs will mute regardless of the setting of the BYPASS pin.

A Carrier Detect output pin  $(\overline{CD})$  indicates the presence of a valid signal at the input of the GS2914. When  $\overline{CD}$  is LOW, the device has detected a valid input on SDI and  $\overline{SDI}$ . When  $\overline{CD}$  is HIGH, the device has not detected a valid input.

NOTE: The MUTE pin may be connected directly to the  $\overline{\text{CD}}$  pin to allow mute on loss of carrier.

NOTE:  $\overline{\text{CD}}$  will only detect loss of carrier for data rates greater than 19Mb/s. The  $\overline{\text{CD}}$  output pin may be connected directly to the MUTE input pin to enable automatic muting of the GS2914 when no valid input signal has been detected.

NOTE: If the minimum input signal strength is not achieved and the device is not in bypass mode, the GS2914 will not assert the  $\overline{\text{CD}}$  pin even if a carrier is present.

Table 4-1: Mute Input Table

Mute	Function
0	SDO and SDO operate normally
1	SDO and SDO are forced to a steady state

Table 4-2: CD Output Table

CD	Input Status
0	Valid Input on SDI, SDI pins
1	Input is not valid

## 5. Application Information

## 5.1 PCB Layout

Special attention must be paid to component layout when designing serial digital interfaces for HDTV. An FR-4 dielectric can be used, however, controlled impedance transmission lines are required for PCB traces longer than approximately 1cm. Note the following PCB artwork features used to optimize performance:

- PCB trace width for HD rate signals is closely matched to SMT component width to minimize reflections due to change in trace impedance.
- The PCB ground plane is removed under the GS2914 input components to minimize parasitic capacitance.

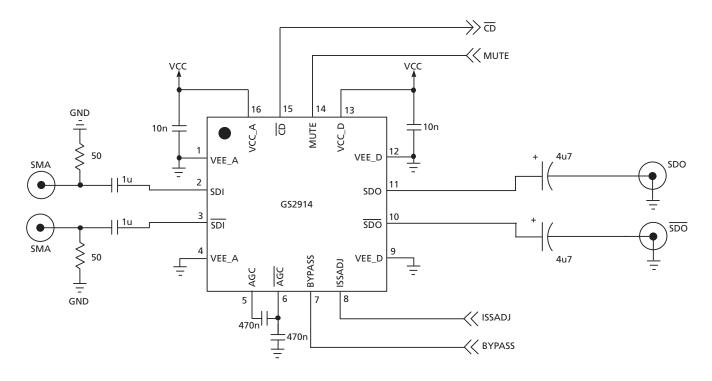


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- The PCB ground plane is removed under the GS2914 output components to minimize parasitic capacitance.
- High speed traces are curved to minimize impedance changes.

## **5.2 Typical Application Circuit**



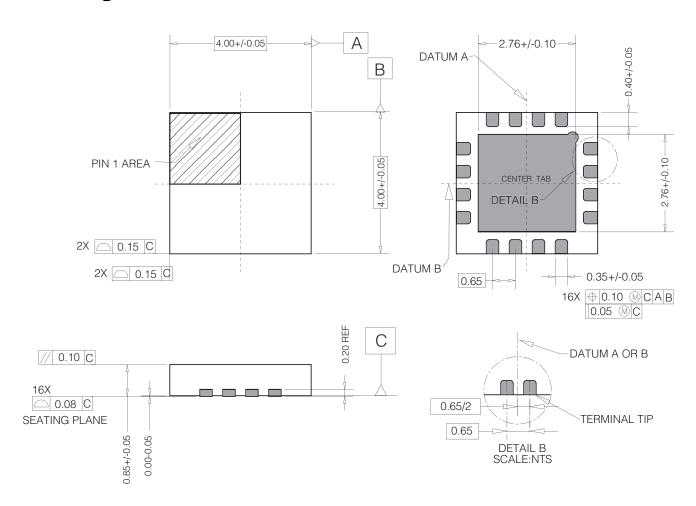
NOTE: All resistors in Ohms, capacitors in Farads, and inductors in Henrys, unless otherwise noted. \* Value dependent on layout

Figure 5-1: GS2914 Typical Application Circuit



# **6. Package & Ordering Information**

## **6.1 Package Dimensions**

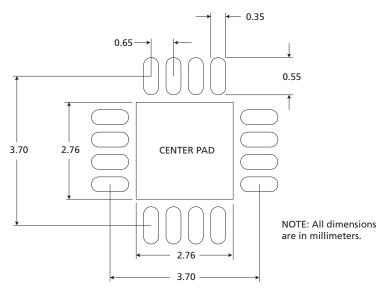


## **6.2 Packaging Data**

Parameter	Value
Package Type	4mm x 4mm 16-pin QFN
Package Drawing Reference	JEDEC M0220
Moisture Sensitivity Level	3
Junction to Case Thermal Resistance, $\theta_{ extstyle{j-c}}$	31.0°C/W
Junction to Air Thermal Resistance, $\theta_{j-a}$ (at zero airflow)	43.8°C/W
Psi, ψ	11.0°C/W
Pb-free and RoHS compliant	Yes



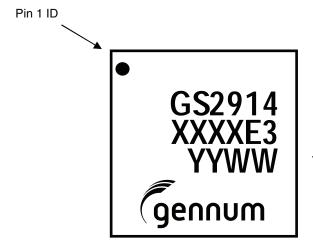
## **6.3 Recommended PCB Footprint**



The Center Pad should be connected to the most negative power supply plane for analog circuitry in the device (VEE\_A) by a minimum of 5 vias.

NOTE: Suggested dimensions only. Final dimensions should conform to customer design rules and process optimizations.

## 6.4 Marking Diagram



XXXX - Lot/Work Order ID

YYWW - Date Code

YY - 2-digit year

WW - 2-digit week number





## **6.5 Solder Reflow Profiles**

The device is manufactured with Matte-Sn terminations and is compatible with both standard eutectic and Pb-free solder reflow profiles. MSL qualification was performed using the maximum Pb-free reflow profile shown in Figure 6-1.

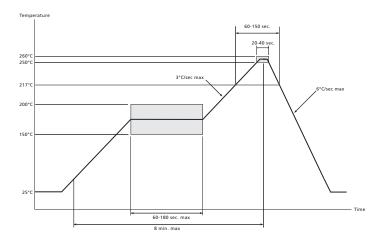


Figure 6-1: Maximum Pb-free Solder Reflow Profile (Preferred)

## **6.6 Ordering Information**

	Part Number	Package	Temperature Range
GS2914	GS2914-CNE3	16-pin QFN	0°C to 70°C
GS2914	GS2914-CNTE3	16-pin QFN Tape & Reel (250pcs)	0°C to 70°C



## DOCUMENT IDENTIFICATION DATA SHEET

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