❑ MN101E58 Series

Type	MN101EF58G
Internal ROM type	FLASH
ROM (byte)	128K
RAM (byte)	6K
Package (Lead-free)	LQFP064-P-1414, TQFP064-P-1010C
Minimum Instruction Execution Time	50 ns (at 2.7 V to 5.5 V, 20 MHz) 125 ns (at 1.8 V to 5.5 V, 8 MHz) *: at internal 2 , 3 , 4 , 5 , 6 , 8 , 10 times oscillation used

■ Interrupts

5 external interrupts. 29 internal interrupts

RESET. NMI. External 0 to 4. Timer 0 to 4. Timer 6. Timer 7 (2 systems). Timer 8 (2 systems). Timer 9 (3 systems). Time base. 24H timer. Alarm. Serial 0 (2 systems). Serial 1 (2 systems). Serial 2 (2 systems). Serial 4 (2 systems). LIN. A/D conversion. ATC. Key interrupt. Low voltage detection

■ Timer Counter

8-bit timer × 7

Timer 0 .....Timer pulse output. Added pulse(2-bit)type PWM output to large current terminal TM0IOB possible. Event count. Simple pulse width measurement

Timer 1 .....Timer pulse output. Event count. 16-bit cascade connected (timer 0, 1). Timer synchronous output

Timer 2 .....Timer pulse output. Added pulse(2-bit)type PWM output to large current terminal TM2IOB possible. Event count. Simple pulse width measurement. 24-bit cascade connected (timer 0, 1, 2). Timer synchronous output

Timer 3 .....Timer pulse output. Event count. 16-bit cascade connected (timer 2, 3). 32-bit cascade connected (timer 0, 1, 2, 3)

Timer 4 .....Timer pulse output. Added pulse (2-bit) type PWM output. Event count. Simple pulse width measurement

Timer 6 .....8-bit freerun timer

Timer A.....Baud rate timer. Clock output for peripheral function

16-bit timer × 3

Timer 7 .....Timer pulse output to large current terminal TM7IOB possible. Event count. High accuracy PWM/IGBT output (cycle/duty continuous variable). Pulse width measurement. Timer synchronous output. Input capture (both edge available). Real time output control. Double buffer compare register

Timer 8 .....Timer pulse output to large current terminal TM8IOB possible. Event count. High accuracy PWM output (cycle/duty continuous variable). Pulse width measurement. Input capture (both edge available). 32-bit cascade connected (timer 7, 8). 32-bit PWM output. Synchronous output event. Double buffer compare register

Timer 9 .....Timer pulse output to large current terminal TM9IOB possible. 3-phase PWM output. Triangular waveform output. Jigsaw waveform output. Dead time setup. Event count

24H timer: Interval function (Interruption every 0.5 seconds, every 1 second, every 1 minute, every 1 hour and 24 hours). Alarm function

Time base timer: One-minute count setting

Watchdog timer × 2

■ Serial interface

Synchronous type/UART (full-duplex)/LIN × 1: Serial 0

Synchronous type/UART (full-duplex) × 2: Serial 1, 2

Synchronous type/Multi-master I^2C × 1: Serial 4

■ DMA controller

1 systems. Maximum transfer cycles are 255

Starting factor: External request. Internal event. Software

■ I/O Pins

I/O 54 : Common use. Specified pull-up/pull-down resistor available. Input/output selectable (bit unit)

■ A/D converter

10-bit × 12 channels

■ Display control function

LCD: 32 segments × 4 commons (Static, 1/2, 1/3, or 1/4 duty)

Usable if VLC1 ≤ VDD

■ Special Ports

Buzzer output. Inverted buzzer output. High-current drive port

■ Reset

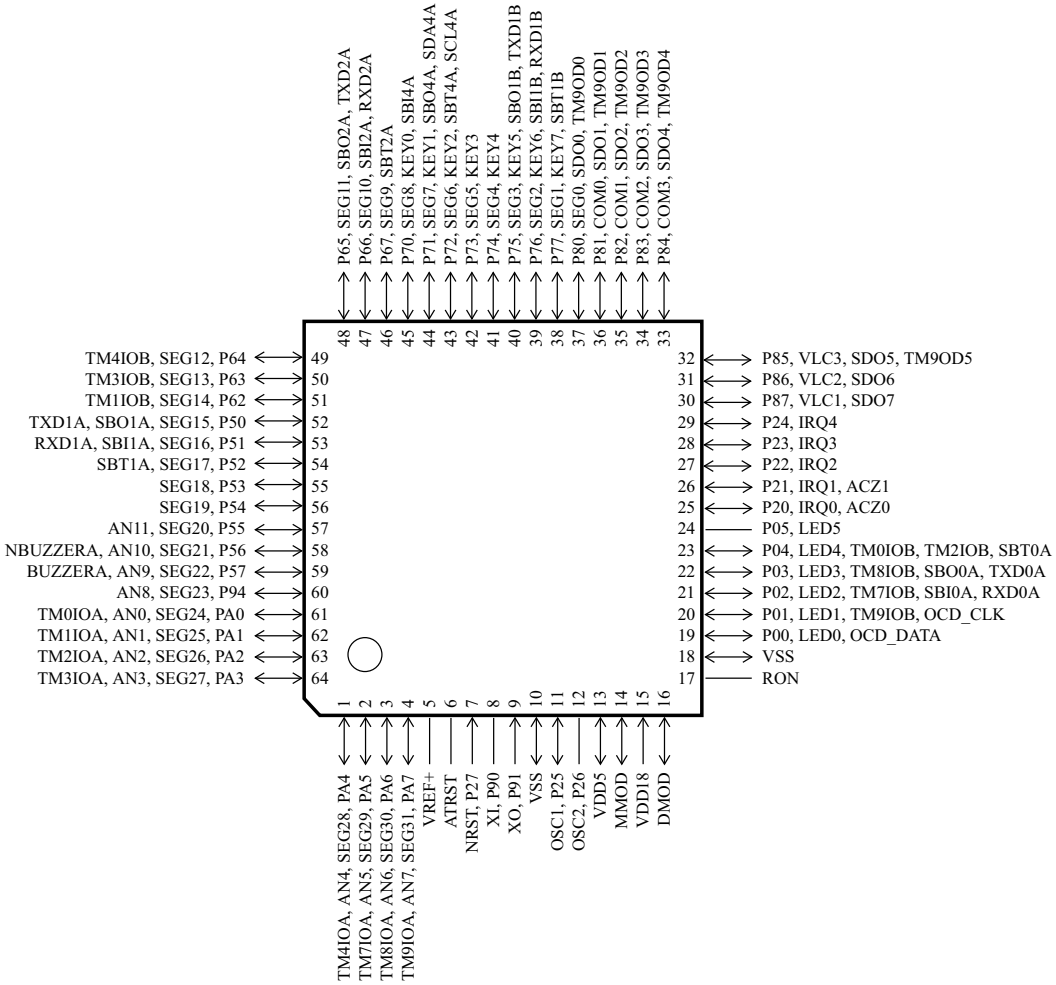
Low voltage detection. Automatic Reset. Reset factor detection

■ Internal oscillation

High speed: 20 MHz/16 MHz. Low speed: 30 kHz

■ Pin Assignment

LQFP064-P-1414, TQFP064-P-1010C



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