

□ MN101CA5 Series

Type	MN101CA5F	MN101CFA5G
Internal ROM type	Mask ROM	FLASH
ROM (byte)	96K	128K
RAM (byte)	4K	10K
Package (Lead-free)	LQFP112-P-2020 (ES (Engineering Sample) available)	
Minimum Instruction Execution Time	0.1 μs (at 4.5 V to 5.5 V, 20 MHz) 0.24 μs (at 2.7 V to 5.5 V, 8.4 MHz) 0.48 μs (at 2.3 V to 5.5 V, 4.19 MHz)* 1.0 μs (at 2.0 V to 5.5 V, 2.0 MHz)* 62.5 μs (at 2.0 V to 5.5 V, 32 kHz)* *: The lower limit for operation guarantee for flash memory built-in type is 2.5 V.	

■ Interrupts

RESET. Watchdog. External 0 to 6. Timer 0 to 4. Timer 6. Timer 7 (2 systems). Timer 8 (2 systems). Time base. Serial 0 (2 systems). Serial 1 (2 systems). Serial 2. Serial 3 (2 systems). A/D conversion finish. Automatic transfer finish. FL display key scan. FL display dimmer

■ Timer Counter

8-bit timer × 6

Timer 0Square-wave/8-bit PWM output. Event count. Remote control carrier output. Simple pulse width measurement
 Timer 1Square-wave output. Event count. Serial transfer clock output
 Timer 2, 4Square-wave/8-bit PWM output. Serial transfer clock output. Event count. Simple pulse width measurement
 Timer 3Square-wave output. Event count. Remote control carrier output. Serial transfer clock output
 Timer 68-bit freerun timer
 Timer 0, 1 can be cascade-connected
 Timer 2, 3 can be cascade-connected

16-bit timer × 2

Timer 7, 8Square-wave output. 16-bit PWM output (cycle/duty continuous variable). Event count. Pulse width measurement.
 Input capture

Time base timer: One-minute count setting

Watchdog timer × 1

■ Serial interface

Synchronous type/UART (full-duplex) × 3: Serial 0, 1, 3

Synchronous type/Single-master I²C × 1: Serial 2

■ DMA controller

Maximum transfer cycles: 255

Starting factor: External request. Various types of interrupt. Software

Transfer mode: 1-byte transfer. Word transfer. Burst transfer

■ I/O Pins

I/O 44 : Common use. Specified pull-up resistor available. Input/output selectable (bit unit)

High Voltage 57 : Output: 26. I/O: 31. P-ch. open drain (breakdown voltage -40 V); FL drive: 57. Specified pull-down resistor mask option: 39

■ A/D converter

8-bit × 8 channels (with S/H)

■ Display control function

FL: (35 to 47) segments × (18 to 10) digits

16 levels dimmer function

Light-and-dark 2-tones display function

Can support automatic display to universal grid display tubes

Output dimmer waveform for FL driver connection (DROUT)

Internal pull down resistor is available between Port 6 and Vpp, Port 9 and Vpp, Port B and Vpp, Port C and Vpp, Port D and Vpp by

Mask option (only for Mask ROM version)

Internal pull down resistor between Port 4 and Vpp, Port 7 and Vpp, Port 8 and Vpp

■ Special Ports

Buzzer output. Remote control carrier output. High-current drive port

■ ROM Correction

Correcting address designation: Up to 3 addresses possible

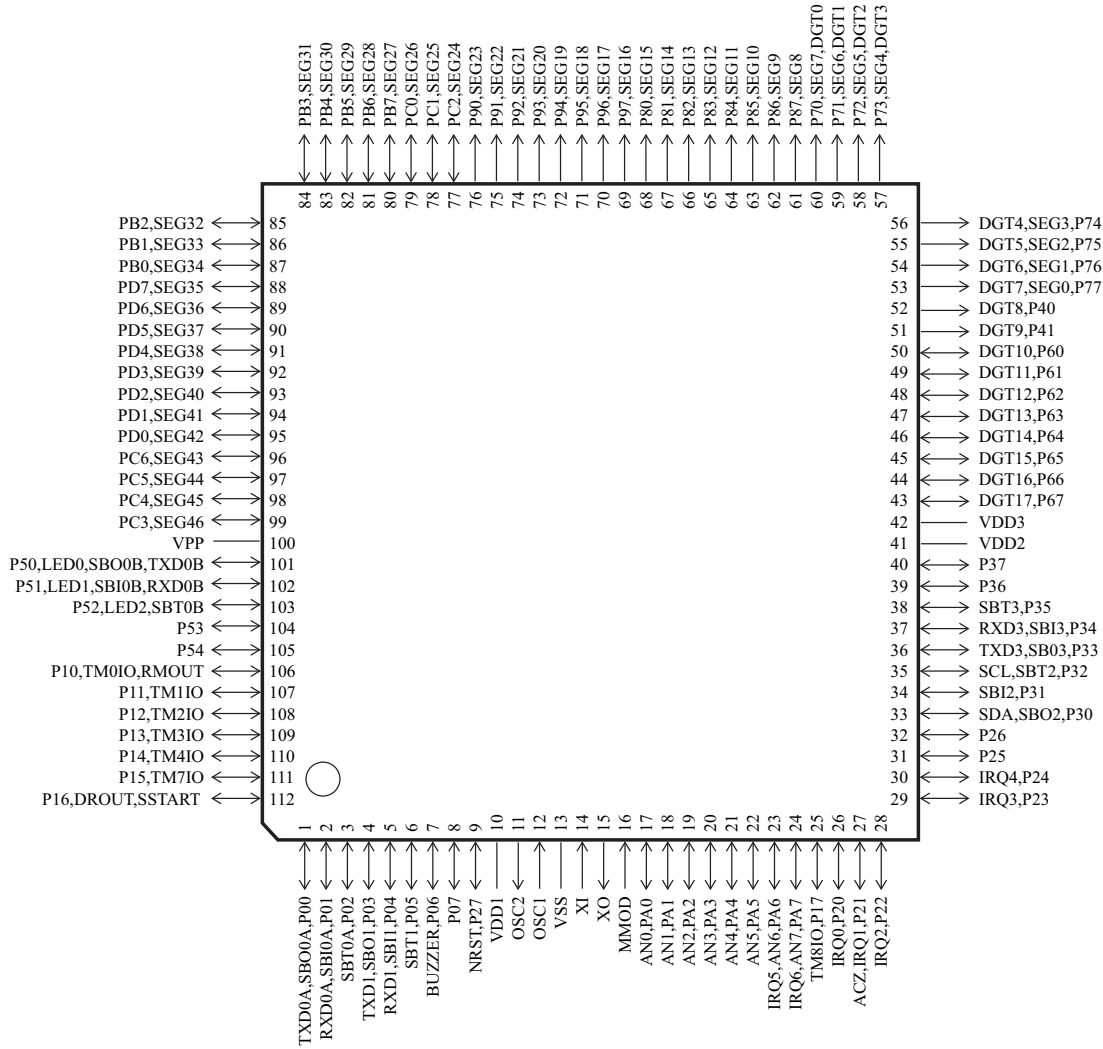
■ Development tools

In-circuit Emulator

PX-ICE101C/D + PX-PRB101CA3-LQFP112-P-2020-M

■ Pin Assignment

LQFP112-P-2020



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