Features

- High-performance, Low-power AVR 8/16-bit XMEGA Microcontroller
- Non-volatile Program and Data Memories
  - 64K/128K/192K/256K Bytes of In-System Self-Programmable Flash
  - 4K/8K/8K/8K Boot Code Section with Independent Lock Bits
  - 2K/2K/4K/4K Bytes EEPROM
  - 4K/8K/16K/16K Bytes Internal SRAM
- Peripheral Features
  - Four-channel DMA Controller with support for external requests
  - Seven 16-bit Timer/Counters
    - 4 Timer/Counters with 4 Output Compare or Input Capture channels
    - 3 Timer/Counters with 2 Output Compare or Input Capture channels
    - High Resolution Extensions on all Timer/Counters
    - Advanced Waveform Extension on 1 Timer/Counters
  - Seven USARTs
    - IrDA Extension on 1 USART
  - AES Crypto Engine
  - DES Crypto Engine
  - Two 2-wire Interfaces (I^2C and SMBus compliant)
  - Four SPIs (Serial Peripheral Interfaces)
  - 16-bit Real Time Counter with Separate Oscillator
  - Two Eight-channel, 12-bit, 2 Msps ADCs
  - One Two-channel, 12-bit, 1 Msps DAC
  - Four Analog Comparators
  - External Interrupts on all General Purpose I/O pins
  - Programmable Watchdog Timer with Separate On-chip Oscillator
- Special Microcontroller Features
  - Power-on Reset and Programmable Brown-out Detection
  - Internal and External Clock Options with PLL
  - Programmable Multi-level Interrupt Controller
  - Sleep Modes: Idle, Power-down, Standby, Power-save, Extended Standby
  - Advanced Programming, Test and Debugging Interfaces
    - JTAG (IEEE 1149.1 Compliant) Interface for test, debug and programming
    - PDI (Program and Debug Interface) for programming, test and debugging
- I/O and Packages
  - 50 Programmable I/O Lines
  - 64-lead TQFP
  - 64-pad MLF
- Operating Voltage
  - 1.8 – 3.6V
- Speed performance
  - 0 – 12 MHz @ 1.8 – 2.7V
  - 0 – 32 MHz @ 2.7 – 3.6V

Typical Applications

- Industrial control
- Factory automation
- Building control
- Board control
- White Goods
- Climate control
- ZigBee
- Motor control
- Networking
- Optical
- Hand-held battery applications
- Power tools
- HVAC
- Metering
- Medical Application

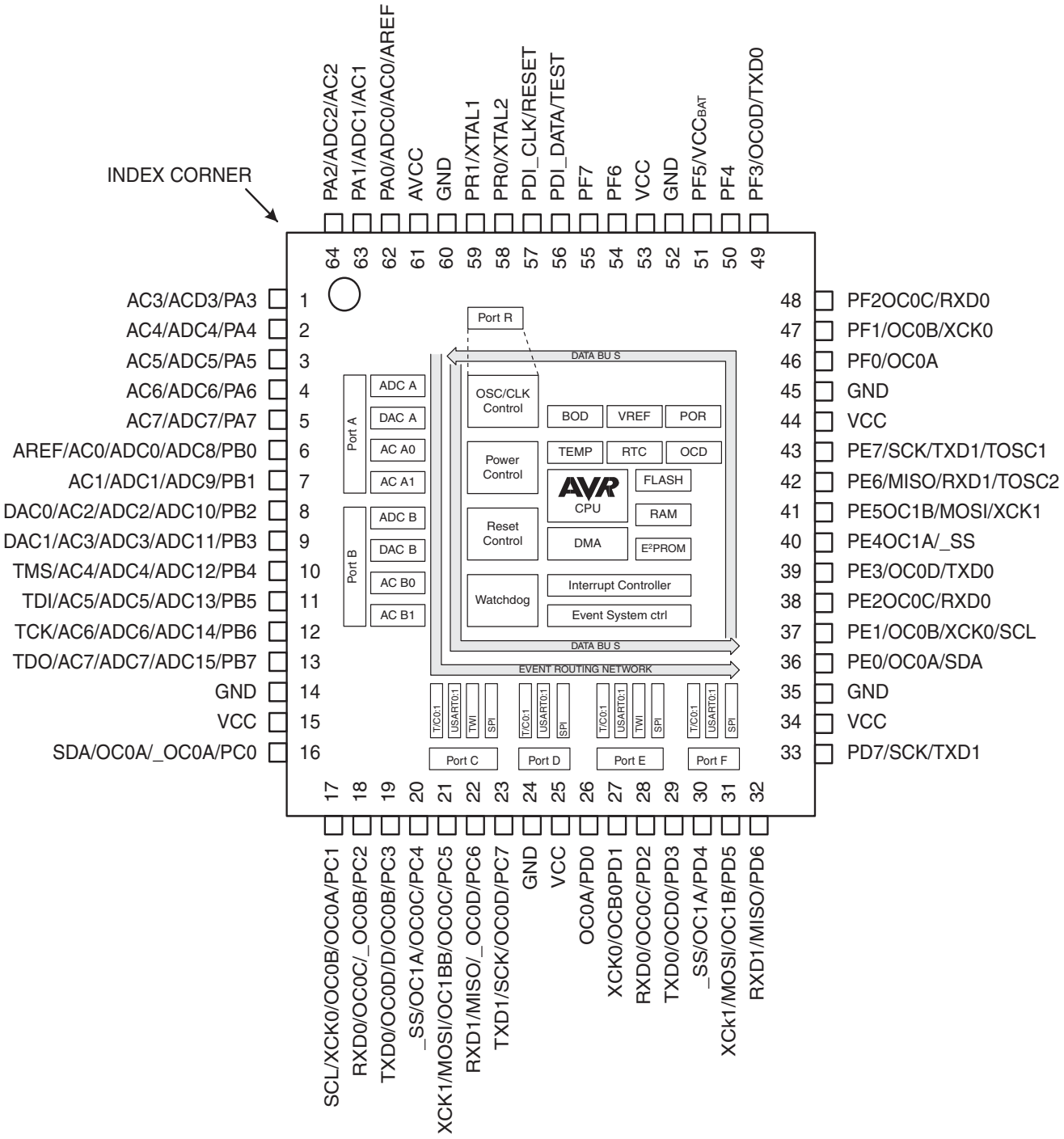
8/16-bit AVR® XMEGA Microcontroller

ATxmega256A3
ATxmega192A3
ATxmega128A3
ATxmega64A3

Advance Information

8068A–AVR–02/08

1. Block Diagram/Pinout



2. Ordering Information

For packaging information, see ”Packaging information” on page 53.

Ordering Code	Flash (B)	E^2 (B)	SRAM (B)	Speed (MHz)	Power Supply	Package[1][2]	Temp
ATxmega256A3-AU	256K + 8K	4K	16K	32	1.8 - 3.6V	64A	-40° - 85°C
ATxmega192A3-AU	192K + 8K	4K	16K	32	1.8 - 3.6V		
ATxmega128A3-AU	128K + 8K	2K	8K	32	1.8 - 3.6V		
ATxmega64A3-AU	64K + 4K	2K	4K	32	1.8 - 3.6V		
ATxmega256A3-MU	256K + 8K	4K	16K	32	1.8 - 3.6V	64M1	
ATxmega192A3-MU	192K + 8K	4K	16K	32	1.8 - 3.6V		
ATxmega128A3-MU	128K + 8K	2K	8K	32	1.8 - 3.6V		
ATxmega64A3-MU	64K + 4K	2K	4K	32	1.8 - 3.6V		

Notes: 1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information.
2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.

Package Type	
64A	64-lead, 14 x 14 mm Body Size, 1.0 mm Body Thickness, 0.8 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)
64M1	64-pad, 9 x 9 x 1.0 mm Body, Lead Pitch 0.50 mm, 5.40 mm Exposed Pad, Micro Lead Frame Package (MLF)

3. Disclaimer

Typical values contained in this datasheet are based on simulations and characterization of other AVR microcontrollers manufactured on the same process technology. Min and Max values will be available after the device is characterized.

4. Overview

The XMEGA A3 is a family of low power, high performance and peripheral rich CMOS 8/16-bit microcontrollers based on the AVR® enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the XMEGA A3 achieves throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.

5. Resources

A comprehensive set of development tools, application notes, and datasheets are available for download on http://www.atmel.com.

5.1 Recommended reading

- **XMEGA A Manual**
- **Application Notes**

This document contains part specific information only. The XMEGA A Manual describes the peripherals in-depth. The application notes contain example code and show applied use of the peripherals.

6. AVR CPU

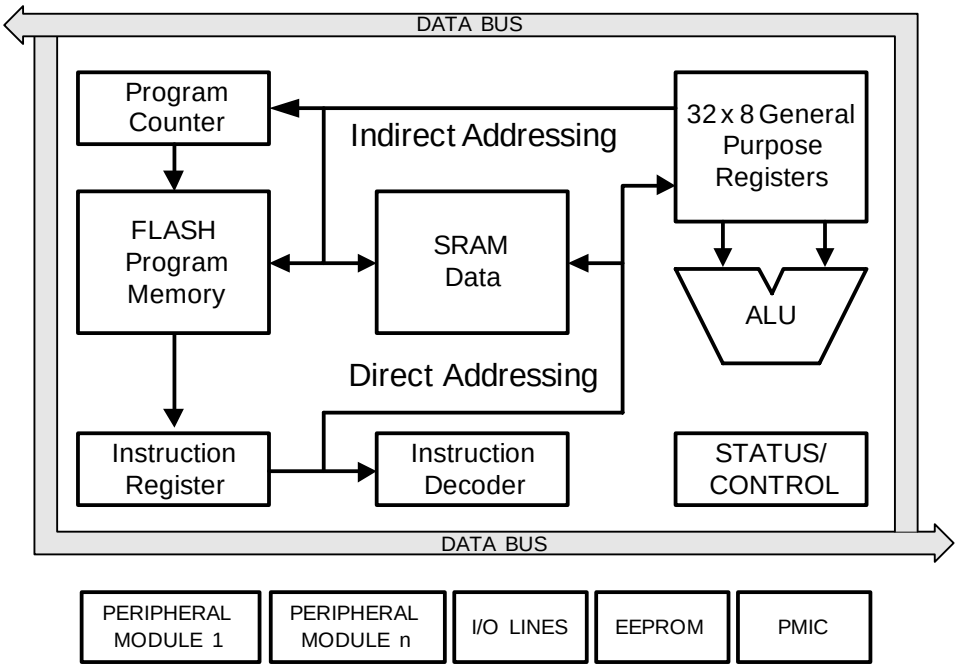
6.1 Features

- **8/16-bit high performance AVR RISC Architecture**
  - **139 instructions**
  - **Hardware multiplier**
- **32x8-bit registers directly connected to the ALU**
- **Stack in RAM**
- **Stack Pointer accessible in I/O memory space**
- **Direct addressing of up to 16M bytes of program and data memory.**
- **True 16/24-bit access to 16/24-bit I/O registers**
- **Support for 8-, 16- and 32-bit Aritmetic's**
- **Configuration Change Protection of system critical features.**

6.2 Overview

The XMEGA A3 uses an 8/16-bit AVR CPU. The main function of the CPU core is to ensure correct program execution. The CPU must therefore be able to access memories, perform calculations and control peripherals. Interrupt handling is described in a separate section. Figure 6-1 on page 5 shows the CPU block diagram.

Figure 6-1. CPU block diagram



The AVR uses a Harvard architecture - with separate memories and buses for program and data. Instructions in the program memory are executed with a single level pipeline. While one instruction is being executed, the next instruction is pre-fetched from the program memory. This concept enables instructions to be executed in every clock cycle. The program memory is In-System Re-programmable Flash memory.

6.3 Register File

The fast-access Register File contains 32 x 8-bit general purpose working registers with a single clock cycle access time. This allows single-cycle Arithmetic Logic Unit (ALU) operation. In a typical ALU operation, two operands are output from the Register File, the operation is executed, and the result is stored back in the Register File - in one clock cycle.

Six of the 32 registers can be used as three 16-bit indirect address register pointers for Data Space addressing - enabling efficient address calculations. One of these address pointers can also be used as an address pointer for look up tables in Flash program memory.

6.4 ALU - Arithmetic Logic Unit

The high performance Arithmetic Logic Unit (ALU) supports arithmetic and logic operations between registers or between a constant and a register. Single register operations can also be executed in the ALU. Within a single clock cycle, arithmetic operations between general purpose registers or between a register and an immediate are executed. After an arithmetic or logic operation, the Status Register is updated to reflect information about the result of the operation.

The ALU operations are divided into three main categories – arithmetic, logical, and bit-functions. Both 8-, 16 and 32-bit arithmetic is supported. The ALU also provide a powerful multiplier supporting both signed/unsigned multiplication and fractional format.

6.5 Program Flow

Program flow is provided by conditional and unconditional jump and call instructions, able to address the whole address space directly. Most AVR instructions use a 16-bit word format. Some instructions also use a 32-bit format.

The Program Flash memory space is divided in two sections, the Boot section and the Application section. Both sections have dedicated Lock bits for write and read/write protection. The Store Program Memory (SPM) instruction used to access the Application section must reside in the Boot section.

A third section exists inside the Application section. This section, the Application Table section, has separate Lock bits for write and read/write protection. The Application Table section can be used for storing non-volatile data or application software.

The Program Counter (PC) addresses the location from where the instructions are fetched. After a reset, the PC is set to location ‘0’.

During interrupts and subroutine calls, the return address PC is stored on the Stack. The Stack is effectively allocated in the general data SRAM, and consequently the Stack size is only limited by the total SRAM size and the usage of the SRAM. The Stack Pointer (SP) is default reset to the highest address of the internal SRAM. The SP is read/write accessible in the I/O space. The data SRAM can easily be accessed through the five different addressing modes supported in the AVR architecture.

7. Memories

7.1 Features

- **Flash Program Memory**
  - **One linear address space**
  - **In-System Reprogrammable**
  - **Self-Programming and Bootloader support**
  - **Application Section for application code**
  - **Application Table Section for application code or data storage**
  - **Bootloader Section for application code or bootloader code**
  - **Separate lock bits and protection for all sections**
- **Data Memory**
  - **One linear address space**
  - **Single cycle access from CPU**
  - **SRAM**
  - **EEPROM**
    - **Byte or page accessible**
    - **Optional memory mapping for direct Load/Store**
  - **I/O Memory**
    - **Configuration and Status register for all peripherals and modules**
    - **16 bit accessible General Purpose Register for global variable or flags**
  - **External Memory**
  - **Bus arbitration**
    - **Safe and deterministic handling of CPU and DMA Controller priority**
  - **Separate buses for SRAM, EEPROM, IO Memory and External Memory access**
    - **Enables simulatiouns bus access for CPU and DMA Controller**

7.2 Overview

The AVR architecture has two main memory spaces, the Program Memory and the Data Memory. In addition, the XMEGA A3 features an EEPROM Memory for non-volatile data storage. All three memory spaces are linear and require no paging. The memory configurations are shown in ”Ordering Information” on page 3.

Non-volatile memory spaces can be locked for further write and read/write operations. This prevents unrestricted access to the application software.

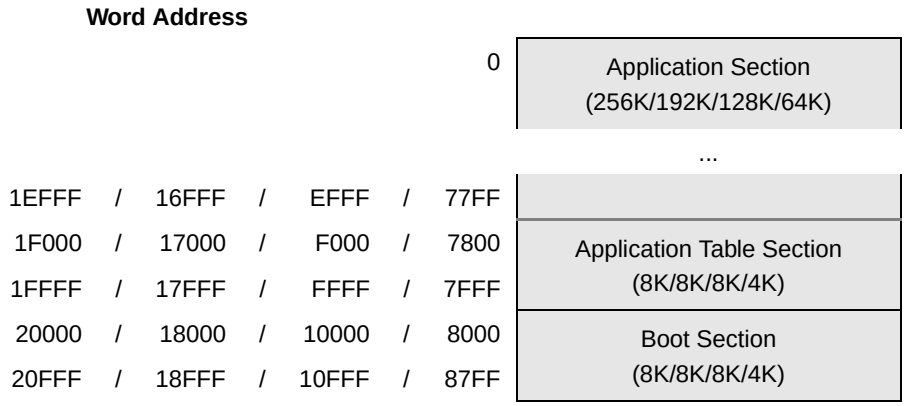
7.3 In-system Programmable Flash Program Memory

The XMEGA A3 contains On-chip In-System Re-programmable Flash memory for program storage, see Table 7-1 on page 8. Since all AVR instructions are 16- or 32-bits wide, each Flash address location is 16 bits.

The XMEGA A3 has additional Boot section for bootloader applications. The Store Program Memory (SPM) instruction used to write to the Flash will only operate from this section. Operation of the SPM is also associated with Boot Lock bits for software protection.

The XMEGA A3 has an Application Table section inside the Application section for storage of Non-volatile data.

Figure 7-1. Flash Program Memory (Hexadecimal address)



The Application Table- and Boot sections can also be used for general application software.

7.4 SRAM Data Memory

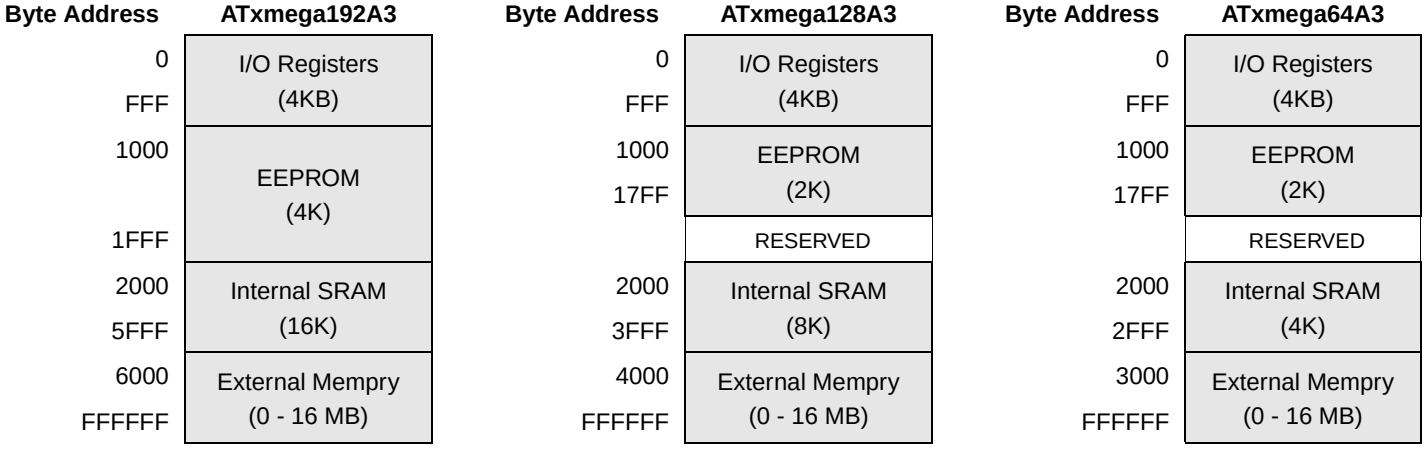
The XMEGA A3 has internal SRAM memory for data storage. The Memory Map for the devices in the family resemble each other, see Table 7-2 on page 8.

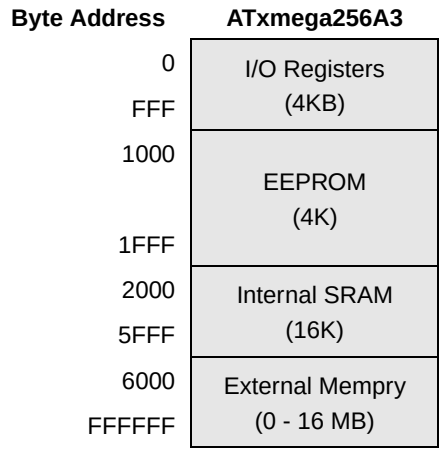
7.5 EEPROM Data Memory

The XMEGA A3 has internal EEPROM memory for non-volatile data storage. It is addressable either in a separate data space or it can be memory mapped the normal data space. The EEPROM memory supports both byte and page access.

The Internal SRAM and EEPROM memory spaces start at the same address in all devices, see Table 7-2 on page 8. The Reserved memory space is empty.

Figure 7-2. Data Memory Map (Hexadecimal address)




Byte Address
ATxmega256A3
0
FFF
1000
1FFF
2000
5FFF
6000
FFFFFF
I/O Registers
(4KB)
EEPROM
(4K)
Internal SRAM
(16K)
External Mempry
(0 - 16 MB)

7.6 I/O Memory

All XMEGA A3 I/Os and peripherals are addressable through I/O memory locations in the data memory space. All I/O locations may be accessed by the LD/LDS/LDD and ST/STS/STD instructions, transferring data between the 32 general purpose registers and the I/O memory.

IN and OUT instructions can address I/O memory locations in the range 0x00 - 0x3F directly.

I/O registers within the address range 0x00 - 0x1F are directly bit-accessible using the SBI and CBI instructions. The value of single bits can be checked by using the SBIS and SBIC instructions in these registers.

The I/O space definition of the XMEGA A3 is shown in ”Peripheral Module Address Map” on page 51.

8. DMA - Direct Memory Access Controller

8.1 Features

- **Allows High-speed data transfer**
  - **From memory to peripheral**
  - **From memory to memory**
  - **From peripheral to memory**
  - **From peripheral to peripheral**
- **4 Channels**
- **From 1 byte and up to 16 M bytes transfers in a single transaction**
- **Multiple addressing modes for source and destination address**
  - **Incremental**
  - **Decremental**
  - **Static**
- **1, 2, 4, or 8 bytes Burst Transfers**
- **Programmable priority between channels**

8.2 Overview

The XMEGA A3 has a Direct Memory Access (DMA) controller to move data between memories and peripherals in the data space. The DMA controller uses the same data bus as the CPU to transfer data.

The XMEGA A3 has 4 DMA channels that may be configured independently. The DMA controller supports transfer of up to 64K data blocks and can be configured to access memory with incrementing, decrementing or static addressing.

Since the DMA can access all the peripherals through the I/O memory, the DMA may be used for automatic transfer of data to/from communication modules, as well as automatic data retrieval from ADC conversions or data transfer to DAC conversions.

The DMA controller can read from memory mapped EEPROM, but it cannot write to the EEPROM or access the Flash.

9. Event System

9.1 Features

- Inter peripheral communication and signalling
- CPU and DMA independent operation
- 8 Event Channels allows for up to 8 signals to be routed at the same time
- Events can be generated by
  - Timer/Counters (TCxn)
  - Real Time Counter (RTC)
  - Analog to Digital Converters (ADCx)
  - Analog Comparators (ACx)
  - Ports (PORTx)
  - System Clock (Clk_{SYS})
  - Software (CPU)
- Events can be used by
  - TImer/Counters (TCxn)
  - Analog to Digital Converters (ADCx)
  - Digital to Analog Converters (DACx)
  - Ports (PORTx)
  - DMA Controller (DMAC)
- Advanced Features
  - Manual Event Generation from software (CPU)
  - Quadrature Decoding
  - Digital Filtering
- Operative in Active and Idle mode

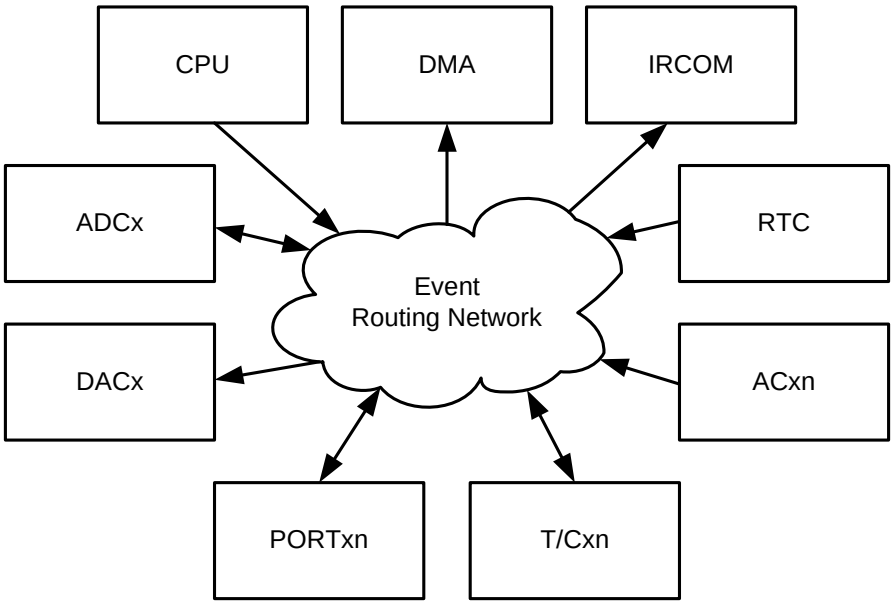
9.2 Overview

The Event System is a set of features for inter peripheral communication. It enables the possibility for a change of state in one peripheral to automatically trigger actions in other peripherals. What change of state in a peripheral that will trigger actions in other peripherals is configurable in software. It is a simple, but powerful system as it allows for autonomous control of peripherals without any use of interrupt, CPU or DMA resources

The indication of a change of state in a peripheral is referred to as an event. The events are passed between peripherals using a dedicated routing network called the Event Routing Network. Figure 9-1 on page 13 shows a basic block diagram of the Event System with the Event Routing Network and the peripherals that are connected. The event system is not a single entity, but a set of features for inter peripheral communication. This highly flexible system can be used for simple rerouting of signals, pin functions or for sequencing of events.

The event system is functional in both Active- and Idle mode.

Figure 9-1. Event system block diagram.



The the event routing network can directly connect together ADCs, DACs, Analog Comparators (AC), I/O ports (PORT), the Real-time Counter (RTC), and Timer/Counters (T/C). Events can also be generated from software (CPU).

10. System Clock and Clock options

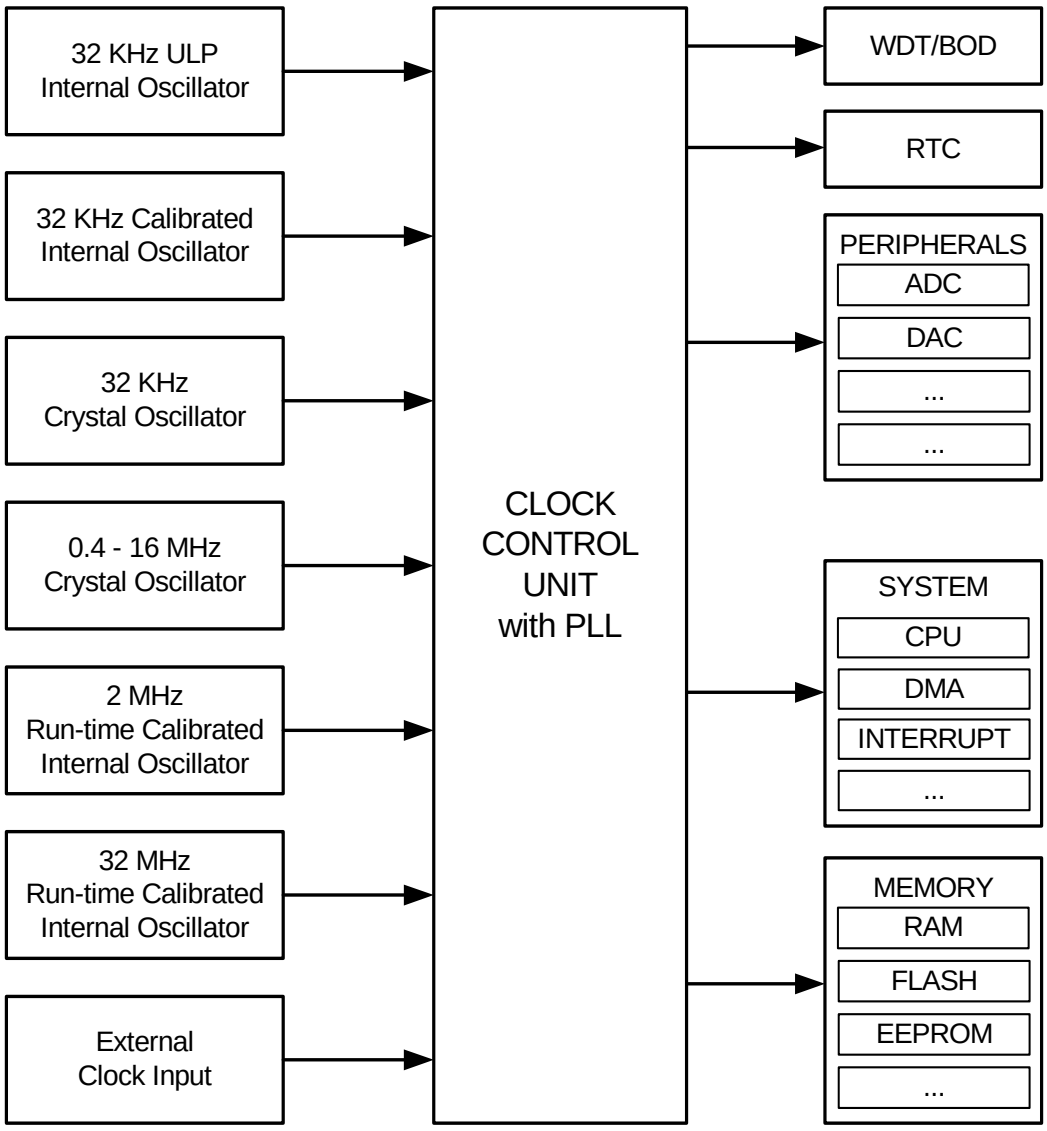
10.1 Features

- **Fast start-up time**
- **Safe run time clock switching**
- **4 Internal Oscillators; 32 MHz, 2 MHz, 32 kHz, 32 kHz Ultra Low Power (ULP)**
- **0.4 - 16 MHz Crystal Oscillator, 32 kHz Crystal Oscillator, external clock**
- **PLL with internal and external clock options and 1 to 31x multiplication**
- **Clock Prescalers with 1 to 2048x division**
- **Fast peripheral clock.**
- **Automatic Run-Time Calibration of internal oscillators**
- **Crystal Oscillator failure detection**

10.2 Overview

XMEGA A3 has an advanced clock system, supporting a large number of clock sources. It incorporates both integrated oscillators, and external crystal oscillators and resonators. A high frequency Phase Locked Loop (PLL) and clock prescalers can be controlled from software to generate a wide range of clock frequencies. The clock distribution also enables the possibility to switch between clock sources from software during run-time. A calibration feature (DFLL) is available, and can be used for automatic run-time calibration of the internal oscillators. A Crystal Oscillator Failure Monitor can be enabled to issue a Non-Maskable Interrupt and switch to internal oscillator if the external oscillator fails. Figure 10-1 on page 15 shows the principal clock system in XMEGA A3.

Figure 10-1. Clock system overview



Each clock source is briefly described in the following sub-sections.

10.3 Clock Options

10.3.1 32 kHz Ultra Low Power Internal Oscillator

The 32 kHz Ultra Low Power (ULP) Internal Oscillator is a very low power consumption clock source based on internal components only. As it is intended mainly for system functions, it should not be used when an accurate clock is required.

10.3.2 32 kHz Calibrated Internal Oscillator

Compared to the internal ULP oscillator, the 32 kHz Calibrated Internal Oscillator is a high accuracy clock source based on internal components only.

10.3.3 32 kHz Crystal Oscillator

The 32 kHz Crystal Oscillator is a low power driver for an external watch crystal.

10.3.4 0.4 - 16 MHz Crystal Oscillator

The 0.4 - 16 MHz Crystal Oscillator is a driver intended both for driving resonators and crystals from 400 kHz to 16 MHz.

10.3.5 2 MHz Run-time Calibrated Internal Oscillator

The 2 MHz Run-time Calibrated Internal Oscillator is a high frequency oscillator based on internal components only. The oscillator can use the 32 kHz Calibrated Internal Oscillator or the 32 kHz Crystal Oscillator to calibrate the frequency run-time to compensate for temperature and voltage drift, optimizing the accuracy of the oscillator.

10.3.6 32 MHz Run-time Calibrated Internal Oscillator

The 32 MHz Run-time Calibrated Internal Oscillator is a high frequency oscillator based on internal components only. The oscillator can use the 32 kHz Calibrated Internal Oscillator or the 32 kHz Crystal Oscillator to calibrate the frequency run-time to compensate for temperature and voltage drift, optimizing the accuracy of the oscillator.

10.3.7 External Clock input

The external clock input gives the possibility to connect to a clock from an external source.

10.3.8 PLL with Multiplication factor 2 - 31x

The PLL provides the possibility of multiplying a frequency with any real number from 2 to 31. In combination with some prescalers, this gives a numerous number of clock frequency options to use.

11. Power Management and Sleep Modes

11.1 Features

- **5 sleep modes**
  - **IDLE**
  - **Power-down**
  - **Power-save**
  - **Standby**
  - **Extended standby**
- **Power Reduction register to disable clock to unused peripheral**

11.2 Overview

The XMEGA A3 provides various sleep modes tailored to reduce power consumption to a minimum. All sleep modes are accessible from Active mode. In Active mode the CPU is executing application code. The application code decides when and what sleep mode to enter.

Various sources can restore the microcontroller from sleep to Active mode. This is called a wake-up.

In addition Power Reduction Registers (PRR) provides a method to stop the clock to individual peripherals from software. When this is done the current state of the peripheral is frozen and there is no power consuption from the peripheral.

11.3 Sleep Modes

11.3.1 Idle Mode

In Idle mode the CPU and Non-Volatile Memory are stopped, but all peripherals including the Interrupt Controller, Event System and DMA Controller are kept running.

Interrupt request from all enabled interrupts will wake the device.

11.3.2 Power-down Mode

In Power-down mode all system clock sources, including the Real Time Counter clock source are stopped. This allows operation of asynchronous modules only. The only interrupts that can wake up the MCU are the Two Wire Interface address match interrupts, and asynchronous port interrupts.

11.3.3 Power-save Mode

Power-save mode is identical to Power-down, with one exception:

If the Real Time Counter (RTC) is enabled, it will keep running during sleep and the device can also wake up from either RTC Overflow or Compare Match interrupt.

11.3.4 Standby Mode

Standby mode is identical to Power-down with the exception that the system clock sources are kept running, while the CPU, Peripheral and RTC clocks are stopped. This reduces the wake-up time when external crystals or resonators are used.

11.3.5 Extended Standby Mode

Extended Standby mode is identical to Power-save mode with the exception that the system clock sources are kept running while the CPU and Peripheral clocks are stopped. This reduces the wake-up time when external crystals or resonators are used.

12. System Control and Reset

12.1 Resetting the AVR

During reset, all I/O Registers are set to their initial values. Application execution starts from the Reset Vector. The instruction placed at the Reset Vector should be a JMP - Absolute Jump - instruction to the reset handling routine. If the application never enables an interrupt source, the Interrupt Vectors are not used. The regular application code can then be placed at these locations. This is also the case if the Reset Vector is in the Application section while the Interrupt Vectors are in the Boot section or vice versa.

The I/O ports of the AVR are immediately tri-stated when a reset source goes active.

The reset functionality is asynchronous, hence no running clock is required to reset the device.

12.2 Reset Sources

The reset source can be determined by the application by readig a reset status register. The XMEGA A3 has the following sources of reset:

- **Power-on Reset**
- **External Reset**
- **Watchdog Reset**
- **Brown-out Reset**
- **JTAG AVR Reset**
- **PDI reset**
- **Software reset**

12.2.1 Power-on Reset

The MCU is reset when the supply voltage VCC is below the Power-on Reset threshold voltage.

12.2.2 External Reset

The MCU is reset when a low level is present on the RESET pin.

12.2.3 Watchdog Reset

The MCU is reset when the Watchdog Timer period expires and the Watchdog Reset is enabled.

12.2.4 Brown-out Reset

The MCU is reset when the supply voltage VCC is below the Brown-out Reset threshold voltage and the Brown-out Detector is enabled.

12.2.5 JTAG AVR Reset

The MCU is reset as long as there is a logic one in the Reset Register, one of the scan chains of the JTAG system. Refer to IEEE 1149.1 (JTAG) Boundary-scan for details.

12.2.6 PDI reset

The MCU may be reset through the Program and Debug Interface (PDI).

12.2.7 Software reset

The MCU may be reset by the CPU writing to a special I/O register.

12.3 WDT - Watchdog Timer

12.3.1 Features

- **11 selectable timeout period, from 8 ms to 8s.**
- **Two operation modes**
  - **Standard mode**
  - **Window mode**
- **Runs from 1 kHz Ultra Low Power clock reference**
- **Configuration lock**

12.3.2 Overview

The XMEGA A3 has a Watchdog Timer (WDT) that will run continuously when turned on. If the Watchdog Timer is not reset within a software configurable time-out period, the microcontroller will reset. To prevent this reset, a Watchdog Reset (WDR) instruction must be run by software to reset the WDT.

The WDT has a Window mode. In this mode the WDR instruction must be run within a specified period called a window. Application software can set the minimum and maximum limits for this window. If the WDR instruction is not run inside the window limits, the microcontroller will be reset.

For maximum safety, the WDT also has an Always-on mode. This mode is enabled by programming a fuse. In Always-on mode, application software can not disable the WDT.

A protection mechanism is used to prevent unwanted enabling, disabling or change of WDT settings.

13. PMIC - Programmable Multi-level Interrupt Controller

13.1 Features

- **Separate interrupt vector for each interrupt**
- **Short, predictable interrupt response time**
- **Programmable Multi-level Interrupt Controller**
  - **3 programmable interrupt levels**
  - **Selectable priority scheme within low level interrupts (round-robin or fixed)**
  - **Non-Maskable Interrupts (NMI)**
- **Interrupt vectors can be moved to the start of the Boot Section**

13.2 Overview

XMEGA A3 has a Programmable Multi-level Interrupt Controller (PMIC). All peripherals can define three different priority levels for interrupts; high, medium or low. Medium level interrupts may interrupt low level interrupt service routines. High level interrupts may interrupt both low- and medium level interrupt service routines. Low level interrupts have an optional round robin scheme to make sure all interrupts are serviced within a certain amount of time.

A Non-Maskable Interrupt (NMI) can detect oscillator failure.

13.3 Interrupt vectors

When an interrupt is serviced, the program counter will jump to the interrupt vector address. The interrupt vector is the sum of the module or peripherals base address and the specific interrupt's offset address. The base addresses for the XMEGA A3 device is shown in Table 13-1. Offset addresses for each interrupt available in the peripheral are described in the manual. For peripherals or modules that have only one interrupt, the interrupt vector is shown in Table 13-1.

Table 13-1. Reset and Interrupt Vectors

Program Address (Base Address)	Source	Interrupt Description
0x000	RESET	
0x002	IVEC_XOSCF_INT_vect	Crystal Oscillator Failure Interrupt vector (NMI)
0x004	IVEC_PORTC_INT_base	Port C Interrupt base
0x008	IVEC_PORTR_INT_base	Port R Interruptbase
0x00C	IVEC_DMAC_INT_base	DMA Controller Interrupt base
0x014	IVEC_RTC_INT_base	Real Time Counter Interrupt base
0x018	IVEC_TWIC_INT_base	Two-Wire Interface on Port C Interrupt base
0x01C	IVEC_TIMERC0_INT_base	Timer/Counter 0 on port C Interrupt base
0x028	IVEC_TIMERC1_INT_base	Timer/Counter 1 on port C Interrupt base
0x030	IVEC_SPIC_INT_vect	SPI C Interrupt vector
0x032	IVEC_USARTC0_INT_base	USART 0 on port C Interrupt base
0x03D	IVEC_USARTC1_INT_base	USART 1 on port C Interrupt base
0x03E	IVEC_AES_INT_vect	AES Interrupt vector
0x040	IVEC_NVM_INT_base	Non-Volatile Memory INT base
0x044	IVEC_PORTB_INT_base	Port B INT base

Table 13-1. Reset and Interrupt Vectors (Continued)

Program Address (Base Address)	Source	Interrupt Description
0x048	IVEC_ACB_INT_base	Analog Comparator Port B INT base
0x04E	IVEC_ADCB_INT_base	Analog to Digital Converter Port B INT base
0x056	IVEC_PORTE_INT_base	Port E INT base
0x05A	IVEC_TWIE_INT_base	Two-Wire Interface on Port E INT base
0x05E	IVEC_TIMERE0_INT_base	Timer/Counter 0 on port E Interrupt base
0x06A	IVEC_TIMERE1_INT_base	Timer/Counter 1 on port E Interrupt base
0x072	IVEC_SPIE_INT_vect	SPI E Interrupt vector
0x074	IVEC_USARTE0_INT_base	USART 0 on port E Interrupt base
0x07A	IVEC_USARTE1_INT_base	USART 1 on port E Interrupt base
0x080	IVEC_PORTD_INT_base	Port D INT base
0x084	IVEC_PORTA_INT_base	Port A INT base
0x088	IVEC_ACA_INT_base	Analog Comparator Port A INT base
0x08E	IVEC_ADCA_INT_base	Analog to Digital Converter Port A INT base
0x096	IVEC_TWID_INT_base	Two-Wire Interface on Port D INT base
0x09A	IVEC_TIMERD0_INT_base	Timer/Counter 0 on port D Interrupt base
0x0A6	IVEC_TIMERD1_INT_base	Timer/Counter 1 on port D Interrupt base
0x0AE	IVEC_SPID_INT_vector	SPI D Interrupt vector
0x0B0	IVEC_USARTD0_INT_base	USART 0 on port D Interrupt base
0x0B6	IVEC_USARTD1_INT_base	USART 1 on port D Interrupt base
0x0D0	IVEC_PORTF_INT_base	Port F INT base
0x0D4	IVEC_TWIF_INT_base	Two-Wire Interface on Port F INT base
0x0D8	IVEC_TIMERF0_INT_base	Timer/Counter 0 on port F Interrupt base
0x0E4	IVEC_TIMERF1_INT_base	Timer/Counter 1 on port F Interrupt base
0x0EC	IVEC_SPIF_INT_vector	SPI F Interrupt base
0x0EE	IVEC_USARTF0_INT_base	USART 0 on port F Interrupt base
0x0F4	IVEC_USARTF1_INT_base	USART 1 on port F Interrupt base

14. I/O Ports

14.1 Features

- **Selectable input and output configuration for each pin individually**
- **Flexible pin configuration through dedicated Pin Configuration Register**
- **Synchronous and/or asynchronous input sensing with port interrupts and events**
  - **Sense both edges**
  - **Sense rising edges**
  - **Sense falling edges**
  - **Sense low level**
- **Asynchronous wake-up signalling**
- **Highly configurable output driver and pull settings:**
  - **Totem-pole**
  - **Pull-up/-down**
  - **Wired-AND**
  - **Wired-OR**
  - **Bus keeper**
  - **Inverted I/O**
- **Slew rate control**
- **Flexible pin masking**
- **Configuration of multiple pins in a single operation**
- **Read-Modify-Write (RMW) support**
- **Toggle/clear/set registers for OUT and DIR registers**
- **Clock output on port pin**
- **Event Channel 7 output on port pin**
- **Mapping of port registers (virtual ports) into bit accessible I/O memory space**

14.2 Overview

The XMEGA A3 has flexible General Purpose I/O (GPIO) Ports. A port consists of up to 8 pins, ranging from pin 0 to pin 7. The ports implement several functions, including interrupts, synchronous/asynchronous input sensing and configurable output settings. All functions are individual per pin, but several pins may be configured in a single operation.

14.3 I/O configuration

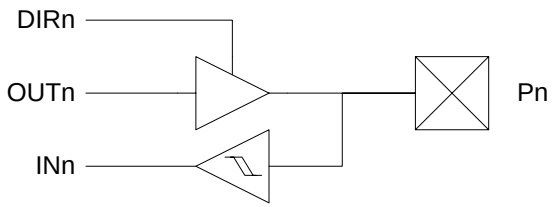
All port pins have programmable output configuration. In addition, all GPIO pins have inverted I/O. For an input, this means inverting the signal between the port pin and the pin register. For an output, this means inverting the output signal between the port register and the port pin. Some port pins also have configurable slew rate limitation to reduce electromagnetic emission.

The configuration options include:

- **Push-pull**
- **Pull-down resistor**
- **Pull-up resistor**
- **Bus keeper**
- **Inverted I/O**
- **Slew rate limitation**

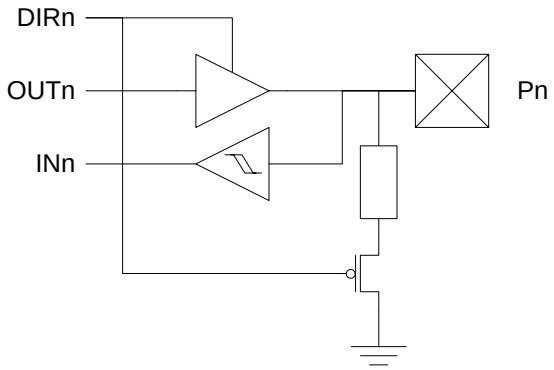
14.4 Push-pull

Figure 14-1. I/O configuration - Totem-pole



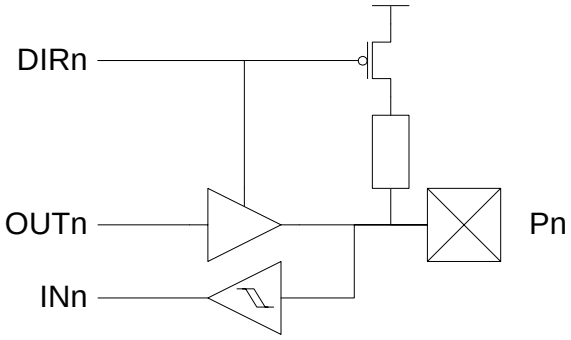
14.5 Pull-down

Figure 14-2. I/O configuration - Totem-pole with pull-down (on input)



14.6 Pull-up

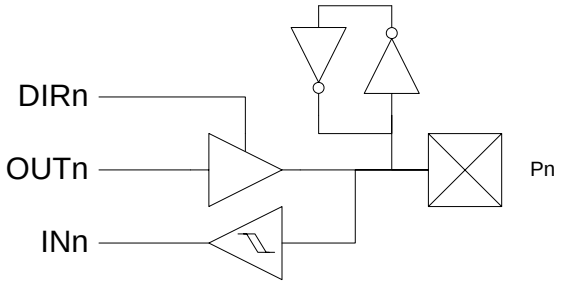
Figure 14-3. I/O configuration - Totem-pole with pull-up (on input)



14.7 Bus-keeper

The bus-keeper's weak output produces the same logical level as the last output level. It acts as a pull-up if the last level was '1', and pull-down if the last level was '0'.

Figure 14-4. I/O configuration - Totem-pole with bus-keeper



14.8 Others

Figure 14-5. Output configuration - Wired-OR with optional pull-down

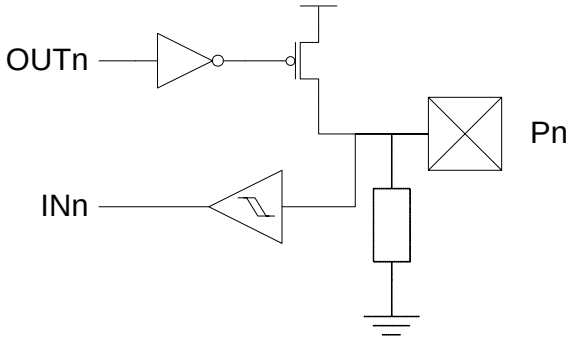
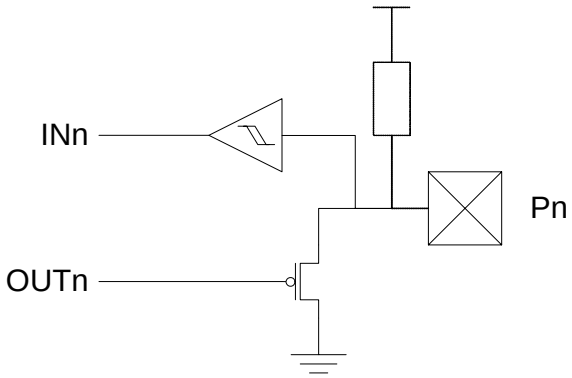


Figure 14-6. I/O configuration - Wired-AND with optional pull-up



14.9 Port Interrupt

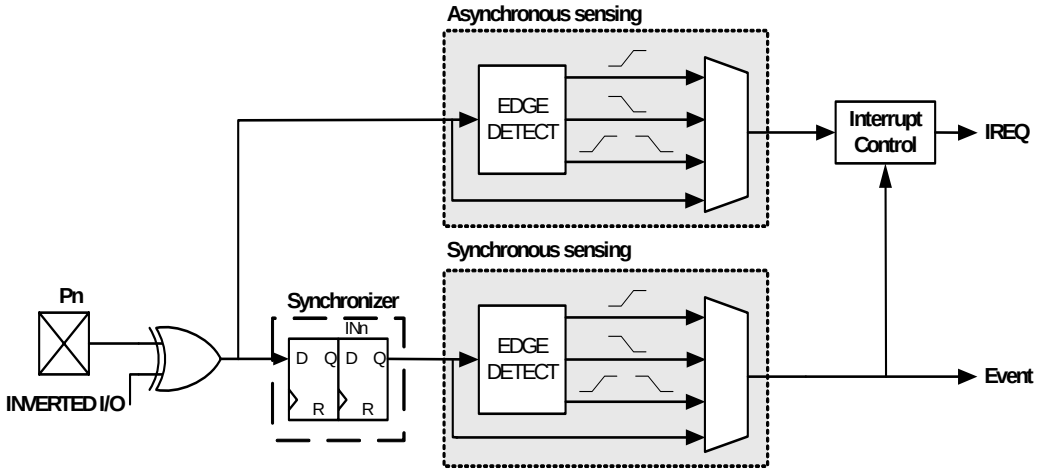
Ports can have pin-change interrupts and external interrupts. Each port supports being the source of two interrupts, and each pin may be configured individually or grouped. Each of the interrupts may be given a specific priority and given specific sense configuration.

14.10 Input sensing

- **Sense both edges**
- **Sense rising edges**
- **Sense falling edges**
- **Sense low level**

The basic input sensing may be synchronous or asynchronous and is built on the configuration shown in Figure 14-7 on page 26.

Figure 14-7. Input sensing system overview



In addition, all GPIO pins may be configured as inverted I/O, meaning that the pin value is inverted before sensing.

15. T/C - 16-bits Timer/Counter with PWM

15.1 Features

- 4 Timer/Counter 0 (Timer0)
- 4 Timer/Counter 1 (Timer1)
- Double Buffered Timer Period Setting
- Compare or Capture Channels are Double Buffered
- 4 Combined Compare or Capture (CC) Channels in Timer0
- 2 Combined Compare or Capture (CC) Channels in Timer1
- Waveform Generation:
  - Single Slope Pulse Width Modulation
  - Dual Slope Pulse Width Modulation
  - Frequency Generation
- Input Capture:
  - Input Capture with Noise Cancelling
  - Frequency capture
  - Pulse width capture
  - 32-bit input capture
- Event Counter with Direction Control
- Timer Overflow and Timer Error Interrupts and Events
- One Compare Match or Capture Interrupt and Event per CC Channel
- Supports DMA Operation
- Hi-Resolution Extension (Hi-Res)
- Advanced Waveform Extension (AWEX)

15.2 Overview

XMEGA A3 has 8 Timer/Counters. 4 are of type Timer0 and 4 of type Timer1. The difference between Timer0 and Timer1 type is that Timer0 has 4 Compare/Capture channels, and Timer1 only has 2. In addition, Timer0 may have an Advanced Waveform Extension (AWEX), that is not available in Timer1.

The Timer/Counters (T/C) are 16-bit wide and can count any clock, event or input signal in the microcontroller. A programmable prescaler is available to get a useful T/C resolution. Updates of Timer and Compare registers are double buffered to ensure glitch free operation. Using Compare channels many different waveforms can be generated, single slope PWM, dual slope PWM and frequency generation.

The High-Resolution Extension can be enabled to increase the waveform generation resolution by 2 bits (4x). This is available for all Timer/Counters.

The Input Capture has a noise canceller to avoid incorrect capture of the T/C. Any input pin or event in the microcontroller can be used to trigger the capture.

A wide range of interrupt or event sources are available, including T/C overflow, Compare match and Capture for each timer and CC channel.

PORTC, PORTD, PORTE and PORTF each has one Timer/Counter 0 and one Timer/Counter 1. Notation of these timers are TCC0, TimerC1, TCD0, TCD1, TCE0, TCE1, TCF0, and TCF1.

16. AWEX - Advanced Waveform Extension

16.1 Features

- **4-DTI Units (8-pin)**
- **8-bit Resolution**
- **Separate High and Low Side Dead-Time Setting**
- **Double Buffered Dead-Time**
- **Fault Protection (Event Controlled)**
- **Single Channel Multiple Output Operation (for BLDC control)**
- **Double Buffered Pattern Generation**

16.2 Overview

The Advanced Waveform Extention (AWEX) provides extra features to the Time/Counter in Waveform Generation (WG) modes. AWEX enables easy and robust implementation of for example advanced motor control (AC, BLDC, SR, and Stepper) and power control applications.

Any WG output from the Timer/Counter 0 are split into a complimentary pair of outputs when any AWEX feature is enabled. These output pairs go through a Dead-Time Insertion (DTI) unit that enables generation of the non-inverted Low Side (LS) and inverted High Side (HS) of the WG output with dead time insertion between LS and HS switching. The DTI output will override the normal port value according to the port override setting. Optionally the final output can be inverted by using inverted I/O (INVEN) bit setting for port pin (Pxn).

The Pattern Generation unit can be used to generate a synchronized bit pattern on the port it is connected to. In addition, the waveform generator output from the Compare Channel A can be distributed to and override all the port pins. When the Pattern generator unit is enabled the DTI unit i bypassed.

The Fault Protection unit is connected to the Event System, enabling any event to trigger a fault condition that will disable the AWEX output.

The AWEX is only available on TCC0 and TCE0. The notation of these are AWEXC and AWEXE.

17. RTC - Real-Time Counter

17.1 Features

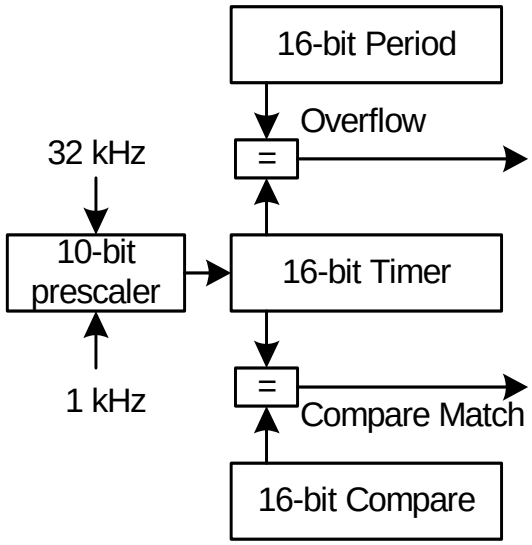
- **16-bit Timer**
- **Flexible Tick resolution ranging from 1 Hz to 32 kHz**
- **1 Compare register**
- **1 Top Value register**
- **Clear timer on Overflow or Compare Match**
- **Overflow or Compare Match event and interrupt generation**

17.2 Overview

The XMEGA A3 includes a 16-bit Real-time Counter (RTC). The RTC can be clocked from a accurate 32.768 kHz Crystal Oscillator, the 32 kHz Calibrated Internal Oscillator, or from the 32 kHz Ultra Low Power Internal Oscillator. The RTC include both a Period and Compare register, for details, see Figure 17-1.

A wide range of Resolution and Time-out periods can be configured using the RTC. With a maximum resolution of 30.5 µs, time-out periods range up to 2000 seconds. With a resolution of 1 second, maximum time-out period is over 18 hours (65536 seconds).

Figure 17-1. Real-time Counter overview



18. TWI - Two Wire Interface

18.1 Features

- **Two Identical TWI peripherals**
- **Simple yet Powerful and Flexible Communication Interface**
- **Both Master and Slave Operation Supported**
- **Device can Operate as Transmitter or Receiver**
- **7-bit Address Space Allows up to 128 Different Slave Addresses**
- **Multi-master Arbitration Support**
- **Up to 400 kHz Data Transfer Speed**
- **Slew-rate Limited Output Drivers**
- **Noise Suppression Circuitry Rejects Spikes on Bus Lines**
- **Fully Programmable Slave Address with General Call Support**
- **Address Recognition Causes Wake-up when in Sleep Mode**
- **I^2C and System Management Bus (SMBus) compliant**

18.2 Overview

The 2-wire Serial Interface (TWI) is a bi-directional bus with only two lines, the clock (SCL) and the data (SDA). The protocol makes it possible to interconnect up to 128 individually addressable devices. Since it is a multi-master bus, one or more devices capable of taking control of the bus, can be connected.

The only external hardware needed to implement the bus is a single pull-up resistor for each of the TWI bus lines. Mechanisms for resolving bus contention are inherent in the TWI protocol.

PORTC and PORTE each have one TWI. Notation of these peripherals are TWIC and TWIE.

19. SPI - Serial Peripheral Interface

19.1 Features

- **4 Identical SPI peripherals**
- **Full-duplex, Three-wire Synchronous Data Transfer**
- **Master or Slave Operation**
- **LSB First or MSB First Data Transfer**
- **Seven Programmable Bit Rates**
- **End of Transmission Interrupt Flag**
- **Write Collision Flag Protection**
- **Wake-up from Idle Mode**
- **Double Speed (CK/2) Master SPI Mode**

19.2 Overview

The Serial Peripheral Interface (SPI) allows high-speed synchronous data transfer between different devices. Devices can communicate using a master-slave scheme, and data are transferred both to and from the devices simultaneously.

PORTC, PORTD, PORTE, and PORTF each have one SPI. Notation of these peripherals are SPIC, SPID, SPIE, and SPIF.

20. USART

20.1 Features

- 8 Identical USART peripherals
- Full Duplex Operation (Independent Serial Receive and Transmit Registers)
- Asynchronous or Synchronous Operation
- Master or Slave Clocked Synchronous Operation
- High-resolution Arithmetic Baud Rate Generator
- Supports Serial Frames with 5, 6, 7, 8, or 9 Data Bits and 1 or 2 Stop Bits
- Odd or Even Parity Generation and Parity Check Supported by Hardware
- Data OverRun Detection
- Framing Error Detection
- Noise Filtering Includes False Start Bit Detection and Digital Low Pass Filter
- Three Separate Interrupts on TX Complete, TX Data Register Empty and RX Complete
- Multi-processor Communication Mode
- Double Speed Asynchronous Communication Mode
- IrDA

20.2 Overview

The Universal Synchronous and Asynchronous serial Receiver and Transmitter (USART) provides highly flexible serial communication device. The frame format can be customized to support a wide range of standards, and the USART implements different error detection.

PORTC, PORTD, PORTE, and PORTF each have two USARTs. Notation of these peripherals are USARTC0, USARTC1, USARTD0, USARTD1, USARTE0, USARTE1, USARTF0, USARTF1.

21. IRCOM - IR Communication Module

21.1 Features

- **Pulse modulation/demodulation for infrared communication**
- **IrDA 1.4 Compatible for baud rates up to 115.2 kbps**
- **Selectable pulse modulation scheme**
  - **3/16 of baud rate period**
  - **Fixed pulse period, 8-bit programmable**
  - **Pulse modulation disabled**
- **Built in filtering**
- **Can be connected to and used by any USART and one USART at the time**

21.2 Overview

XMEGA contains an Infrared Communication Module (IRCOM) IrDA 1.4 compatible module for baud rates up to 115.2 kbps. This supports three modulation schemes: 3/16 of baud rate period, fixed programmable pulse time based on the Peripheral Clock speed, or pulse modulation disabled. There is one IRCOM available, and this can be connected to any USART to enable infrared pulse coding/decoding for that USART.

22. Crypto Engine

22.1 Features

- **Data Encryption Standard (DES) core instruction**
- **Advanced Encryption Standard (AES) crypto module**
- **DES Instruction**
  - **Encryption and Decryption**
  - **DES and triple-DES supported**
  - **Single-cycle DES instruction**
  - **Encryption/Decryption in 16 clock cycles per 8-byte block**
- **AES Crypto Module**
  - **Encryption and Decryption**
  - **Support 128-bit keys**
  - **Support XOR data load mode to the State memory**
  - **Encryption/Decryption in 375 clock cycles per 16-byte block**

22.2 Overview

The Advanced Encryption Standard (AES) and Data Encryption Standard (DES) are two commonly used standards for encryption. These are supported through an AES peripheral module and a DES core instruction.

DES is supported by a DES instruction in the AVR XMEGA CPU. The 8-byte key and 8-byte data blocks must be loaded into the Register file, and then DES must be executed 16 times to encrypt/decrypt the data block.

The AES Crypto Module encrypts and decrypts 128-bit data blocks with the use of a 128-bit key. The key and data must be loaded into the module before encryption/decryption is started. It takes 375 peripheral clock cycles before encrypted/decrypted data can be read out.

23. ADC - 12-bit Analog to Digital Converter

23.1 Features

- **Two ADCs with 12-bit resolution**
- **2 Msps conversion rate**
- **Signed- and Unsigned conversions**
- **4 result registers with individual channel control for each ADC**
- **16 single ended inputs**
- **16x8 differential inputs**
- **Gain of 1, 2, 4, 8, 16, 32 or 64**
- **Selectable accuracy of 8-, 10- or 12-bit.**
- **Built-in Auto Calibration**
- **Internal- or External Reference**
- **Event triggered conversion for accurate timing**
- **DMA transfer of conversion results**
- **Interrupt/Event on compare result**

23.2 Overview

The XMEGA A3 devices has two Analog to Digital Converters (ADC), see Figure 23-1 on page 36. The two ADCs modules can be operated simultaneously, individually or synchronized.

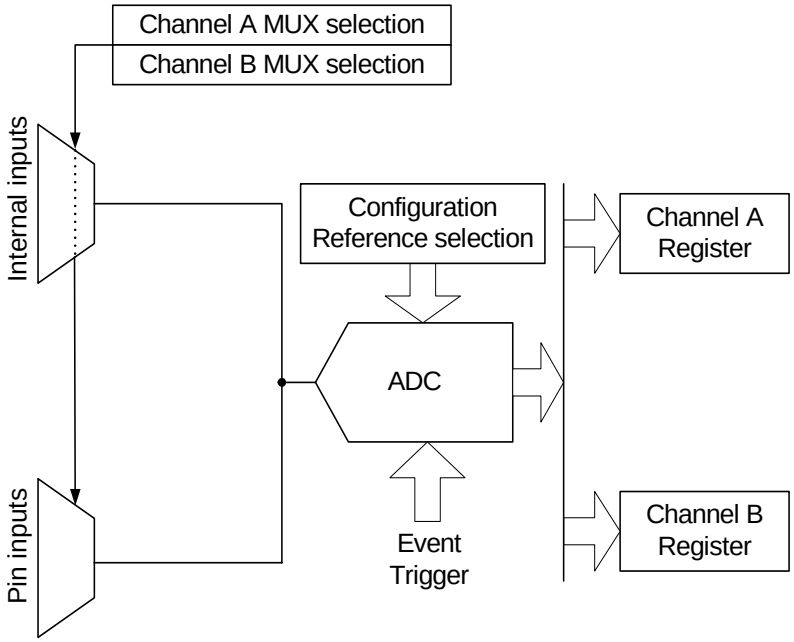
The ADC converts analog voltages to digital values.The ADC has 12-bit resolution and is capable of converting up to 2 million samples per second. The input selection is flexible, and both single-ended and differential measurements can be done. The ADC provides both signed and unsigned results, and an optional gain stage is available to increase the dynamic range of the ADC.

The ADC uses Successive Approximation Result (SAR) ADC. A SAR ADC measures one bit of the conversion result a time. The ADC has a pipeline architecture. This means that a new analog voltage can be sampled and a new ADC measurement started while other ADC measurements are ongoing.

ADC measurements can either be started by the application software or an incoming event from another peripheral in the device. Four different result registers with individual channel selection (MUX registers) are provided to make it easier for the application to keep track of the data. It is also possible to use DMA to move ADC results directly to memory or peripherals.

Both internal and external analog reference voltages can be used. A very accurate internal 1.0V reference is available, providing a conversion range from 0 - 1.0 V in unsigned mode and -1.0 to 1.0V in signed mode.

Figure 23-1. ADC overview



Each ADC has 4 registers defining a MUX selection with a corresponding result register. This means that 4 channels may be sampled within 1.5 µs without any intervention by the application other than starting the conversion, and the result will be available in 4 data registers.

The ADC may be configured to make 8-, or 12-bit results, reducing the conversion time (propagation delay) from 4µs for 12-bit to 3µs for 8-bit resolution.

ADC conversion results are provided left- or right adjusted with optional ‘1’ or ‘0’ padding. This eases calculation when the result is represented as a signed integer (signed 16-bit number).

PORTA and PORTB each have one ADC. Notation of these peripherals are ADCA and ADCB.

24. DAC - 12-bit Digital to Analog Converter

24.1 Features

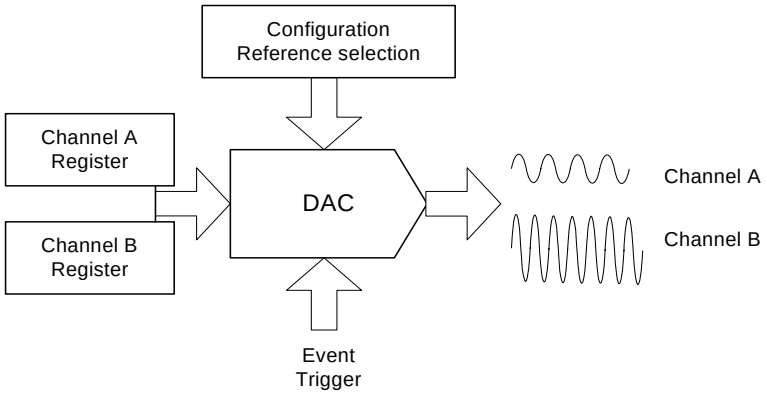
- **One DAC with 12-bit resolution**
- **Up to 1 Msps conversion rate**
- **Flexible conversion range**
- **Multiple trigger sources**
- **1 continuous time or 2 Sample and Hold (S/H) outputs for each DAC**
- **Built-in offset and gain calibration**
- **High drive capabilities**
- **DAC Power reduction mode**

24.2 Overview

The XMEGA A3 features one 12-bit, 1 Msps DAC with built-in calibration of offset and gain, see Figure 24-1 on page 37.

A DAC converts a digital value into an analog signal. The DAC may use the bandgap reference voltage as upper limit for conversion, but it is also possible to use the supply voltage or any applied voltage in-between. An external reference input is shared with the ADC reference input.

Figure 24-1. DAC overview



Each DAC has one continuous output with high drive capabilities for both resistive and capacitive loads. It is also possible to split the continuous time channel into two Sample and Hold (S/H) channels; each with separate data conversion registers.

A DAC conversion may be started from the application software by writing the data conversion registers. The DAC may also be configured to do conversions triggered by the Event System to have regular timing independent of the application. DMA may be used for transferring data from memory location to DAC data registers.

A DAC power reduction mode can be enabled to reduce power consumption.

The DAC has a built-in calibration system that removes offset and gain error.

PORTB have one DAC and the notation of this is DACB.

25. AC - Analog Comparator

25.1 Features

- **Four Analog Comparators**
- **Selectable Power vs. Speed**
  - **20 µA/500 ns active current consumption/propagation delay, or**
  - **130 µA/30 ns active current consumption/propagation delay**
- **Selectable hysteresis**
  - **0, 20 mV, 50 mV**
- **Analog Comparator output available on pin**
- **Flexible Input Selection**
- **Basic interrupt and event generation on**
  - **Rising edge**
  - **Falling edge**
  - **Toggle**
- **Window function interrupt and event generation on**
  - **Signal above window**
  - **Signal inside window**
  - **Signal below window**

25.2 Overview

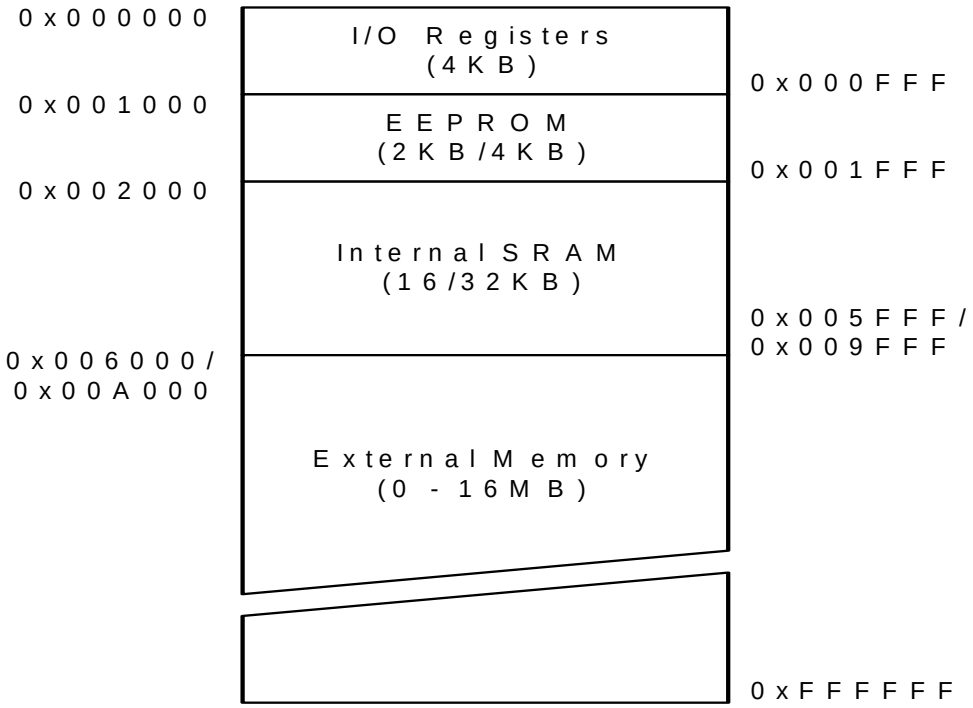
The XMEGA A3 features four Analog Comparators (AC). An Analog Comparator compares two voltages, and the output indicates which input is largest. The Analog Comparator may be configured to give interrupt requests and/or events upon several different combinations of input change.

Both hysteresis and propagation delays may be adjusted in order to find the optimal operation for each application.

The Analog Comparators are always grouped in pairs (AC0 and AC1) on each analog port. They have identical behavior but separate control registers

PORTA and PORTB each have one AC. Notations are ACA0, ACA1, ACB0, and ACB1.

Figure 25-1. Analog comparator overview



25.3 Input Selection

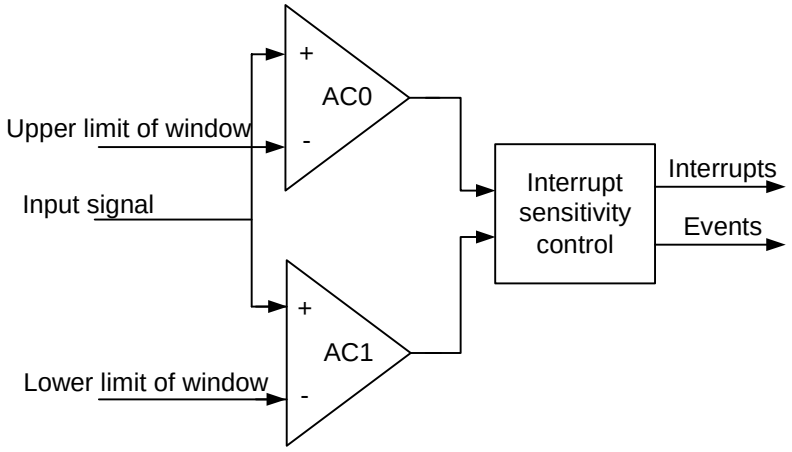
The Analog comparators have a very flexible input selection and the two comparators grouped in a pair may be used to realize a window function. One pair of analog comparators is shown in Figure 25-1 on page 39.

- **Input selection from pin**
  - **Pin 0, 1, 2, 4, 6 selectable to positive input of analog comparator**
  - **Pin 0, 1, 3, 5, 7 selectable to negative input of analog comparator**
- **Internal signals available on both analog comparator inputs**
  - **Bandgap Reference voltage**
  - **Output from 12-bit DAC**
- **6-bit scale down of VCC, available on both analog comparator inputs**

25.4 Window Function

The window function is realized by connecting the inputs of the two analog comparators in a pair as shown in Figure 25-2.

Figure 25-2. Analog comparator window function



26. OCD - On-chip Debug

26.1 Features

- **Complete Program Flow Control**
  - **Symbolic Debugging Support in Hardware**
  - **Go, Stop, Reset, Step into, Step over, Step out, Run-to-Cursor**
- **1 dedicated program address breakpoint or symbolic breakpoint for AVR studio/emulator**
- **4 Hardware Breakpoints**
- **Unlimited Number of User Program Breakpoints**
- **Uses CPU for Accessing I/O, Data, and Program**
- **Non-Intrusive Operation**
  - **Uses no hardware or software resources**
- **High Speed Operation**
  - **No limitation on frequency of TCK versus system clock frequency**

26.2 Overview

The XMEGA A3 has an On-chip debug (OCD) system that - in combination with Atmel's development tools - provides all the necessary functions to debug an application.

27. Program, Debug and Test Interfaces

27.1 Features

- **JTAG Interface (IEEE std. 1149.1 compliant)**
- **PDI - Program and Debug Interface (Atmel proprietary 2-pin interface)**
- **Boundary-scan capabilities according to the IEEE Std. 1149.1 (JTAG)**
- **Access to the OCD system**
- **Programming of Flash, EEPROM, Fuses and Lock Bits**

27.2 Overview

The JTAG and PDI are the physical interface to access the programming and debug facilities. The PDI uses one dedicated pin together with the Reset pin, no general purpose pins are used. When JTAG is used it makes use of four general purpose pins.

27.3 JTAG interface

The JTAG physical layer handles the basic low-level serial communication over four I/O lines named TMS, TCK, TDI, and TDO. It complies to the IEEE Std. 1149.1 for test access port and boundary scan.

27.4 PDI - Program and Debug Interface

The PDI is an Atmel proprietary protocol for communication between the microcontroller and Atmel’s development tools.

28. Pinout

The pinout of XMEGA A3 is shown in ”Block Diagram/Pinout” on page 2. In addition to general I/O functionality, each pin may have several function. This will depend on which peripheral is enabled and connected to the actual pin. Only one of the alternate pin functions can be used at the time.

28.1 Alternate Pin Function Description

The tables below shows the notation for all pin functions available and describe its function.

28.1.1 Operation/Power Supply

VCC	Digital supply voltage
AVCC	Analog supply voltage
GND	Ground

28.1.2 Analog functions

ACxn	Analog Comparator input port x pin y
ADCn	Analog to Digital Converter input port x pin y
DACn	Digital to Analog Converter output port x pin y
AREFx	Analog Reference input port x pin

28.1.3 Timer functions

OCnx	Output Compare Channel x for Timer n
_OCnx	Inverted Output Compare Channel x for Timer n

28.1.4 Communication functions

SCL	Serial Clock for TWI
SDA	Serial Data for TWI
XCK0	Transfer Clock for USART n
RxD0	Receiver Data for USART n
TxD0	Transmitter Data for USART n
_SS	Slave Select for SPI
MOSI	Master Out Slave In for SPI
MISO	Master In Slave Out for SPI
SCK	Serial Clock for SPI

28.1.5 Oscillators

TOSCn	Timer Oscillator pin x
XTALn	Input/Ouptut to inverting Oscillator

28.1.6 DEBUG/SYSTEM functions

TEST	Test pin
PROG	Programming pin
RESET	Reset pin
PDI_CLK	Program and Debug Interface Clock
PDI_DATA	Program and Debug Interface Data
TCK	JTAG Test Clock
TDI	JTAG Test Data In
TDO	JTAG Test Data Out
TMS	JTAG Test Mode Select

28.2 Alternate Pin Functions

The tables below shows the main and alternate pin functions for all pins on each port. It also shows which peripheral which make use of or enable the alternate pin function.

Table 28-1. Port A - Alternate functions

PORT A	PIN #	INTERRUPT	ADCA POS	ADCA NEG	ADAA GAINPOS	ADCA GAINNEG	ACA POS	ACA NEG	ACA OUT	DACA	REFA
GND	60										
AVCC	61										
PA0	62	SYNC	ADC0	ADC0	ADC0		AC0	AC0			AREFA
PA1	63	SYNC	ADC1	ADC1	ADC1		AC1	AC1			
PA2	64	SYNC/ASYNC	ADC2	ADC2	ADC2		AC2			DAC0	
PA3	1	SYNC	ADC3	ADC3	ADC3		AC3	AC3		DAC1	
PA4	2	SYNC	ADC4		ADC4	ADC4	AC4				
PA5	3	SYNC	ADC5		ADC5	ADC5	AC5	AC5			
PA6	4	SYNC	ADC6		ADC6	ADC6	AC6				
PA7	5	SYNC	ADC7		ADC7	ADC7		AC7	AC0 OUT		

Table 28-2. Port B - Alternate functions

PORT B	PIN #	INTERRUPT	ADCB POS	ADCB NEG	ADCB GAINPOS	ADCB GAINNEG	ACB POS	ACB NEG	ACB OUT	DACB	REFB	JTAG
PB0	6	SYNC	ADC0	ADC0	ADC0		AC0	AC0			AREFB	
PB1	6	SYNC	ADC1	ADC1	ADC1		AC1	AC1				
PB2	8	SYNC/ASYNC	ADC2	ADC2	ADC2		AC2			DAC0		
PB3	9	SYNC	ADC3	ADC3	ADC3		AC3	AC3		DAC1		
PB4	10	SYNC	ADC4		ADC4	ADC4	AC4					TMS

Table 28-2. Port B - Alternate functions

PORT B	PIN #	INTERRUPT	ADCB POS	ADCB NEG	ADCB GAINPOS	ADCB GAINNEG	ACB POS	ACB NEG	ACB OUT	DACB	REFB	JTAG
PB5	11	SYNC	ADC5		ADC5	ADC5	AC5	AC5				TDI
PB6	12	SYNC	ADC6		ADC6	ADC6	AC6					TCK
PB7	13	SYNC	ADC7		ADC7	ADC7		AC7	AC0 OUT			TDO
GND	14											
VCC	15											

Table 28-3. Port C - Alternate functions

PORT C	PIN #	INTERRUPT	TCC0	AWEXC	TCC1	USARTC0	USARTC1	SPIC	TWIC	CLOCKOUT	EVENTOUT
PC0	16	SYNC	OC0A	$\overline{\text{OC0A}}$					SDA		
PC1	17	SYNC	OC0B	OC0A		XCK0			SCL		
PC2	18	SYNC/ASYNC	OC0C	$\overline{\text{OC0B}}$		RXD0					
PC3	19	SYNC	OC0D	OC0B		TXD0					
PC4	20	SYNC		$\overline{\text{OC0C}}$	OC1A			$\overline{\text{SS}}$			
PC5	21	SYNC		OC0C	OC1B		XCK1	MOSI			
PC6	22	SYNC		$\overline{\text{OC0D}}$			RXD1	MISO			
PC7	23	SYNC		OC0D			TXD1	SCK		CLKOUT	EVOUT
GND	24										
VCC	25										

Table 28-4. Port D - Alternate functions

PORT D	PIN #	INTERRUPT	TCD0	TCD1	USARTD0	USARTD1	SPDI	TWID	CLOCKOUT	EVENTOUT
PD0	26	SYNC	OC0A					SDA		
PD1	27	SYNC	OC0B		XCK0			SCL		
PD2	28	SYNC/ASYNC	OC0C		RXD0					
PD3	29	SYNC	OC0D		TXD0					
PD4	30	SYNC		OC1A			$\overline{\text{SS}}$			
PD5	31	SYNC		OC1B		XCK1	MOSI			
PD6	32	SYNC				RXD1	MISO			
PD7	33	SYNC				TXD1	SCK		CLKOUT	EVOUT
GND	34									
VCC	35									

Table 28-5. Port E - Alternate functions

PORT E	PIN #	INTERRUPT	TCE0	AWEXEI	TCE1	USARTE0	USARTE1	SPIE	TWIE	CLOCKOUT	EVENTOUT
PE0	36	SYNC	OC0A	$\overline{\text{OC0A}}$					SDA		
PE1	37	SYNC	OC0B	OC0A		XCK0			SCL		
PE2	38	SYNC/ASYNC	OC0C	$\overline{\text{OC0B}}$		RXD0					
PE3	39	SYNC	OC0D	OC0B		TXD0					
PE4	40	SYNC		$\overline{\text{OC0C}}$	OC1A			$\overline{\text{SS}}$			
PE5	41	SYNC		OC0C	OC1B		XCK1	MOSI			

Table 28-5. Port E - Alternate functions

PORT E	PIN #	INTERRUPT	TCE0	AWEXEI	TCE1	USARTE0	USARTE1	SPIE	TWIE	CLOCKOUT	EVENTOUT
PE6	42	SYNC		$\overline{\text{OC0D}}$			RXD1	MISO			
PE7	43	SYNC		OC0D			TXD1	SCK		CLKOUT	EVOUT
GND	44										
VCC	45										

Table 28-6. Port F - Alternate functions

PORT F	PIN #	INTERRUPT	TCF0	TCF1	USARTF0	USARTF1	SPIF	TWIF
PF0	46	SYNC	OC0A					SDA
PF1	47	SYNC	OC0B		XCK0			SCL
PF2	48	SYNC/ASYNC	OC0C		RXD0			
PF3	49	SYNC	OC0D		TXD0			
PF4	50	SYNC		OC1A			$\overline{\text{SS}}$	
PF5	51	SYNC		OC1B		XCK1	MOSI	
PF6	54	SYNC				RXD1	MISO	
PF7	55	SYNC				TXD1	SCK	
GND	52							
VCC	53							

29. Electrical Characteristics - TBD

29.1 Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on any Pin with respect to Ground	-0.5V to V_{CC}+0.5V
Maximum Operating Voltage	3.6V
DC Current per I/O Pin	20.0 mA
DC Current V_{CC} and GND Pins	200.0 mA

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

29.2 DC Characteristics

T_A = -40°C to 85°C, V_{CC} = 1.8V to 3.6V (unless otherwise noted)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IL}	Input Low Voltage, except XTAL1 pin					V
V_{IL1}	Input Low Voltage, XTAL1 pins					V
V_{IH}	Input High Voltage, except XTAL1 pin					V
V_{IH1}	Input High Voltage, XTAL1 pin					V
V_{OL}	Output Low Voltage					
V_{OH}	Output High Voltage					
I_{IL}	Input Leakage Current I/O Pin					µA
I_{IH}	Input Leakage Current I/O Pin					µA
R_{RST}	Reset Pull-up Resistor					kΩ
R_{PU}	I/O Pin Pull-up Resistor					kΩ
I_{CC}	Power Supply Current	Active 32 MHz				mA
		Active 20 MHz				mA
		Active 8MHz				mA
		Idle 32 MHz				mA
		Idle 20 MHz				mA
	Power-down mode	WDT disabled				µA
		WDT slow sampling				µA
		WDT fast sampling				

Note: 1. “Max” means the highest value where the pin is guaranteed to be read as low
2. “Min” means the lowest value where the pin is guaranteed to be read as high

29.3 ADC Characteristics – TBD

Table 29-1. ADC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
	Resolution					LSB
	Integral Non-Linearity (INL)					LSB
	Differential Non-Linearity (DNL)					LSB
	Gain Error					LSB
	Offset Error					LSB
	Conversion Time					µs
	ADC Clock Frequency					MHz
	DC Supply Voltage					mA
	Source Impedance					Ω
	Start-up time					µs
AVCC	Analog Supply Voltage		VCC - 0.3		VCC + 0.3	V

Table 29-2. ADC Gain Stage Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
	Gain					
	Input Capacitance					pF
	Offset Error					mV
	Gain Error					%
	Signal Range					V
	DC Supply Current					mA
	Start-up time					# clk cycles

29.4 DAC Characteristics – TBD

Table 29-3. DAC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
	Resolution					LSB
	Integral Non-Linearity (INL)					LSB
	Differential Non-Linearity (DNL)					LSB
	Gain Error					LSB
	Offset Error					LSB
	Calibrated Gain/Offset Error					LSB
	Output Range					V
	Output Settling Time					µs
	Output Capacitance					nF
	Output Resistance					kΩ
	Reference Input Voltage					V
	Reference Input Capacitance					pF
	Reference Input Resistance					kΩ
	Current Consumption					mA
	Start-up time					µs

29.5 Analog Comparator Characteristics – TBD

Table 29-4. Analog Comparator Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
	Offset					mV
	Hysteresis	No				mV
		Low				
		High				
	Propagation Delay	High Speed mode				ns
		Low power mode				
	Current Consumption	High Speed mode				µA
		Low power mode				
	Start-up time					µs

30. Typical Characteristics - TBD

31. Peripheral Module Address Map

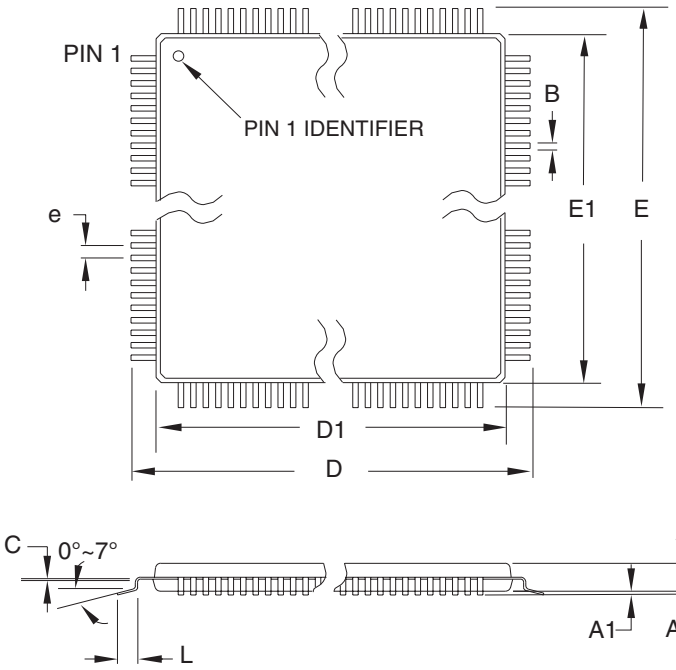
The address maps shows the base address for each peripheral and module in XMEGA A3. For complete register description and summary for each peripheral module, refer to the XMEGA A Manual.

Base Address	Name	Description
0x0000	GPIO	General Purpose IO Registers
0x0010	VPORT0	Virtual Port 0
0x0014	VPORT1	Virtual Port 1
0x0018	VPORT2	Virtual Port 2
0x001C	VPORT3	Virtual Port 2
0x0030	CPU	CPU
0x0040	CLK	Clock Control
0x0048	SLEEP	Sleep Controller
0x0050	OSC	Oscillator Control
0x0060	DFLLRC32M	DFLL for the 32 MHz Internal RC Oscillator
0x0068	DFLLRC2M	DFLL for the 2 MHz RC Oscillator
0x0070	PR	Power Reduction
0x0078	RST	Reset Controller
0x0080	WDT	Watch-Dog Timer
0x0090	MCU	MCU Control
0x00A0	PMIC	Programmable MUltilevel Interrupt Controller
0x00B0	PORTCFG	Port Configuration
0x00C0	AES	AES Module
0x0100	DMA	DMA Controller
0x0180	EVSYS	Event System
0x01C0	NVM	Non Volatile Memory (NVM) Controller
0x0200	ADCA	Analog to Digital Converter on port A
0x0240	ADCB	Analog to Digital Converter on port B
0x0320	DACB	Digital to Analog Converter on port B
0x0380	ACA	Analog Comparator pair on port A
0x0390	ACB	Analog Comparator pair on port B
0x0400	RTC	Real Time Counter
0x0480	TWIC	Two Wire Interface on port C
0x0490	TWID	Two Wire Interface on port D
0x04A0	TWIE	Two Wire Interfaceon port E
0x04B0	TWIF	Two Wire Interface on port F
0x0600	PORTA	Port A
0x0620	PORTB	Port B
0x0640	PORTC	Port C
0x0660	PORTD	Port D
0x0680	PORTE	Port E
0x06A0	PORTF	Port F
0x07E0	PORTR	Port R
0x0800	TCC0	Timer/Counter 0 on port C
0x0840	TCC1	Timer/Counter 1 on port C
0x0880	AWEXC	Advanced Waveform Extension on port C
0x0890	HIRESC	High Resolution Extension on port C
0x08A0	USARTC0	USART 0 on port C
0x08B0	USARTC1	USART 1 on port C
0x08C0	SPIC	Serial Peripheral Interface on port C
0x08F8	IRCOM	Infrared Communication Module
0x0900	TCD0	Timer/Counter 0 on port D
0x0940	TCD1	Timer/Counter 1 on port D
0x0990	HIRESD	High Resolution Extension on port D
0x09A0	USARTD0	USART 0 on port D
0x09B0	USARTD1	USART 1 on port D
0x09C0	SPID	Serial Peripheral Interface on port D
0x0A00	TCE0	Timer/Counter 0 on port E
0x0A40	TCE1	Timer/Counter 1 on port E
0x0A80	AWEXE	Advanced Waveform Extensionon port E
0x0A90	HIRESE	High Resolution Extension on port E
0x0AA0	USARTE0	USART 0 on port E
0x0AB0	USARTE1	USART 1 on oirt E

Base Address	Name	Description
0x0AC0	SPIE	Serial Peripheral Interface on port E
0x0B00	TCF0	Timer/Counter 0 on port F
0x0B40	TCF1	Timer/Counter 1 on port F
0x0B90	HIRESF	High Resolution Extension on port F
0x0BA0	USARTF0	USART 0 on port F
0x0BB0	USARTF1	USART 1 on port F
0x0BC0	SPIF	Serial Peripheral Interface on port F

32. Packaging information

32.1 64A



COMMON DIMENSIONS
(Unit of Measure = mm)

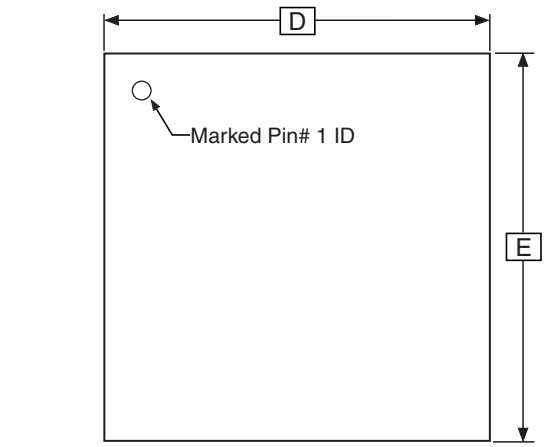
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	15.75	16.00	16.25	
D1	13.90	14.00	14.10	Note 2
E	15.75	16.00	16.25	
E1	13.90	14.00	14.10	Note 2
B	0.30	–	0.45	
C	0.09	–	0.20	
L	0.45	–	0.75	
e	0.80 TYP			

Notes:
1. This package conforms to JEDEC reference MS-026, Variation AEB.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10 mm maximum.

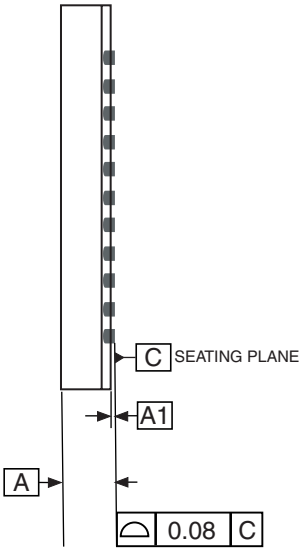
10/5/2001

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**64A,** 64-lead, 14 x 14 mm Body Size, 1.0 mm Body Thickness, 0.8 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)	64A	B

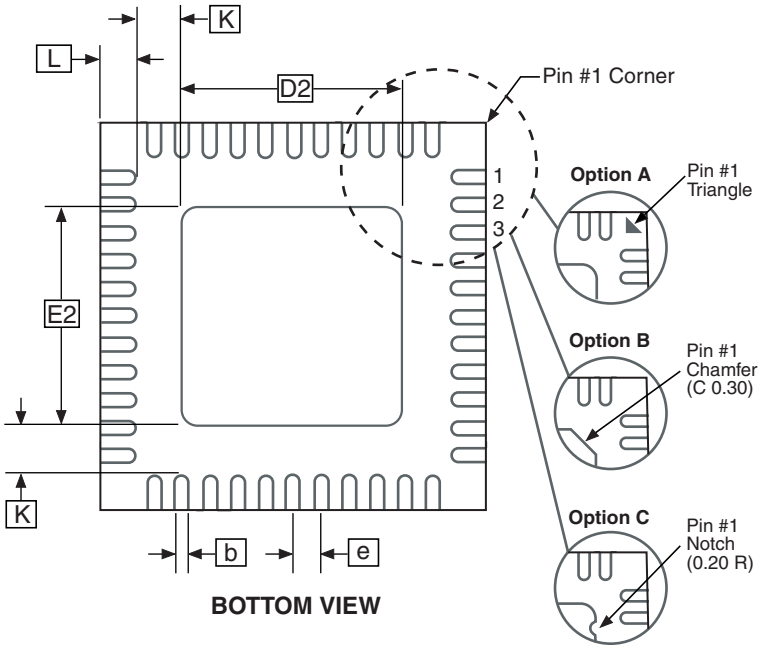
32.2 64M1



TOP VIEW



SIDE VIEW



BOTTOM VIEW

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.80	0.90	1.00	
A1	–	0.02	0.05	
b	0.18	0.25	0.30	
D	8.90	9.00	9.10	
D2	5.20	5.40	5.60	
E	8.90	9.00	9.10	
E2	5.20	5.40	5.60	
e	0.50 BSC			
L	0.35	0.40	0.45	
K	1.25	1.40	1.55	

Note: 1. JEDEC Standard MO-220, (SAW Singulation) Fig. 1, VMMD.
2. Dimension and tolerance conform to ASMEY14.5M-1994.

5/25/06

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**64M1**, 64-pad, 9 x 9 x 1.0 mm Body, Lead Pitch 0.50 mm, 5.40 mm Exposed Pad, Micro Lead Frame Package (MLF)	64M1	G

33. Errata

33.1 All rev.

No known errata.

34. Datasheet Revision History

34.1 8068A – 02/08

1. Initial revision.

Table of Contents

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