FEATURES

- 4 Matched NPN Transistors (300)
  4 Matched PNP Transistors (320)
  2 Matched NPNs and PNPs (340)
- Monolithic Construction
- Low Noise
  - $0.75\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$ (PNP)
  - $0.8\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$ (NPN)
- High Speed
  - f_T = 350 MHz (NPN)
  - f_T = 325 MHz (PNP)
- Excellent Matching – 500 µV typical between devices of same gender
- Dielectrically Isolated for low crosstalk and high DC isolation
- 36V V_{CEO}

APPLICATIONS

- Microphone Preamplifiers
- Current Sources
- Current Mirrors
- Log/Antilog Amplifiers
- Multipliers
- Servos

DESCRIPTION

The THAT 300 series are large-geometry, 4-transistor, monolithic NPN and/or PNP arrays exhibiting both high speed and low noise, with excellent parameter matching between transistors of the same gender. With typical base-spreading resistances of 25 ohms for the PNP devices (30 ohms for the NPNs), their resulting low voltage noise of under 1 nV/root-Hz makes the 300 series ideally suited for low-noise amplifier input stages, among other applications.

Fabricated in a dielectrically isolated, complementary bipolar process, each transistor is electrically insulated from the others by a layer of insulating oxide (not the reverse-biased PN junctions used in conventional arrays) and exhibit inter-device crosstalk and DC isolation similar to that expected from discrete transistors. The resulting low collector-to-substrate capacitance produces a typical NPN f_T of 350 MHz (325 MHz for the PNPs). Substrate biasing is not required for normal operation, though the substrate should be grounded to optimize speed and minimize crosstalk.

An eight-transistor bare-die array with similar performance characteristics (the THAT 380G) is also available from THAT Corporation. Please contact us directly or through your local distributor for more information.

Part Number	Configuration	Package
THAT300P	4-Matched NPN Transistors	DIP14
THAT300S		SO14
THAT320P	4- Matched PNP Transistors	DIP14
THAT320S		SO14
THAT340P	2 Matched NPN Transistors and 2 Matched PNP Transistors	DIP14
THAT340S		SO14

Table 1. Ordering Info

SPECIFICATIONS[1]

Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
NPN Collector-Emitter Voltage	BV_{CEO}	I_C = 1 mAdc, I_B = 0	36	40	—	V
NPN Collector-Base Voltage	BV_{CBO}	I_C =10 µAdc, I_E=0	36	40	—	V
NPN Emitter-Base Voltage	BV_{EBO}	I_E = 100 µAdc, I_C = 0	5	—	—	V
NPN Collector Current	$I_{C\ MAX}$		10	20		mA
NPN Emitter Current	$I_{E\ MAX}$		10	20		mA
PNP Collector-Emitter Voltage	BV_{CEO}	I_C = 1 mAdc, I_B = 0	–36	–40	—	V
PNP Collector-Base Voltage	BV_{CBO}	I_C = 10 µAdc, I_E = 0	–36	–40	—	V
PNP Emitter-Base Voltage	BV_{EBO}	I_E = 100 µAdc, I_C = 0	–5	—	—	V
PNP Collector Current	$I_{C\ MAX}$		–10	–20		mA
PNP Emitter Current	$I_{E\ MAX}$		–10	–20		mA
Collector-Collector Voltage	BV_{CC}		±100	±200	—	V
Emitter-Emitter Voltage	BV_{EE}		±100	±200	—	V
Operating Temperature Range	T_A		0		70	°C
Maximum Junction Temperature	T_{JMAX}				150	°C
Storage Temperature	T_{STORE}		-45		125	°C

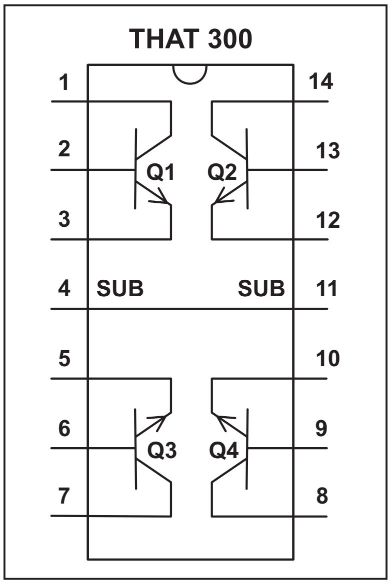

Fig 1. 300 Pinout

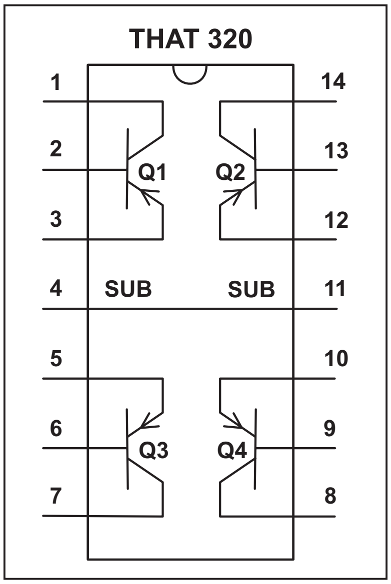

Fig 2. 320 Pinout

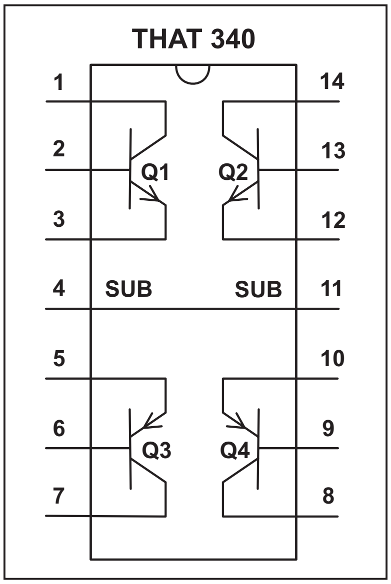

Fig 3. 340 Pinout

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SPECIFICATIONS[1] (Cont'd)

NPN Electrical Characteristics[2]

Parameter	Symbol	Conditions	Min	Typ	Max	Units
NPN Current Gain	h_{fe}	V_{CB} = 10 V				
		I_C = 1 mA	60	100	—	
		I_C = 10 µA		100	—	
NPN Current Gain Matching	Δh_{fe}	V_{CB} = 10 V, I_C = 1 mA	—	5	—	%
NPN Noise Voltage Density	e_N	V_{CB} = 10 V, I_C = 1 mA, 1 kHz	—	0.8	—	$nV/\sqrt{Hz}$
NPN Gain-Bandwidth Product	f_T	I_C = 1 mA, V_{CB} = 10 V		350		MHz
NPN ΔV_{BE} (THAT300: V_{BE1}-V_{BE2} ;V_{BE3}-V_{BE4}) (THAT340: V_{BE1}-V_{BE2})						
	V_{OS}	I_C = 1 mA	—	±0.5	±3	mV
		I_C = 10 µA	—	±0.5		mV
NPN ΔI_B (THAT300: I_{B1}-I_{B2}, I_{B3}-I_{B4}) (THAT340: I_{B1}-I_{B2})						
	I_{OS}	I_C = 1 mA	—	±500	±1500	nA
		I_C = 10 µA	—	±5		nA
NPN Collector-Base Leakage Current	I_{CBO}	V_{CB} = 25 V	—	25	—	pA
NPN Bulk Resistance	r_{BE}	V_{CB} = 0 V, 10 µA < I_C < 10 mA	—	2	—	Ω
NPN Base Spreading Resistance	r_{bb}	V_{CB} = 10 V, I_C = 1 mA	—	30	—	Ω
NPN Collector Saturation Voltage	$V_{CE(SAT)}$	I_C = 1 mA, I_B = 100µA	—	0.05		V
NPN Output Capacitance	C_{OB}	V_{CB} = 10 V, I_E = 0 mA, 100 kHz		3		pF
NPN Collector-CollectorCapacitance (THAT300: Q1-Q2, Q3-Q4) (THAT340: Q1-Q2)						
	C_{CC}	V_{CC} = 0 V, 100 kHz		0.7		pF

PNP Electrical Characteristics[2]

Parameter	Symbol	Conditions	Min	Typ	Max	Units
PNP Current Gain	h_{fe}	V_{CB} = 10 V				
		I_C = 1 mA	50	75	—	
		I_C = 10 µA		75	—	
PNP Current Gain Matching	Δh_{fe}	V_{CB} = 10 V, I_C = 1 mA	—	5	—	%
PNP Noise Voltage Density	e_N	V_{CB} = 10 V, I_C = 1 mA, 1 kHz	—	0.75	—	$nV/\sqrt{Hz}$
PNP Gain-Bandwidth Product	f_T	I_C = 1 mA, V_{CB} = 10 V		325		MHz
PNP ΔV_{BE} (THAT320: V_{BE1}-V_{BE2}; V_{BE3}-V_{BE4}) (THAT340: V_{BE3}-V_{BE4})						
	V_{OS}	I_C = 1 mA	—	±0.5	±3	mV
		I_C = 10 µA	—	±0.5		mV
PNP ΔI_B (THAT320: I_{B1}-I_{B2}; I_{B3}-I_{B4}) (THAT340: I_{B3}-I_{B4})						
	I_{OS}	I_C = 1 mA	—	±700	±1800	nA
		I_C = 10 µA	—	±7		nA
PNP Collector-Base Leakage Current	I_{CBO}	V_{CB} = 25 V	—	–25	—	pA

1. All specifications subject to change without notice.
2. Unless otherwise noted, T_A=25°C.

SPECIFICATIONS[1] (Cont'd)

PNP Bulk Resistance	r_{BE}	V_{CB} = 0 V, 10µA < I_C< 10 mA	—	2	—	Ω
PNP Base Spreading Resistance	r_{bb}	V_{CB} = 10 V, I_C = 1 mA	—	25	—	Ω
PNP Collector Saturation Voltage	$V_{CE(SAT)}$	I_C = 1 mA, I_B = 100 µA	—	–0.05		V
PNP Output Capacitance	C_{OB}	V_{CB} = 10 V, I_E = 0 mA, 100 kHz		3		pF
PNP Collector-Collector Capacitance (THAT320: Q1-Q2; Q3-Q4) (THAT340: Q3-Q4)	C_{CC}	V_{CC} = 0 V, 100 kHz		0.6		pF

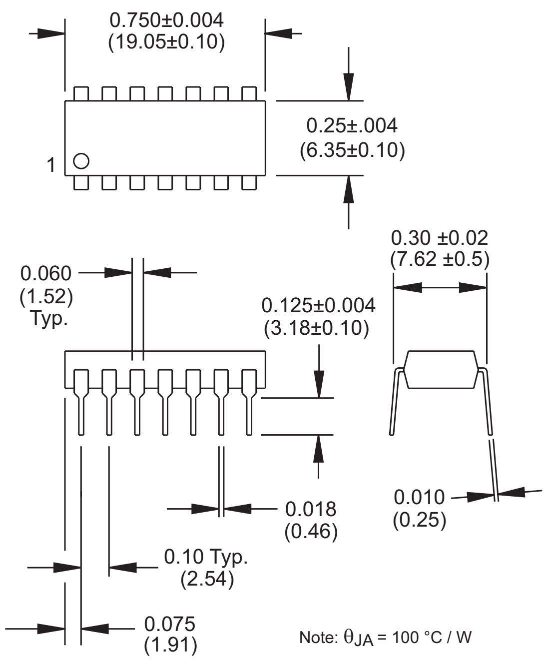

Figure 4. Dual-In-Line Package Outline

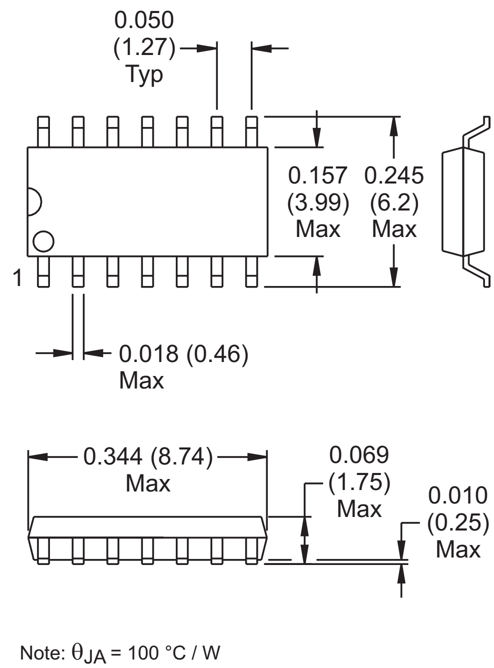

Figure 5. Surface-Mount Package Outline

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LIFE SUPPORT POLICY

THAT Corporation products are not designed for use in life support equipment where malfunction of such products can reasonably be expected to result in personal injury or death. The buyer uses or sells such products for life suport application at the buyer's own risk and agrees to hold harmless THAT Corporation from all damages, claims, suits or expense resulting from such use.

CAUTION: THIS IS AN ESD (ELECTROSTATIC DISCHARGE) SENSITIVE DEVICE.

It can be damaged by the currents generated by electrostatic discharge. Static charge and therefore dangerous voltages can accumulate and discharge without detection causing a loss of function or performance to occur.

The transistors in this device are unprotected in order to maximize performance and flexibility. They are more sensitive to ESD damage than many other ICs which include protection devices at their inputs. Note that all of the pins (not just the "inputs") are susceptible.

Use ESD preventative measures when storing and handling this device. Unused devices should be stored in conductive packaging. Packaging should be discharged to the destination socket before the devices are removed. ESD damage can occur to these devices even after they are installed in a board-level assembly. Circuits should include specific and appropriate ESD protection.

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