THAT Corporation

**Dual Balanced
Line Receiver ICs**

THAT 1280, 1283, 1286

FEATURES

- High CMRR: typ. 90 dB at 60Hz
- Self-contained
- Excellent audio performance
  – Wide bandwidth: typ. >7.6 MHz
  – High slew rate: typ. 15 V/μs
  – Low distortion: typ. 0.0006% THD
  – Low noise: typ. -104.5 dBu
- Low current: typ. 3 mA (per amplifier)
- Several gains: 0 dB, ±3 dB, ±6 dB
- Industry Standard Pinout

APPLICATIONS

- Balanced Audio Line Receivers
- Instrumentation Amplifiers
- Differential Amplifiers
- Precision Summers
- Current Shunt Monitors

Description

The THAT 1280 series of precision differential amplifiers was designed primarily for use as balanced line receivers for audio applications. Gains of 0 dB, ±3 dB, and ±6 dB are available to suit various applications requirements.

These devices are laser-trimmed in wafer form to obtain the precision resistor matching needed for high CMR performance and precise gain. Manufactured in THAT Corporation's proprietary complementary dielectric isolation (DI) process, the 1280 series provides the sonic benefits of discrete designs with the simplicity,

reliability, matching, and small size of a fully integrated solution.

All three versions of the part typically exhibit 90 dB of common-mode rejection. With 15 V/μs slew rate, 7.6 MHz or higher bandwidth, and 0.0006% THD, these devices are sonically transparent. Moreover, current consumption is typically a low 6 mA (3 mA per amplifier).

The 1280 series is available in a 14-pin SOIC package. The 1280 is pin-compatible with the TI INA2134, and the 1286 is pin-compatible with the TI INA2137 and the ADI AD8273.

Part No.	Gain	R$_1$ & R$_3$	R$_2$ & R$_4$
THAT1280	0 dB	9 kΩ	9 kΩ
THAT1283	-3 dB	10.5 kΩ	7.5 kΩ
THAT1286	-6 dB	12 kΩ	6 kΩ

Figure 1. Equivalent circuit

Pin Name	Pin Number
N/C	1
IN- A	2
IN+ A	3
V$_{EE}$	4
IN+ B	5
IN- B	6
N/C	7
REF B	8
OUT B	9
SENSE B	10
V$_{CC}$	11
SENSE A	12
OUT A	13
REF A	14

Table 1. Pin assignments

SPECIFICATIONS[1]

Absolute Maximum Ratings[2,3]

Supply Voltages (V_{CC} - V_{EE})	40V	Storage Temperature Range (T_{ST})	-40 to +125 °C
Maximum In- or In+ Voltage	-50V + V_{CC}, 50V + V_{EE}	Operating Temperature Range (T_{OP})	-40 to +85 °C
Max/Min Ref or Sense Voltage	V_{CC} + 0.5V, V_{EE} - 0.5V	Output Short-Circuit Duration (t_{SH})	Continuous
Maximum Output Voltage (V_{OM})	V_{CC} + 0.5V, V_{EE} - 0.5V	Junction Temperature (T_J)	+125 °C

Electrical Characteristics[2,4]

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Current	I_{CC}; -I_{EE}	No signal	—	6	8	mA
Supply Voltage	V_{CC}-V_{EE}		6	—	36	V
Input Voltage Range	$V_{IN-DIFF}$	Differential (equal and opposite swing)				
		1280 (0dB gain)	—	21.5	—	dBu
		1283 (-3dB gain)	—	24.5	—	dBu
		1286 (-6dB gain)	—	27.5	—	dBu
	V_{IN-CM}	Common Mode				
		1280 (0dB gain)	—	27.5	—	dBu
		1283 (-3dB gain)	—	29.1	—	dBu
		1286 (-6dB gain)	—	31	—	dBu
Input Impedance[5]	$Z_{IN-DIFF}$	Differential				
		1280 (0dB gain)	—	18	—	kΩ
		1283 (-3dB gain)	—	21	—	kΩ
		1286 (-6dB gain)	—	24	—	kΩ
	Z_{IN-CM}	Common Mode				
		All versions	—	18	—	kΩ
Common Mode Rejection Ratio	CMRR	Matched source impedances; V_{CM} = ±10V				
		DC	70	90	—	dB
		60Hz	70	90	—	dB
		20kHz	—	85	—	dB
Power Supply Rejection Ratio[6]	PSRR	±3V to ±18V; V_{CC} = -V_{EE}; all gains	—	90	—	dB
Total Harmonic Distortion	THD	V_{out} = 5Vrms, f = 1kHz, BW = 22kHz, R_L = 2 kΩ				
			—	0.0006	—	%
Output Noise	e_{OUT}	22 Hz to 22kHz bandwidth				
		1280 (0dB gain)	—	-104.5	—	dBu
		1283 (-3dB gain)	—	-105.9	—	dBu
		1286 (-6dB gain)	—	-107.3	—	dBu
Slew Rate	SR	R_L = 2kΩ; C_L = 300 pF, all gains	10.5	15	—	V/µs

1. All specifications are subject to change without notice.
2. Unless otherwise noted, T_A=25ºC, V_{CC}=+15V, V_{EE}= -15V.
3. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
4. 0 dBu = 0.775 Vrms.
5. While specific resistor ratios are very closely trimmed, absolute resistance values can vary ±25% from the typical values shown. Input impedance is monitored by lot sampling.
6. Defined with respect to differential gain.
7. Parameter guaranteed over the entire range of power supply and temperature.

Electrical Characteristics (con't)[2,4]

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Small signal bandwidth	BW_{-3dB}	$R_L = 2k\Omega$; $C_L = 10$ pF				
		1280 (0dB gain)	—	7.6	—	MHz
		1283 (-3dB gain)	—	9.6	—	MHz
		1286 (-6dB gain)	—	11.6	—	MHz
Output Gain Error	G_{ER-OUT}		-0.05	—	0.05	dB
Output Voltage Swing	V_{O+}	$R_L = 2k\Omega$; $C_L = 200$ pF	V_{CC}-2.5	V_{CC}-2	—	V
	V_{O-}	$R_L = 2k\Omega$; $C_L = 200$ pF	—	V_{EE}+2	V_{EE}+2.5	V
Output Offset Voltage	V_{OFF}	No signal	-1	—	1	mV
Output Short Circuit Current	I_{SC}	$R_L = 0\ \Omega$	—	±42	—	mA
Capacitive Load[7]	C_L		—	—	300	pF
Channel Separation		f = 1kHz	—	120	—	dB

Figure 2. Simplified test circuit (1/2 of 128x shown)

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Theory of Operation

The THAT 1280 series ICs consist of two high performance opamps with integrated, laser-trimmed resistors. These designs take advantage of THAT's fully complementary dielectric isolation (DI) process to deliver excellent performance with low current consumption. The devices are simple to apply in a wide range of applications.

Resistor Trimming, Values, and CMRR

The 1280-series devices rely upon proprietary, laser-trimmed, silicon-chromium (Si-Cr), thin-film, integrated resistors to deliver the precise matching required to achieve a 90 dB common mode rejection ratio. Trimming is performed in two cycles, both using dc inputs. First, gain is set by trimming the R_1/R_2 pair. Then, CMRR is set by trimming the other pair (R_3/R_4). Generally, only one resistor of each pair is trimmed (whichever needs to increase to meet the required specification).

To achieve 90 dB CMRR, the R_3/R_4 ratio is trimmed to within ±0.005 % of the R_1/R_2 ratio. Since the resistors themselves are on the order of 10 kΩ (see Figure 1 for actual values, which change with the specific part), an increase of as little as 0.6 Ω can reduce the CMRR from over 90 dB to 84 dB. The better the starting CMRR, the more impact (in dB) a given added resistance will have.

Therefore, to achieve this high CMRR in practice, take care to ensure that all source imped-ances remain balanced. To accomplish this, PCB traces carrying signals should be balanced in length, connector resistance should be minimized, and any input capacitance (including strays) should be balanced between the + and - legs of the input circuitry. Note that the additional contact resistance of some sockets is sufficient to undo the effects of precision trimming. Therefore, socketing the parts is not recommended. THAT's 1200-series InGenius® input stages address many of these difficulties through a patented method of increasing common-mode input impedance, and should be considered for any critical applications.

A further consideration is that after trimming, the two resistor divider ratios are tightly controlled, but the actual value of any individual resistor is not. The initial tolerance of the resistors is quite wide, so it is possible for any given resistor to vary over a surprisingly wide range. Lot-to-lot variations of up to ±30 % are to be expected.

Input Considerations

The 1280-series devices are internally protected against input overload via an unusual arrangement of diodes connecting the + and - input pins to the power supply pins. The circuit of Figure 3 shows the arrangement used for the R_3/R_4 side; a similar one applies to the other side. The zener diodes prevent the protection network from conducting until an input pin is raised at least 50 V above V_{CC} or lowered 50V below V_{EE}. Thus, the protection networks protect the devices without constraining the allowable signal swing at the input pins. The reference (and sense) pins are protected via more conventional reverse-biased diodes which will conduct if these pins are raised above V_{CC} or below V_{EE}.

To reduce risk of damage from ESD, and to prevent RF from reaching the devices, THAT recom-mends the circuit of Figure 4. C_3 through C_5 should be located close to the point where the input signal comes into the chassis, preferably directly on the connector. The unusual circuit design is intended to minimize the unbalancing impact of differences in the values of C_4 and C_5 by forcing the capacitance from each input to chassis ground to depend primar-ily on the value of C_3. The circuit shown is approxi-mately ten times less sensitive to mismatches between C_4 and C_5 than the more conventional approach in which the junction of C_4 and C_5 is grounded directly. An excellent discussion of input stage grounding can be found in the June 1995 issue of the Journal of the Audio Engineering Society, Vol. 43, No. 6, in articles by Stephen Macatee, Bill Whitlock, and others.

Note that because of the tight matching of the internal resistor ratios, coupled with the uncertainty

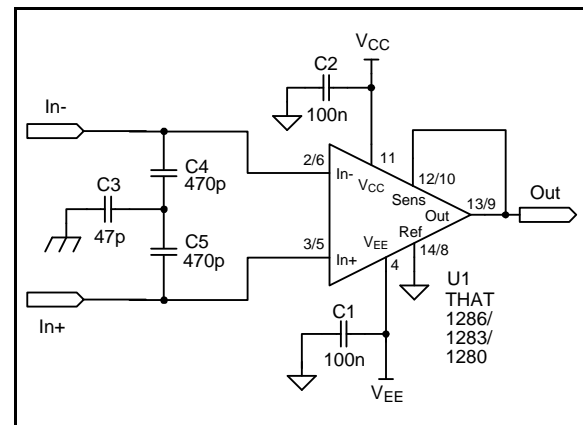Figure 3. Representative input protection circuit

Figure 4. RFI and supply bypassing

in absolute value of any individual resistor, RF bypassing through the addition of R-C networks at the inputs (series resistor followed by a capacitor to ground at each input) is not recommended. The added resistors can interact with the internal ones in unexpected ways. If some impedance for the RF-bypass capacitor to work against is deemed necessary, THAT recommends the use of a ferrite bead or balun instead.

If it is necessary to ac-couple the inputs of the 1280-series parts, the coupling capacitors should be sized to present negligible impedance at any frequencies of interest for common mode rejection. Regardless of the type of coupling capacitor chosen, variations in the values of the two capacitors, working against the 1280-series input impedance (itself subject to potential imbalances in absolute value, even when trimmed for perfect ratio match), can unbalance common mode input signals. This can convert common-mode to balanced signals which will not be rejected by the CMRR of the devices. For this reason, THAT recommends dc-coupling the inputs of the 1280-series devices.

Input Voltage Limitations

When configured, respectively, for -3 dB and -6 dB gain, the 1283 and 1286 devices are capable of accepting input signals above the power supply rails. This is because the internal opamp's inputs connect to the outside world only through the on-chip resistors R_1 through R_4 at nodes a and b as shown in Figure 2. Consider the following analysis.

Differential Input Signals

For differential signals ($v_{IN(DIFF)}$), the limitation to signal handling will be output clipping. The outputs of all the devices typically clip at within 2V of the supply rails. Therefore, maximum differential input signal levels are directly related to the gain and supply rails and can be calculated in dBu as follows:

$$V_{in(diff)} = 20\log\frac{\frac{V_{CC}-V_{EE}}{2}-2V}{\frac{\sqrt{2}}{0.775}} - Gain$$

or

$$V_{in(diff)} = 20\log(V_{CC} - V_{EE} - 4V) - Gain - 6.8dB$$

For example, If V_{CC}=15V, V_{EE}=-15V, and $Gain$ = -3 dB, then

$$V_{in(diff)} = 20\log[15V - (-15V) - 4V] - (-3dB) - 6.8dB$$

$$= 24.5 \text{ dBu}$$

Common-Mode Input Signals

For common-mode input signals, there is essentially no output signal. The limitation on common-mode handling is the point at which the inputs are overloaded. So, we must consider the inputs of the opamp.

For common-mode signals ($V_{IN(CM)}$), the common-mode input current splits to flow through both R_1/R_2 and through

R_3/R_4. Because v_b is constrained to follow V_a, we will consider only the voltage at node a.

The voltage at a can be calculated as:

$$V_a = V_{IN(CM)}\left[\frac{R_4}{R_3+R_4}\right]$$

Solving for $v_{IN(CM)}$,

$$V_{IN(CM)} = V_a\left[\frac{R_3+R_4}{R_4}\right]$$

For the 1280, $(R_3 + R_4)/R_4 = 2$. For the 1283, $(R_3 + R_4)/R_4 = 2.4$. For the 1286, $(R_3 + R_4)/R_4 = 3$. Furthermore, the same constraints apply to v_a as in the differential analysis.

Following the same reasoning as above, the maximum common-mode input signal for the 1280 is $(2V_{CC} - 4)$ V, and the minimum is $(2V_{EE} + 4)$ V. For the 1283, these figures are $(2.4V_{CC} - 4.8)$ V, and $(2.4V_{EE} + 4.8)$ V. For the 1286, these figures are $(3V_{CC} - 6)$ V, and $(3V_{EE} + 6)$ V.

Therefore, for common-mode signals and ±15 V rails, the 1280 will accept up to ~26 V in either direction. As an ac signal, this is 52 V peak-peak, 18.4 V rms, or +27.5 dBu. With the same supply rails, the 1283 will accept up to ~31 V in either direction. As an ac signal, this is 62 V peak-peak, 21.9 V rms, or +29 dBu. With the same supply rails, the 1286 will accept up to ~39 V in either direction. As an ac signal, this is 78 V peak-peak, 27.6 V rms, or +31 dBu.

Of course, in the real world, differential and common-mode signals combine. The maximum signal that can be accommodated will depend on the superposition of both differential and common-mode limitations.

Output Considerations

The 1280-series devices are typically capable of supplying 42 mA into a short circuit. While they will survive a short, power dissipation will rise dramatically if the output is shorted. Junction temperature must be kept under 125 °C to maintain the devices' specifications.

These devices are stable with up to 300 pF of load capacitance over the entire rated temperature range, and even more at room temperature.

Power Supply Considerations

The 1280-series parts are not particularly sensitive to the power supply, but they *do* contain wide bandwidth opamps. Accordingly, small local bypass capacitors should be located within a few inches of the supply pins on these parts, as shown in Figure 4.

Selecting a Gain Variation

The three different parts offer different gain structures to suit different applications. The 1286 is customarily configured for -6 dB gain, but by reversing the resistor connections, it can also be configured for +6 dB. The 1283 is most often configured for -3 dB gain, but can also be configured for +3 dB. The choice of input gain is determined by the input

voltage range to be accommodated, and the power supply voltages used within the circuit.

To minimize noise and maximize signal-to-noise ratio, the input stage should be selected and configured for the highest possible gain that will ensure that maximum-level input signals will not clip the input stage or succeeding stages. For example, with ±18 V supply rails, the 1280-series parts have a maximum output signal swing of +23 dBu. In order to accommodate +24 dBu input signals, the maximum gain for the stage is -1 dB. With ±15 V supply rails, the maximum output signal swing is ~+21.1 dBu; here, -3 dB is the maximum gain. In each case, a 1283 configured for -3 dB gain is the ideal choice. The 1280 (0 dB gain only) will not provide enough headroom at its output to support a +24 dBu input signal. The 1286 (configured for -6 dB gain) will increase noise, thus reducing dynamic range, by attenuating the input signal more than necessary to support a +24 dBu input.

In fact, for most professional audio applications, THAT recommends the -3 dB input configuration possible only with the 1283 in order to preserve dynamic range within a reasonable range of power supply voltages and external headroom limits.

Applications

The THAT 1280, 1283, and 1286 are usually thought of as precision differential amplifiers with gains of zero, -3 and -6 dB respectively. These devices are primarily intended as balanced line receivers for audio applications. However, their topology lends itself to other applications as well.

Basic Balanced Receiver Applications

Figures 5, 6, and 7, respectively, show the 1280, 1286 and 1286 configured as zero, -3 dB, and -6 dB line receivers. Figures 8 and 9, respectively, show the 1283 and 1286 configured as +3 dB and +6 dB line receivers. The higher gains are achieved by swapping the positions of the resistors within each pair in regard to signal input vs. Output.

Precision Summing Application

Figure 10 shows a 1280 configured as a precision summing amplifier. This circuit uses both the In+ and Ref pins as inputs. Because of the excellent matching between the laser-trimmed resistor pairs, the output voltage is precisely equal to the sum of the two input voltages.

Instrumentation Amplifier Application

Figure 11 shows one half of a 1280 configured as an instrumentation amplifier. The two opamps preceding the 1280 buffer the input signal before passing it on to the 1280. The OP270 shown was chosen for its combination of good ac and dc performance. In this configuration, the opamps provide gain equal to $1+(9.98 \text{ k}\Omega / R_g)$ for differential signals, but unity gain for common-mode signals. The 1280 then rejects the common mode signal while passing on the differential portion. As well, the opamps buffer the input of the 1280, raising the circuit's input impedance to both differential *and* common-mode signals. This makes the circuit's common-mode rejection less sensitive to variations in the source impedance driving the stage.

As noted in the Theory of Operation section, THAT's InGenius® input stages use patented circuitry to increase common-mode input impedance. This even further inproves common-mode rejection in real-world applications. See the THAT 1200-series datasheet for more information.
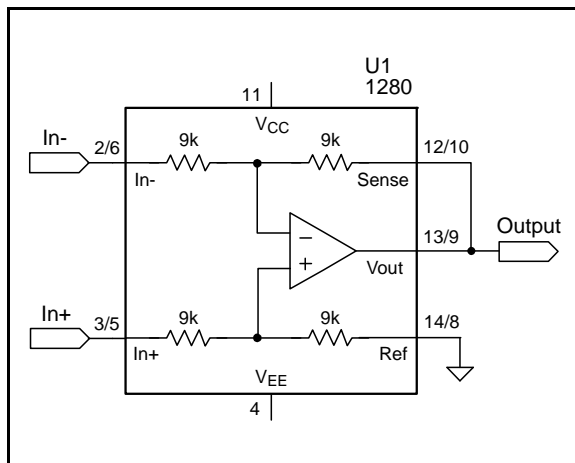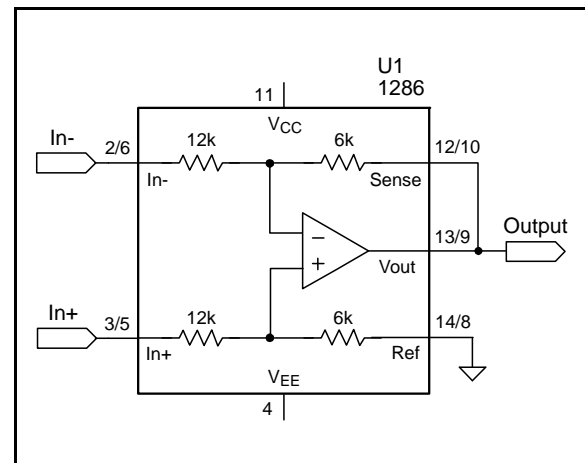

Figure 5. Zero dB line receiver
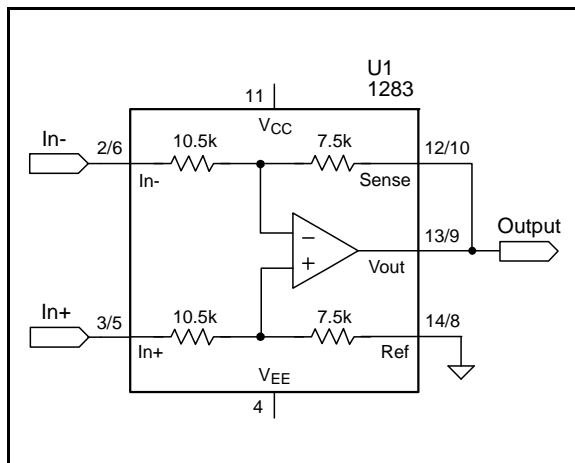

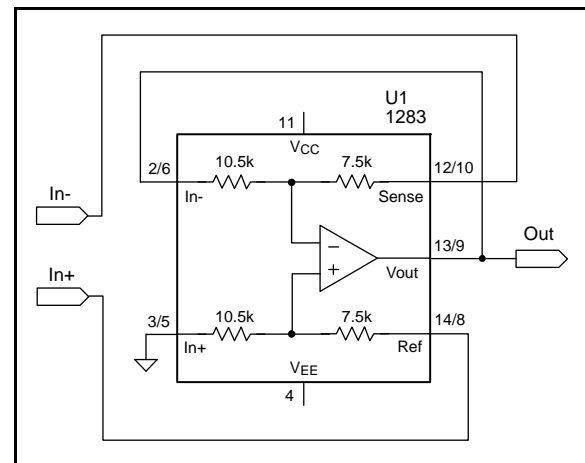Figure 7. -6 dB line receiver

Figure 6. -3 dB line receiver

Figure 8. +3 dB line receiver

Driving Analog-to-Digital Converters

Figure 12 shows a convenient method of driving a typical audio ADC with balanced inputs. This circuit accepts +24 dBu in. By using both halves of a single 1283 IC connected in anti-phase, the maximum signal level between their respective outputs is +27 dBu. An attenuator network brings

Figure 9. +6 dB line receiver

Figure 10. Precision two-input summing circuit

Figure 11. Instrumentation amplifier

this signal down by 18.8 dB while attenuating the noise of the line receivers as well.

In ADC applications such as this, noise is usually a significant consideration. The output noise of one channel of a THAT1283 is -105.9 dBu in a 22 kHz bandwidth, or 26.6 nV/√Hz. Since both channels are used, and since noise adds in random fashion (square-root of the sum of the squares), the total noise level at the input of the resistive pad ($R_1 \sim R_3$) will be -102.9 dBu or 37.5 nV/√Hz. The pad reduces this noise level to -121.7 dBu or 4.3 nV/√Hz at the input to the ADC, while C_1 provides low-pass filtering typically required by ADCs.

The thermal noise of the resistive attenuator is 1.87 nV/√Hz or the equivalent noise of a 210 Ω resistor. Therefore, the total noise density going into the input of the ADC will be

$$e_{n\ ADC\ input} = \sqrt{(1.87\tfrac{nV}{\sqrt{Hz}})^2 + (4.3\tfrac{nV}{\sqrt{Hz}})^2} = 4.7\tfrac{nV}{\sqrt{Hz}}.$$

The noise floor can then be calculated to be

$$Noise_{(dBu)} = 20\ \log\frac{4.7\tfrac{nV}{\sqrt{Hz}}\times\sqrt{22kHz}}{0.775} = -121\ dBu.$$

Controlling Gain in Balanced Systems

When it becomes necessary to control gain in a balanced system, designers are often tempted to keep the signal balanced and use two Voltage Controlled Amplifiers (VCAs) to control the gain on each half of the balanced signal. Unfortunately, this can result in common-mode to differential-mode conversion (degrading CMRR) when there are even slight differences in gain between the VCAs. A better approach is to convert the signal to single-ended, alter the gain, and then convert back to balanced.

Figure 13 shows a stereo gain control for a balanced system. First, we use a 1283 -3 dB line receiver to perform the balanced to single-ended conversion. A THAT 1606, with +6dB gain, is used to rebalance the signal before the circuit's output. A THAT 2162 dual VCA is used to alter gain based on a dc voltage applied at E_C, the "Control Voltage" node. (This point is intended to be driven from a low-impedance, low-noise voltage source. See the THAT 2162-series data sheet for details.)

As shown, the VCA section is configured for "static" gain of -3 dB (gain with 0 Vdc applied to the E_{C-}) due to the choice of ratio of R_3 to R_2 and R_7 to R_6. Additionally, the 1283 has a gain of -3 dB for a total attenuation of 6 dB before the output driver. The 1606 has a gain of 6 dB, therefore the circuit has a gain of 0 dB with 0 V at the control voltage node.

This circuit accepts and delivers over +24 dBu before clipping, and has a noise floor of -91.5 dBu (22 kHz bandwidth). By varying the Control Voltage, gains from -70 dB to +40 dB may easily be achieved. The VCA's "deci-linear" relationship between Control Voltage and gain makes the gain setting precise, predictable, and repeatable.

Figure 12. Circuit for audio ADCs with balanced inputs

Figure 13. Voltage-controlled gain control of a balanced signal

Package Information

The THAT1280 series is available in a 14-pin surface mount (SOIC) package. Package dimensions are shown in Figure 14 below; Pinouts are given in Table 1 on page 1. Ordering information is provided in Table 2 below.

The 1280 series package is entirely lead-free. The lead-frame is copper, plated with successive layers of nickel, palladium, and gold. This approach makes it possible to solder these devices using lead-free and lead-bearing solders.

Neither the lead-frame nor the the plastic mold compound used in the 1280-series contains any hazardous substances as specified in the European Union's *Directive on the Restriction of the Use of Certain Hazardous Substances in Electrical and Electronic Equipment 2002/95/EG* of January 27, 2003.

The surface-mount package is suitable for use in a 100% tin solder process.

Package Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Package Style		See Fig. 14 for dimensions		14 Pin SO		
Thermal Resistance	θ_{JA}	SO package soldered to board		100		ºC/W
Environmental Regulation Compliance		Complies with January 27, 2003 RoHS requirements				
Soldering Reflow Profile		JEDEC JESD22-A113-D (250 ºC)				
Moisture Sensitivity Level	MSL	Above-referenced JEDEC soldering profile		1		

ITEM	MILLIMETERS	INCHES
A	8.56/8.79	0.337/0.346
B	3.81/3.99	0.150/0.157
C	5.80/6.20	0.228/0.244
D	0.36/0.46	0.014/0.018
E	1.27	0.050
F	1.35/1.73	0.053/0.068
G	0.19/0.25	0.0075/0.0098
H	0.41/1.27	0.016/0.05
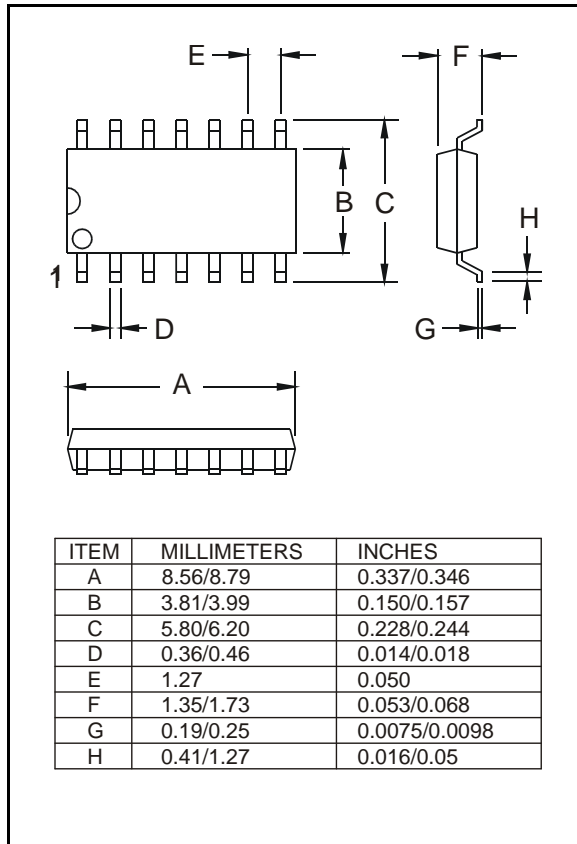
Figure 14. SO package outline drawing

Gain	Order Number
0 dB	1280S14-U
-3 dB	1283S14-U
-6 dB	1286S14-U

Table 2. Ordering information

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