5 Channels ACPI Regulator

General Description

The RT9645 is a combo regulator which is compliant to ACPI specification for desktop/server power management and system application. The part features one switching regulator for DDR memory VDDQ power; a second PWM controller for GMCH core power, a LDO controller for FSB_ VTT termination, a LDO controller for 5VSB to 3VSB conversion; and a dual power control 5VDL for S0 and S3 system power.

The part is generally operated to conform to ACPI specification. In S3 mode, only VDDQ and 3.3VSB regulators remain on while the FSB_ VTT regulator is off. In the transition from S3 to S0, an internal SS capacitor is attached for linear regulators to control its slew rate respectively to avoid inrush current induced.

RT9645 supports both Intel VR11 and AMD K8 platform. There is extra control pin VTT_EN to enable FSB_VTT regulator at AMD K8 mode. This part also implements PWM1 (V_{DDQ}) enabled by release COMP1 at AMD K8 application. This part is assemblyed in the tiny VQFN-24L 4x4 package.

Ordering Information

RT9645□□

- Package Type
  QV : VQFN-24L 4x4
- Operating Temperature Range
  P : Pb Free with Commercial Standard
  G : Green (Halogen Free with Commercial Standard)

Note :

Richtek Pb-free and Green products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.
- 100% matte tin (Sn) plating.

Features

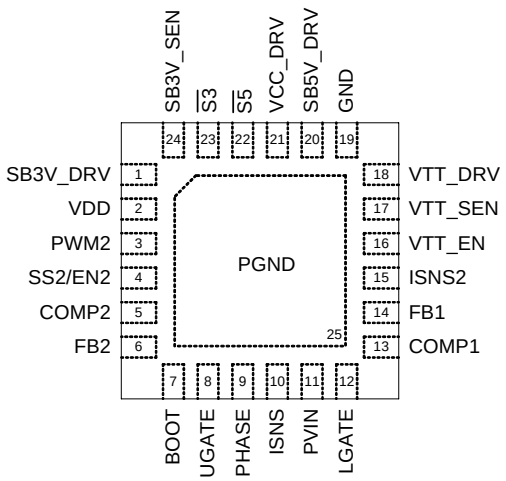
- **Integrated 5 Channels Power Regulator**
- **DC/DC Buck PWM Regulator (Driver Included)**
- **DC/DC Buck PWM Controller**
- **Linear Regulator Controller for FSB_VTT Power**
- **3.3VSB Linear Regulator Controller with 40mA Output Capability**
- **5VDL Switch Control**
- **Conform to ACPI Specification, Supporting Power Management at S0, S3, and S5 State**
- **300kHz Fixed Frequency Oscillator**
- **Low-Side $R_{DS(ON)}$ Current Sensing for Precision Over-Current Detection**
- **Thermal Shutdown**
- **Small 24-Lead VQFN Package**
- **RoHS Compliant and 100% Lead (Pb)-Free**

Applications

- Desktop System Power
- Server System Power

Pin Configurations

(TOP VIEW)



VQFN-24L 4x4

Typical Application Circuit

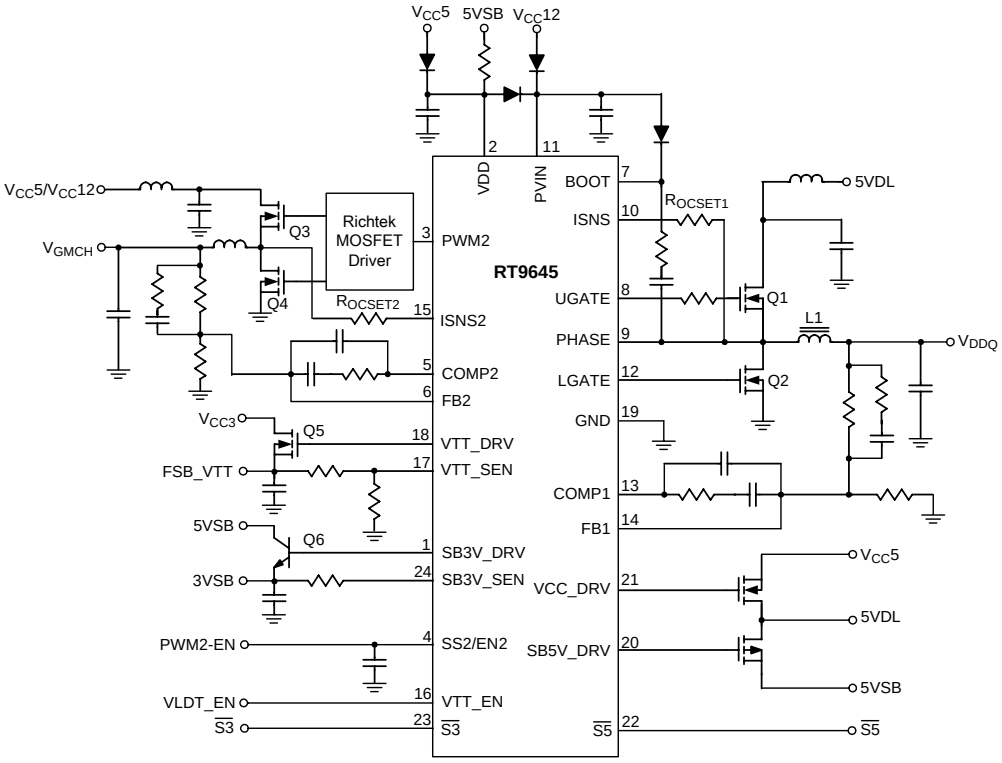


Figure 1. RT9645 Typical Application for Intel Mode

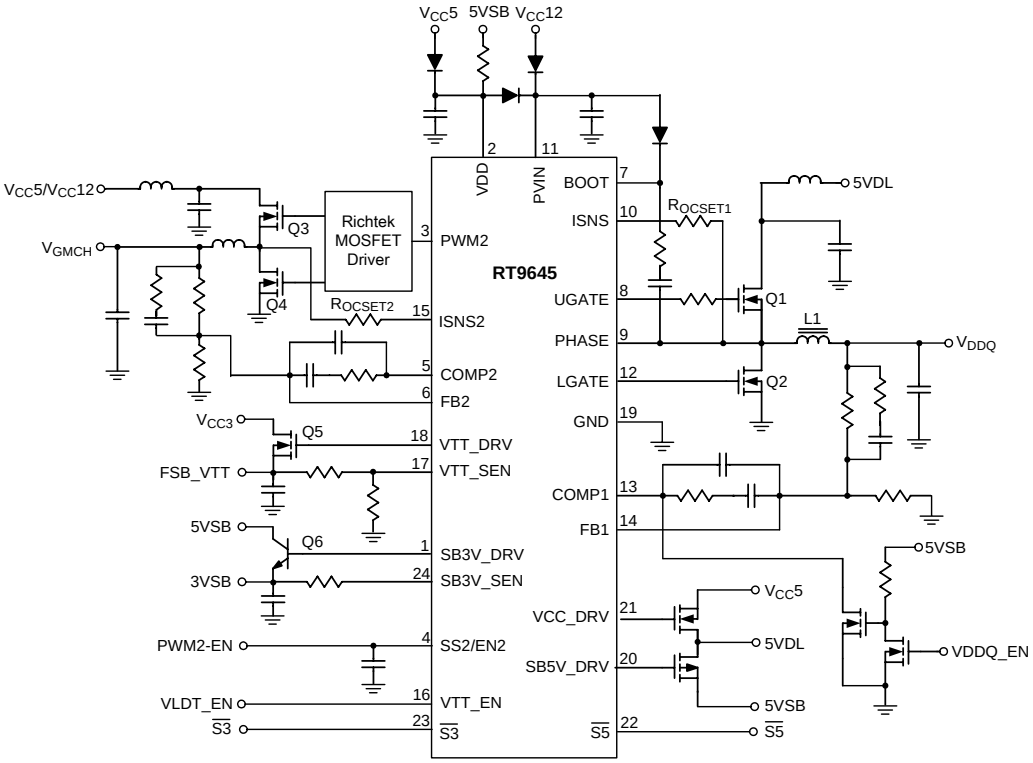


Figure 2. RT9645 Typical Application for AMD K8

Timing Diagram

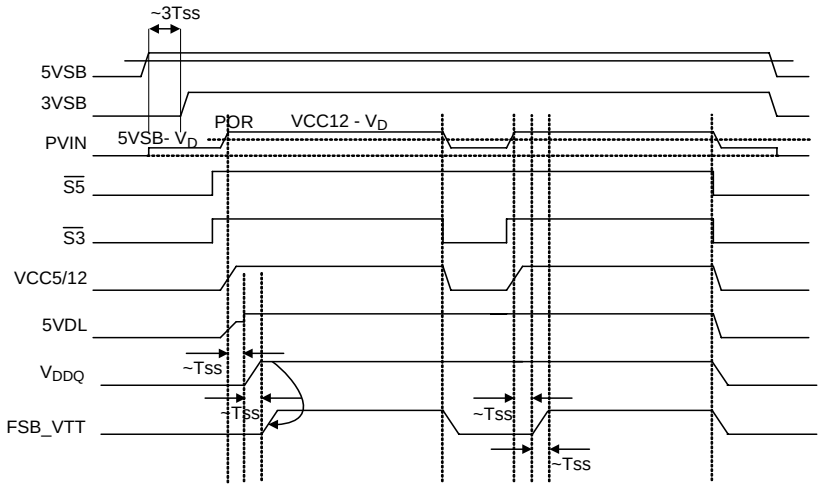


Figure 3. RT9645 Timing Diagram for Intel CPU

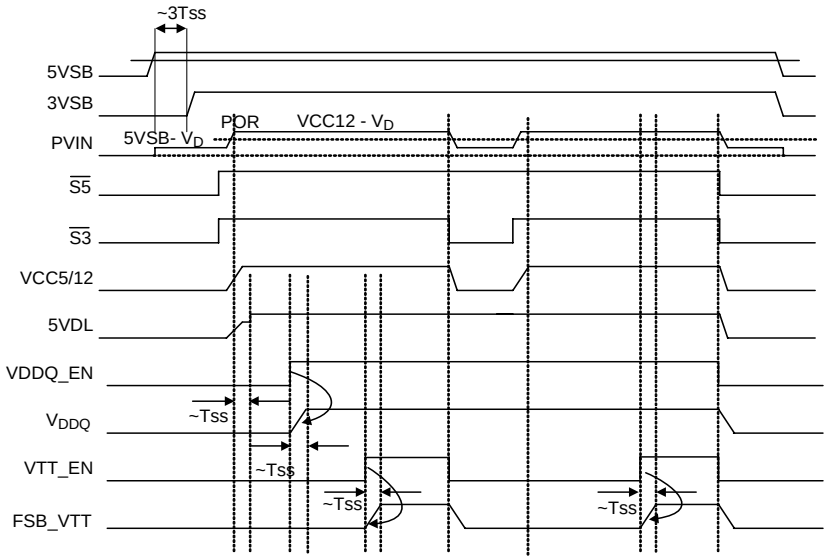


Figure 4. RT9645 Timing Diagram for AMD CPU

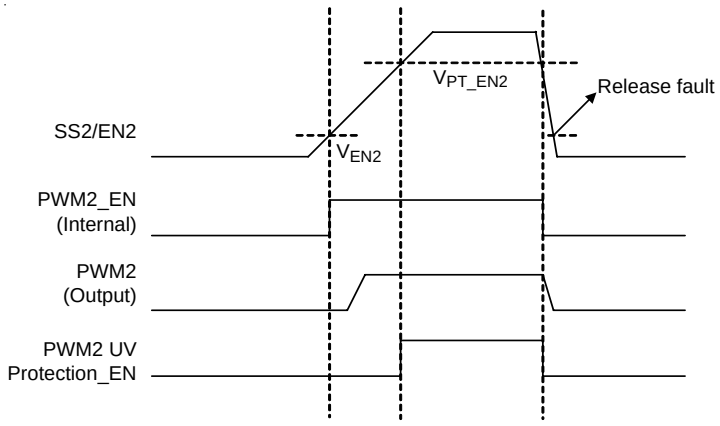
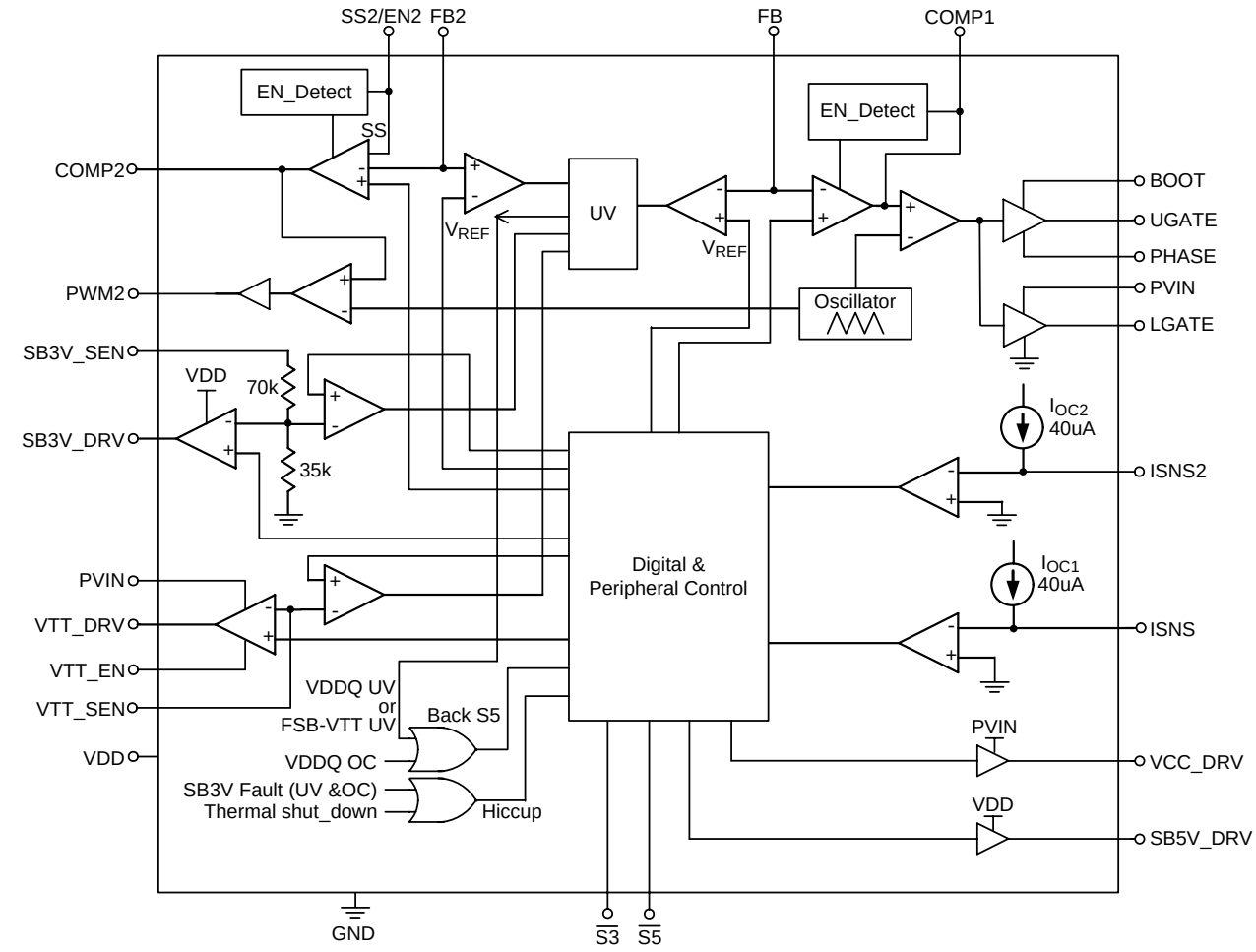


Figure 5. RT9645 Timing Diagram for PWM2

Functional Pin Description

Pin No.	Pin Name	Function Description
1	SB3V_DRV	Gate Drive for 3.3VSB Linear Controller. The pin will be high in S0, S3 and S5 state.
2	VDD	IC Power Supply. 5VSB is generally applied for bias power for IC logics and gate driver control.
3	PWM2	Second PWM Output Signal
4	SS2/EN2	Second PWM Soft Start Ramp/Enable Control SS ramp slope is defined by $V/T = 5\mu A/C_{SS}$.
5	COMP2	Compensation pin of PWM2. Output of the PWM2 error amplifier. Connect compensation network between this pin and FB2.
6	FB2	The output feedback of PWM2. The pin is applied for voltage regulation and provide under-voltage protection.
7	BOOT	The pin is applied for VDDQ PWM bootstrapped power for the embedded driver power.
8	UGATE	High-Side Drive. High-side MOSFET driver output of VDDQ PWM. Connect to gate of high-side MOSFET.
9	PHASE	Phase Node of VDDQ PWM. The pin is applied to sense phase node of VDDQ PWM for gates switch control.
10	ISNS	Current Sense Input. Monitors the voltage drop across the low-side MOSFET for Over current protection. $R_{OCSET1} \times 40\mu A = R_{DS(ON)} \times I_{MAX}$
11	PVIN	Apply to Driver Power Source and generate Internal Power Good Signal.
12	LGATE	Low-Side Drive. The low-side MOSFET driver output. Connect to gate of low-side MOSFET.
13	COMP1	Compensation pin of VDDQ. Output of the VDDQ error amplifier. Connect compensation network between this pin and FB1 In AMD Application. This pin can be used to control VDDQ sequence. This pin needs to be pulled low ($< V_{DIS1}$) to disable the PWM.
14	FB1	The output feedback of PWM1. The pin is applied for voltage regulation, under-voltage and Over Voltage protection.
15	ISNS2	PWM2 Current Sense Input. Monitors the voltage drop across the low-side MOSFET for Over current protection. $R_{OCSET2} \times 40\mu A = R_{DS(ON)} \times I_{MAX}$
16	VTT_EN	In AMD K8 Application, Connect this pin to VLDT_EN to control FSB_VTT Timing.
17	VTT_SEN	Feedback for the FSB_VTT Linear Controller. The pin is applied for FSB_VTT LDO output regulation sense.
18	VTT_DRV	Gate drive for FSB_VTT Linear Controller. The pin will be turned off in S3 and S5 state.
19	GND	Signal Ground.
20	SB5V_DRV	5VSB Control Switch. The pin is applied to drive an external P-Channel MOSFET to switch 5VDL power to 5VSB in S3 state. The pin goes high in S0 and S5 States.
21	VCC_DRV	VCC5 Control Switch. The pin is applied to driver an external N-Channel MOSFET low in S5 and S3 States. The pin goes high in S0 State.
22	$\overline{S5}$	ACPI Control Signal.
23	$\overline{S3}$	ACPI Control Signal.
24	SB3V_SEN	Feedback for the 3.3VSB Linear Controller. The pin is applied for 3.3V LDO output regulation sense.
Exposed Pad (25)	PGND	The exposed pad must be soldered to a large PCB and connected to PGND for maximum power dissipation.

Function Block Diagram



Absolute Maximum Ratings (Note 1)

- Supply Voltage, V_{DD} ---------- 7V
- Supply Voltage, PVIN ---------- 16V
- PHASE to GND
  DC ---------- –0.5V to 7V
  < 200ns ---------- –2V to 7V
- BOOT to GND
  DC ---------- –0.3V to 20V
  < 200ns ---------- –0.3V to 22V
- BOOT, $V_{BOOT} – V_{PHASE}$ ---------- 16V
- UGATE Voltage ---------- V_{PHASE} – 0.3V to V_{BOOT} + 0.3V
- LGATE Voltage ---------- GND – 0.3V to VDD + 0.3V
- Input, Output or I/O Voltage ---------- GND – 0.3V to 7V
- Power Dissipation, PD @ T_A = 25°C
  VQFN-24L 4x4 ---------- 1.85W
- Package Thermal Resistance (Note 4)
  VQFN-24L 4x4, θ_{JA} ---------- 54°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –40°C to 150°C
- ESD Susceptibility (Note 2)
  HBM (Human Body Mode) ---------- 2kV
  MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 3)

- Supply Voltage, V_{DD} ---------- 5V ± 5%
- Supply Voltage, PVIN ---------- 12V ± 10%
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- 0°C to 70°C

Electrical Characteristics

(V_{DD} = 5V, PVIN = 12V, T_A = 25°C, unless otherwise specification)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Supply Current						
Nominal Supply Current	I_{CC}	S0; no load for UGATE / LGATE and regulators	--	4	--	mA
Power-On Reset						
Rising VDD POR Threshold	V_{PORH_5V}		3.9	4.1	4.3	V
VDD POR Hysteresis	V_{PORHYS_5V}		0.06	0.1	--	V
Rising PVIN POR Threshold	V_{PORH_12V}	V_{DD} = 5V	9	9.5	10	V
PVIN POR Hysteresis	V_{PORHYS_12V}	V_{DD} = 5V	0.6	1	--	V

To be continued

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Oscillator and Soft-Start						
PWM Frequency	f_{OSC}		265	300	345	kHz
Ramp Amplitude	ΔV_{OSC}		--	1.2	--	V
Ramp Offset	V_{OSC_OS}		--	0.9	--	V
Soft-Start Interval	T_{SS}		4	8	--	ms
Reference Voltage						
Reference Voltage V_{REF}	V_{REF}		0.784	0.8	0.816	V
VDDQ PWM1 Controller						
UGATE Source	$I_{UGATEsc}$	$V_{BOOT} - V_{PHASE}$ = 12V; $V_{UGATE} - V_{PHASE}$ = 6V	0.5	1	--	A
UGATE Sink	$R_{UGATEsk}$	$V_{BOOT} - V_{PHASE}$ = 12V; $V_{UGATE} - V_{PHASE}$ = 1V	--	4	8	Ω
LGATE Source	$I_{LGATEsc}$	V_{PVIN} = 12V; V_{LGATE} = 6V	0.5	1	--	A
LGATE Sink	$R_{LGATEsk}$	V_{PVIN} = 12V; V_{LGATE} = 1V	--	3	5	Ω
OC Current Source	I_{OC1}	V_{ISNS} = 0V	34	40	46	μA
Under Voltage Lockout	V_{UV1}		--	75	--	%
COMP1 Enable Threshold	V_{EN1}		0.1	0.2	--	V
PWM2 Controller						
OC current source	I_{OC2}	V_{ISNS2} = 0V	34	40	46	μA
Under Voltage Lockout	V_{UV2}		--	75	--	%
SS2/EN2 Source Current	I_{SS2}	$V_{SS2/EN2}$ = 0V	--	5	--	μA
Enable Threshold	V_{EN2}		--	0.5	--	V
UV Protection Enable Threshold	V_{PT_EN2}	V_{DD} = 5V	--	3.6	--	V
FSB_VTT Regulator						
External Gate Driver	V_{OH3}	V_{PVIN} = 12V	10.5	--	--	V
Gate Source Current	I_{SC3}	V_{VTT_DRV} = 3V	--	4	--	mA
Gate Sink Current	I_{SK3}	V_{VTT_DRV} = 0.6V	15	22	--	mA
Under Voltage Lockout	V_{UV3}		--	75	--	%
3VSB Regulator						
Regulated Voltage	V_{3VSB}		3.2	3.3	3.4	V
Source Current	I_{SC4}		30	40	--	mA
OC Current	I_{OC4}		40	80	--	mA
Under Voltage Lockout	V_{UV4}		--	75	--	%
Others						
$\overline{S3}$, $\overline{S5}$ High Input Threshold	V_{IL}		--	--	0.75	V
$\overline{S3}$, $\overline{S5}$ Low Input Threshold	V_{IH}		2.2	--	--	V
Thermal Shutdown Limit	T_{SHDN}		--	140	--	°C

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution is highly recommended.

Note 3. The device is not guaranteed to function outside its operating conditions.

Note 4. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard. The case point of θ_{JC} is on the expose pad for the QFN package.

Application Information

Overview

The RT9645 integrates two synchronous buck PWM controllers, two LDO controllers, and a dual power switching controller. It is primarily designed for computer applications powered from an ATX power supply.

A 300kHz Synchronous Buck PWM controller with a precision 0.8V reference provides the proper Core voltage to the system main memory.

A second 300kHz PWM Buck controller which requires an external MOSFET driver, provides the GMCH core voltage. One LDO controller regulates for FSB_VTT termination and other one is for the 3VSB power regulation.

RT9645 also provides a dual power control 5VDL for S0 and S3 system power.

Table 1

State	VCC_DRV	SB5V_DRV	5VDL
S5	L	H	Off
S3	L	L	On
S0	H	H	On

State	FSB_VTT	3VSB	VDDQ
S5	Off	On	Off
S3	Off	On	On
S0	On	On	On

ACPI State Transitions

ACPI compliance is realized through the $\overline{S3}$ and $\overline{S5}$ sleep signals. Figure 3 shows how the RT9645 regulators are working during all state transitions.

S5 to S0 Transition

After AC power is plugged, the RT9645 stays in S5 state until the power button is pushed on. The $\overline{S3}$ and $\overline{S5}$ signals transit to HIGH and the +12V rail starts to ramp up. The RT9645 POR is executed as soon as PVIN voltage exceeds the threshold.

In Intel mode, after an internal time delay T_{SS} the VDDQ PWM will enable soft-start sequence and VCC_DRV will change to high. In AMD mode, VDDQ PWM is enabled after VDDQ_EN goes high. FSB_VTT soft-start will follow VDDQ soft-start with a time delay T_{SS} in Intel mode, but in AMD mode FSB_VTT soft-start is triggered by VTT_EN becoming high. After VDDQ rail and the FSB_VTT soft-start completes, all RT9645 regulators work in normal operation. Refer to Figure 3 and Figure 4 for the detailed timing diagrams.

S0 to S3 Transition

When $\overline{S3}$ goes LOW but $\overline{S5}$ still HIGH ,the RT9645 will disable FSB_VTT regulators. SB5V_DRV and VCC_DRV will go low to continually power on 5VDL rail. The memory power V_{DDQ} is also maintained.

S3 to S0 Transition

When $\overline{S3}$ transits from LOW to HIGH with $\overline{S5}$ keeps HIGH and after the PVIN exceeds its POR threshold, in Intel mode the RT9645 will wait a time delay T_{SS} and then soft-starts FSB_VTT LDO. In AMD mode, FSB_VTT will soft-start after VTT_EN goes high.

S0 to S5 Transition

When the system transits from active state to shutdown (S0 to S5) state, the RT9645 keeps powering 3VSB and turn off the other power regulators.

Fault Protection

The RT9645 monitors the VDDQ ,PWM2 and 3VSB regulator for under voltage and over-current protection. The FSB_VTT LDO regulator is monitored for under voltage protection. If RT9645 detects thermal Shutdown, over current (or Under Voltage) of 3VSB, the RT9645 will immediately shutdown all regulators and jump to first system state to redo power sequence.

When VDDQ issues Under Voltage or Over Current or FSB_VTT issues Under Voltage, the RT9645 will immediately enters into $\overline{S5}$ sleep state.This can only be cleared by toggling the S5 signal.

VDDQ and PWM2 Over Current Protection

The RT9645 senses the current flowing through low side MOSFET for over current protection (OCP). A 40μA current source flows through the external resistor R_{OCSET} to PHASE pin causes 40μA x R_{OCSET} voltage drop across the resistor. OCP is triggered if the voltage at PHASE pin (drop of lower MOSFET V_{DS}) is lower than Rocset voltage drop when low side MOSFET conducting. Accordingly inductor current threshold for OCP is a function of conducting resistance of lower MOSFET $R_{DS(ON)}$ as :

$$I_{OCSET} = \frac{40\mu A \times R_{OCSET}}{R_{DS(ON)}}$$

To prevent OC form tripping in normal operation, R_{OCSET} must be carefully chosen with :

1. Maximum $R_{DS(ON)}$ at highest junction temperature

2. Minimum I_{OCSET} from specification table

3. $I_{L(MAX)} > I_{OUT(MAX)} + \Delta I_L / 2$

ΔI_L = inductor ripple current

If Low side MOSFET with $R_{DS(ON)}$ = 6mΩ is used, the OCP threshold current is about 20A. Once OCP is triggered, the RT9645 enters S5 sleep state.

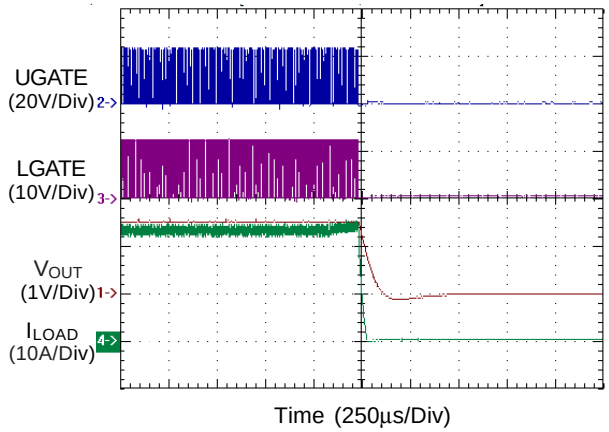


Figure 6. Over Cuuent Protection

Feedback Compensation

Figure 7 highlights the voltage-mode control loop for a synchronous buck converter. Figure 8 shows the corresponding Bode plot. The output voltage (V_{OUT}) is regulated to the reference voltage. The error amplifier EA output (COMP) is compared with the oscillator (OSC) sawtooth wave to provide a pulse-width modulated (PWM) wave with an amplitude of V_{IN} at the PHASE node. The PWM wave is smoothed by the output filter (L and C_{OUT}). The modulator transfer function is the small-signal transfer function of V_{OUT}/COMP. This function is dominated by a DC gain and the output filter (L and C_{OUT}), with a double pole break frequency at F_{P_LC} and a zero at F_{Z_ESR}. The DC gain of the modulator is simply the input voltage (V_{IN}) divided by the peak-to-peak oscillator voltage ΔV_{OSC}. The break frequency F_{LC} and F_{ESR} are expressed as Equation (1) and (2) respectively.

$$F_{P\_LC} = \frac{1}{2\pi\sqrt{LC_{OUT}}} \quad (1)$$

$$F_{Z\_ESR} = \frac{1}{2\pi \times ESR \times C_{OUT}} \quad (2)$$

The compensation network consists of the error amplifier EA and the impedance networks Z_{IN} and Z_{FB}. The goal of the compensation network is to provide a closed loop transfer function with the highest DC gain, the highest 0dB crossing frequency (FC) and adequate phase margin. Typically, FC in range 1/5 to 1/10 of switching frequency is adequate. Higher FC will cause faster dynamic response. A phase margin in the range of 45°C to 60°C is desirable. The equations below relate the compensation network poles, zeros and gain to the components (R1, R2, R3, C1, C2, and C3) in Figure 7.

$$F_{Z1} = \frac{1}{2\pi \times R2 \times C1} \quad (3)$$

$$F_{Z2} = \frac{1}{2\pi \times (R1+R3) \times C3} \quad (4)$$

$$F_{P1} = \frac{1}{2\pi \times R2 \times \frac{C1 \times C2}{C1+C2}} \quad (5)$$

$$F_{P2} = \frac{1}{2\pi \times R3 \times C3} \quad (6)$$

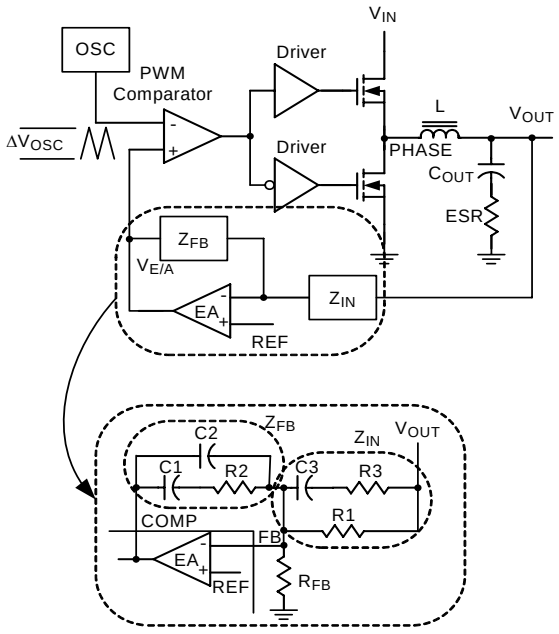


Figure 7

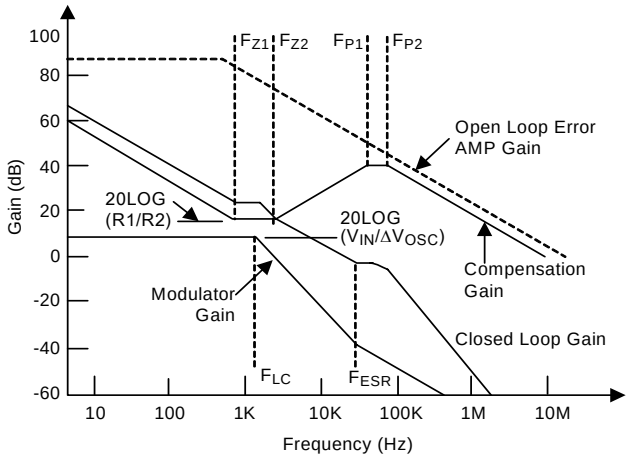


Figure 8

Feedback Loop Design Procedure

Use these guidelines for locating the poles and zeros of the compensation network :

1. Pick Gain (R2/R1) for desired 0dB crossing frequency (FC).
2. Place 1st zero F_{Z1} below modulator double pole F_{LC} (~75% F_{LC}).
3. Place 2nd zero F_{Z2} at modulator double pole F_{LC}.
4. Place 1st pole F_{P1} at the ESR zero F_{Z_ESR}
5. Place 2nd pole F_{P2} at half the switching frequency.
6. Check gain against error amplifier's open-loop gain.
7. Pick R_{FB} for desired output voltage.
8. Estimate phase margin and repeat if necessary.

Component Selection

Components should be appropriately selected to ensure stable operation, fast transient response, high efficiency, minimum BOM cost and maximum reliability.

Output Inductor Selection

The selection of output inductor is based on the considerations of efficiency, output power and operating frequency. For a synchronous buck converter, the ripple current of inductor (%I_L) can be calculated as follows :

$$\Delta I_L = (V_{IN} - V_{OUT}) \times \frac{V_{OUT}}{V_{IN} \times I_{OSC} \times L} \quad (7)$$

Generally, an inductor that limits the ripple current between 20% and 50% of output current is appropriate. Make sure that the output inductor could handle the maximum output current and would not saturate over the operation temperature range.

Output Capacitor Selection

The output capacitors determine the output ripple voltage (%V_{OUT}) and the initial voltage drop after a high slew rate load transient. The selection of output capacitor depends on the output ripple requirement. The output ripple voltage is described as Equation (8).

$$\Delta V_{OUT} = \Delta I_L \times ESR + \frac{1}{8} \times \frac{V_{OUT}}{I_{OSC}^2 \times L \times C_{OUT}} (1 - D) \quad (8)$$

For electrolytic capacitor application, typically 90 to 95% of the output voltage ripple is contributed by the ESR of output capacitors. Paralleling lower ESR ceramic capacitor with the bulk capacitors could dramatically reduce the equivalent ESR and consequently the ripple voltage.

Input Capacitor Selection

Use mixed types of input bypass capacitors to control the input voltage ripple and switching voltage spike across the MOSFETs. The buck converter draws pulsewise current from the input capacitor during the on time of upper MOSFET. The RMS value of ripple current flowing through the input capacitor is described as :

$$I_{IN(RMS)} = I_{OUT} \times \sqrt{D \times (1 - D)}$$

The input bulk capacitor must be cable of handling this ripple current. Sometime, for higher efficiency the low ESR capacitor is necessarily. Appropriate high frequency ceramic capacitors physically near the MOSFETs effectively reduce the switching voltage spikes.

MOSFET Selection of PWM Buck Converter

The selection of MOSFETs is based upon the considerations of $R_{DS(ON)}$, gate driving requirements, and thermal management requirements. The power loss of upper MOSFET consists of conduction loss and switching loss and is expressed as :

$$P_{UPPER} = P_{COND\_UPPER} + P_{SW\_UPPER}$$

$$= I_{OUT}^2 \times R_{DS(ON)} \times D + \frac{1}{2} I_{OUT} \times V_{IN} \times (T_{RISE} + T_{FALL}) \times I_{OSC}$$

where T_{RISE} and T_{FALL} are rising and falling time of V_{DS} of upper MOSFET respectively. $R_{DS(ON)}$ and QG should be simultaneously considered to minimize power loss of upper MOSFET.

The power loss of lower MOSFET consists of conduction loss, reverse recovery loss of body diode, and conduction loss of body diode and is expressed as :

$$P_{LOWER} = P_{COND\_LOWER} + P_{RR} + P_{DIODE}$$
$$= I_{OUT}^2 \times R_{DS(ON)} \times (1-D) + Q_{RR} \times V_{IN} \times f_{OSC}$$
$$+ \frac{1}{2} I_{OUT} \times V_f \times T_{DIODE} \times f_{OSC}$$

where T_{DIODE} is the conducting time of lower body diode. Special control scheme is adopted to minimize body diode conducting time. As a result, the $R_{DS(ON)}$ loss dominates the power loss of lower MOSFET. Use MOSFET with adequate $R_{DS(ON)}$ to minimize power loss and satisfy thermal requirements.

MOSFET Selection of LDO

The main criteria for selection of the LDO pass transistor is package selection for efficient removal of heat. Select a package and heatsink that maintains the junction temperature below the rating with a maximum expected ambient temperature.

The power dissipated in the linear regulator is :

$P_D = I_{OUT(MAX)} \times (V_{IN} - V_{OUT})$

where $I_{OUT(MAX)}$ is the maximum output current and V_{OUT} is the nominal output voltage of LDO.

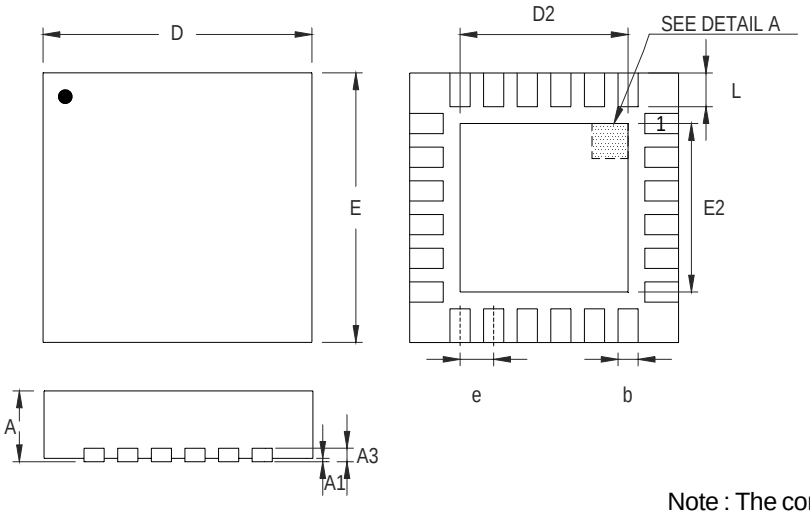
Layout Consideration

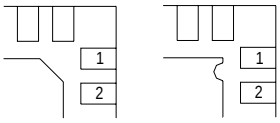
Layout is very important in high frequency switching converter design. If designed improperly, the PCB could radiate excessive noise and contribute to the converter instability. First, place the PWM power stage components. Mount all the power components and connections in the top layer with wide copper areas. The MOSFETs of Buck, inductor, and output capacitor should be as close to each other as possible. This can reduce the radiation of EMI due to the high frequency current loop. If the output capacitors are placed in parallel to reduce the ESR of capacitor, equal sharing ripple current should be considered.

Place the input capacitor directly to the drain of high-side MOSFET. The MOSFETs of linear regulator should have wide pad to dissipate the heat. In multilayer PCB, use one layer as power ground and have a separate control signal ground as the reference of the all signal. To avoid the signal ground is effect by noise and have best load regulation, it should be connected to the ground terminal of output. Furthermore, follows below guide lines can get better performance of IC :

- The IC needs a bypassing ceramic capacitor as a R-C filter to isolate the pulse current from power stage and supply to IC, so the ceramic capacitor should be placed adjacent to the IC.
- Place the high frequency ceramic decoupling close to the power MOSFETs.
- The feedback part should be placed as close to IC as possible and keep away from the inductor and all noise sources.
- The components of bootstraps should be closed to each other and close to MOSFETs.
- The PCB trace from Ug and Lg of controller to MOSFETs should be as short as possible and can carry 1A peak current.
- Place all of the components as close to IC as possible.

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.000	0.031	0.039
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	3.950	4.050	0.156	0.159
D2	2.300	2.750	0.091	0.108
E	3.950	4.050	0.156	0.159
E2	2.300	2.750	0.091	0.108
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

V-Type 24L QFN 4x4 Package

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