Data Sheet | February 18, 2009 | FN6846.0

Adaptive Digital DC-DC Controller with Current Sharing

Description

The ZL2004 is a digital DC-DC controller designed to work with the ZL1505 MOSFET driver IC. Current sharing allows multiple devices to be connected in parallel to source loads with very high current demands. Adaptive performance optimization algorithms improve power conversion efficiency across the entire load range. Zilker Labs Digital-DC™ technology enables a blend of power conversion performance and power management features.

The ZL2004 is designed to be a flexible building block for DC power and can be easily adapted to designs ranging from a single-phase power supply operating from a 4.5 V input to a multi-phase supply operating from a 12V input. The ZL2004 eliminates the need for complicated power supply managers as well as numerous external discrete components.

All operating features can be configured by simple pin-strap/resistor selection or through the SMBus™ serial interface. The ZL2004 uses the PMBus™ protocol for communication with a host controller and the Digital-DC bus for communication between other Zilker Labs devices.

Features

Power Conversion

- Efficient synchronous buck controller
- Adaptive performance optimization algorithms
- 4.5 V to 14 V input range
- 0.54 V to 4 V output range (with margin)
- ± 1% V_{OUT} set-point accuracy
- Fast load transient response
- Current sharing and phase interleaving
- Digitally adjustable current sense range
- *Snapshot*™ parameter capture
- RoHS compliant (5 x 5 mm) QFN package

Power Management

- Digital soft start/stop
- Precision delay and ramp-up
- Power good/enable
- Voltage tracking, sequencing and margining
- Voltage/current/temperature monitoring
- SMBus communication (PMBus compliant)
- Output voltage and current protection
- Internal non-volatile memory (NVM)

Applications

- Servers / storage equipment
- Telecom / datacom equipment
- Power supplies (memory, DSP, ASIC, FPGA)

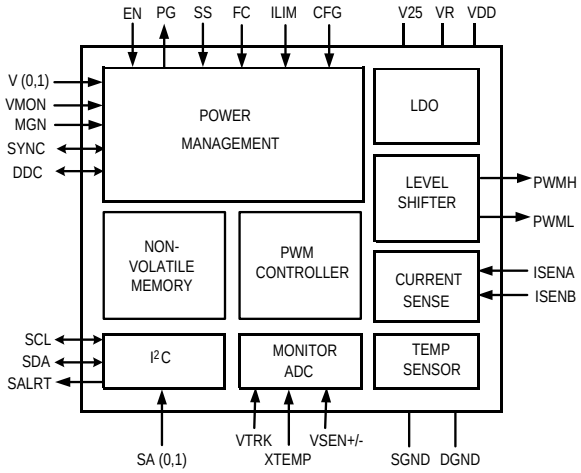


Figure 1. Block Diagram

Table of Contents

1. Electrical Characteristics

Table 1. Absolute Maximum Ratings

Operating beyond these limits may cause permanent damage to the device. Functional operation beyond the Recommended Operating Conditions is not implied. Voltage measured with respect to SGND.

Parameter	Pin(s)	Value	Unit
DC supply voltage	VDD	-0.3 to 17	V
Logic I/O voltage	CFG, DDC, EN, FC, ILIM, MGN, PG, SA(0,1), SALRT, SCL, SDA, SS, SYNC, VMON, V(0,1)	-0.3 to 6.5	V
Analog input voltages	VSEN+, VSEN-, VTRK, XTEMP	-0.3 to 6.5	V
	ISENA, ISENB	-1.5 to 6.5	V
MOSFET drive reference	VR	-0.3 to 6.5	V
Logic reference	V25	-0.3 to 3	V
Ground voltage differential (V_{DGND}-V_{SGND})	DGND, SGND	-0.3 to +0.3	V
Junction temperature	–	-55 to 150	°C
Storage temperature range	–	-55 to 150	°C
Lead temperature (soldering, 10 s)	All	300	°C

Table 2. Recommended Operating Conditions and Thermal Information

Parameter	Symbol	Min	Typ	Max	Unit
Input Supply Voltage Range	V_{DD}	4.5	–	14	V
Output Voltage Range (Inductor sensing)[1]	V_{OUT}	0.54		4.0	V
Operating Junction Temperature Range	T_J	-40	–	125	°C
Junction to Ambient Thermal Impedance[2]	Θ_{JA}	–	35	–	°C/W
Junction to Case Thermal Impedance[3]	Θ_{JC}	–	5	–	°C/W

Notes:

1. Includes margin limits.

2. Θ_{JA} is measured in free air with the device mounted on a multi-layer FR4 test board and the exposed metal pad soldered to a low impedance ground plane using multiple vias.

3. For Θ_{JC}, the “case” temperature is measured at the center of the exposed metal pad.

Table 3. Electrical Specifications

V_{DD} = 12 V, T_A = -40°C to 85°C unless otherwise noted. Typical values are at T_A = 25°C.

Parameter	Conditions	Min	Typ	Max	Unit
Input and Supply Characteristics					
I_{DD} supply current at f_{SW} = 200 kHz I_{DD} supply current at f_{SW} = 1.4 MHz	GH no load, GL no load, MISC_CONFIG[7] = 1	– –	16 25	30 50	mA mA
I_{DDS} shutdown current	EN = 0 V, No I^2C/SMBus activity	–	6.5	8	mA
VR reference output voltage	V_{DD} > 6 V, I_{VR} < 50 mA	4.5	5.2	5.5	V
V25 reference output voltage	V_R > 3 V, I_{V25} < 50 mA	2.25	2.5	2.75	V
Output Characteristics					
Output voltage adjustment range[1]	V_{IN} > V_{OUT}	0.6	–	3.6	V
Output voltage set-point resolution	Set using resistors	–	10	–	mV
	Set using I^2C/SMBus	–	±0.025	–	% FS[2]
Output voltage accuracy [3]	Includes line, load, temp	- 1	–	1	%
VSEN input bias current	VSEN = 4 V	–	80	150	µA
Current sense differential input voltage (V_{OUT} referenced)	V_{ISENA} - V_{ISENB}	- 50	–	50	mV
Current sense input bias current (V_{OUT} referenced, V_{OUT} <= 3.6V)	ISENA	- 1	–	1	µA
	ISENB	- 100	–	100	µA
Soft start delay duration range	Set using SS pin or resistor	2	–	20	ms
	Set using I^2C/SMBus	0.002	–	500	s
Soft start delay duration accuracy	Turn-on delay (precise mode) [4,5] Turn-on delay (normal mode) [6] Turn-off delay [6]	– – –	±0.25 -0.25/+4 -0.25/+4	– – –	ms ms ms
Soft start ramp duration range	Set using SS pin or resistor	2	–	20	ms
	Set using I^2C	0	–	200	ms
Soft start ramp duration accuracy		–	100	–	µs
Logic Input/Output Characteristics					
Logic input bias current	EN,PG,SCL,SDA,SALRT pins	- 10	–	10	µA
MGN input bias current		- 1	–	1	mA
Logic input low, V_{IL}		–	–	0.8	V
Logic input OPEN (N/C)	Multi-mode logic pins	–	1.4	–	V
Logic input high, V_{IH}		2.0	–	–	V
Logic output low, V_{OL}	$I_{OL} \leq$ 4 mA	–	–	0.4	V
Logic output high, V_{OH}	$I_{OH} \geq$ -2 mA	2.25	–	–	V

Notes:
1. Set point adjustment range does not include margin limits.
2. Percentage of Full Scale (FS) with temperature compensation applied.
3. V_{OUT} set-point measured at the termination of the VSEN+ and VSEN- sense points.
4. The device requires approximately 2 ms following an enable signal and prior to ramping its output. The delay accuracy will vary by ±0.25 ms around the 2 ms minimum delay value.
5. Precise ramp timing mode is only valid when using EN pin to enable the device rather than PMBus enable.
6. The devices may require up to a 4 ms delay following an assertion of the enable signal (normal mode) or following the de-assertion of the enable signal.

Table 3. Electrical Characteristics (continued)

V_{DD} = 12 V, T_A = -40°C to 85°C unless otherwise noted. Typical values are at T_A = 25°C.

Parameter	Conditions	Min	Typ	Max	Unit
Oscillator and Switching Characteristics					
Switching frequency range		200	–	1400	kHz
Switching frequency set-point accuracy		- 5	–	5	%
Maximum PWM duty cycle	Factory default	95	–	–	%
Minimum SYNC pulse width		150	–	–	ns
Input clock frequency drift tolerance	External clock source	- 13	–	13	%
Tracking					
VTRK input bias current	VTRK = 4.0 V	–	110	200	µA
VTRK tracking ramp accuracy	100% Tracking, V_{OUT} - VTRK	- 100	–	+ 100	mV
VTRK regulation accuracy	100% Tracking, V_{OUT} - VTRK	- 1	–	1	%
Fault Protection Characteristics					
UVLO threshold range	Configurable via I^2C/SMBus	2.85	–	16	V
UVLO set-point accuracy		- 150	–	150	mV
UVLO hysteresis	Factory default	–	3	–	%
	Configurable via I^2C/SMBus	0	–	100	%
UVLO delay		–	–	2.5	µs
Power good V_{OUT} low threshold	Factory default	–	90	–	% V_{OUT}
Power good V_{OUT} high threshold	Factory default	–	115	–	% V_{OUT}
Power good V_{OUT} hysteresis	Factory default	–	5	–	%
Power good delay	Using pin-strap or resistor [7]	2	–	20	ms
	Configurable via I^2C/SMBus	0	–	500	s
VSEN undervoltage threshold	Factory default	–	85	–	% V_{OUT}
	Configurable via I^2C/SMBus	0	–	110	% V_{OUT}
VSEN overvoltage threshold	Factory default	–	115	–	% V_{OUT}
	Configurable via I^2C/SMBus	0	–	115	% V_{OUT}
VSEN undervoltage hysteresis		–	5	–	% V_{OUT}
VSEN undervoltage/ overvoltage fault response time	Factory default	–	16	–	µs
	Configurable via I^2C/SMBus	5	–	60	µs
Current limit set-point accuracy (V_{OUT} referenced)		–	±10	–	% FS[8]
Current limit protection delay	Factory default	–	5	–	t_{SW} [9]
	Configurable via I^2C/SMBus	1	–	32	t_{SW} [9]
Temperature compensation of current limit protection threshold	Factory default		4400		ppm / °C
	Configurable via I^2C/SMBus	100		12700	
Thermal protection threshold (junction temperature)	Factory default	–	125	–	°C
	Configurable via I^2C/SMBus	- 40	–	125	°C
Thermal protection hysteresis		–	15	–	°C

Notes: 7. Factory default Power Good delay is set to the same value as the soft start ramp time.

8. Percentage of Full Scale (FS) with temperature compensation applied.

9. $t_{SW} = 1/f_{SW}$, where f_{SW} is the switching frequency.

2. Pin Descriptions

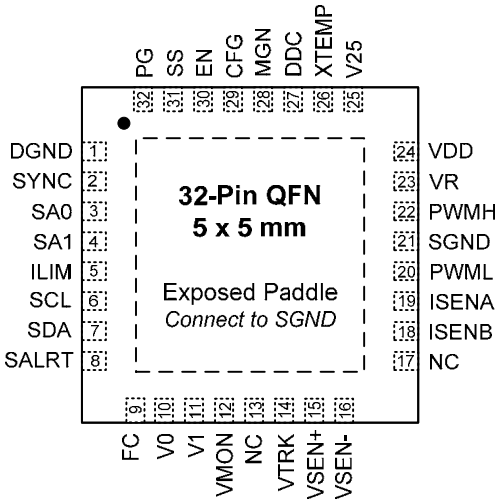


Figure 2. ZL2004 Pin Configurations (top view)

Table 4. Pin Descriptions

Pin	Label	Type[1]	Description
1	DGND	PWR	Digital ground. Connect to low impedance ground plane.
2	SYNC	I/O, M[2]	Clock synchronization input. Used to set the frequency of the internal switch clock, to sync to an external clock or to output internal clock.
3	SA0	I, M	Serial address select pins. Used to assign unique address for each individual device or to enable certain management features.
4	SA1		
5	ILIM	I, M	Current limit select. Sets the overcurrent threshold voltage for ISENA, ISENB.
6	SCL	I/O	Serial clock. Connect to external host and/or to other ZL devices.
7	SDA	I/O	Serial data. Connect to external host and/or to other ZL devices.
8	SALRT	O	Serial alert. Connect to external host if desired.
9	FC	I	Loop compensation selection pin.
10	V0	I, M	Output voltage selection pins. Used to set V_{OUT} set-point and V_{OUT} max.
11	V1		
12	VMON	I, M	External voltage monitoring (Can be used for external driver bias monitoring for Power good).
13	NC		No Connect.
14	VTRK	I	Tracking sense input. Used to track an external voltage source.
15	VSEN+	I	Differential Output voltage sense feedback. Connect to positive output regulation point.
16	VSEN-	I	Differential Output voltage sense feedback. Connect to negative output regulation point.
17	NC		No Connect.
18	ISENB	I	Differential voltage input for current sensing.
19	ISENA	I	Differential voltage input for current sensing. High voltage (DCR).

Table 4. Pin Descriptions (continued)

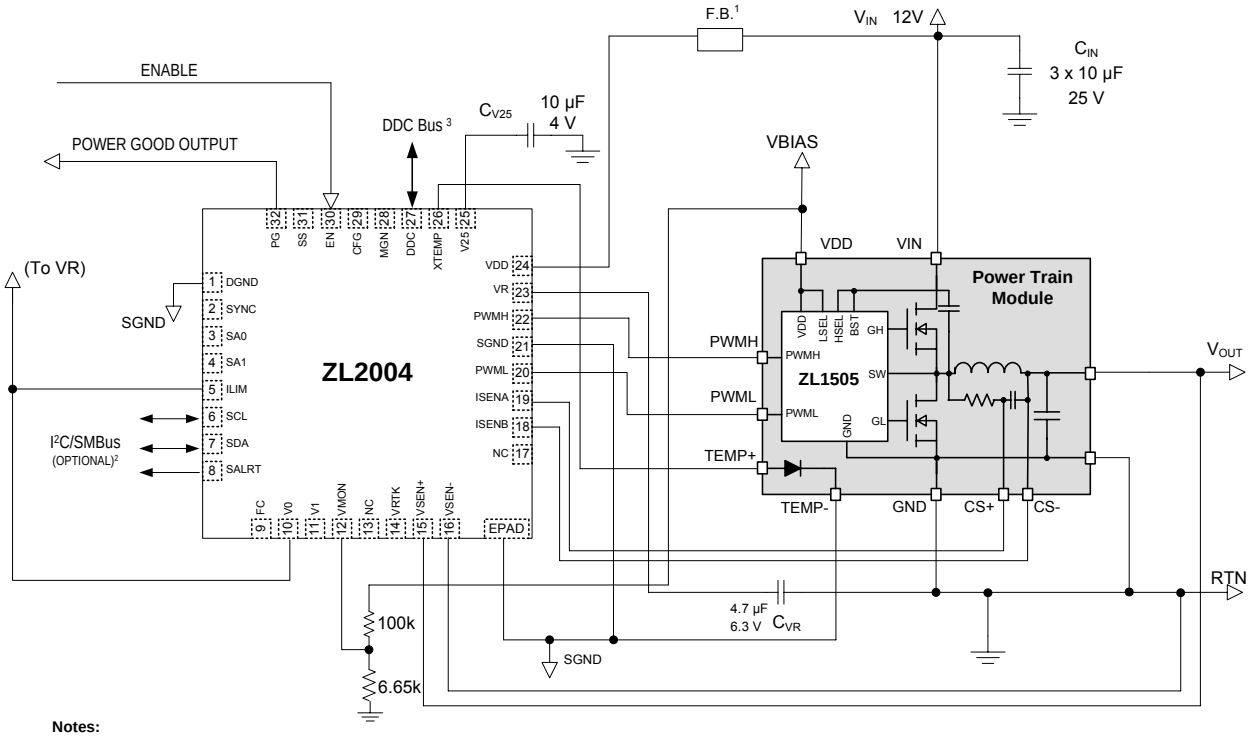
Pin	Label	Type[1]	Description
20	PWML	O	PWM Gate low signal.
21	SGND	PWR	Connect to low impedance ground plane. Internal connection to SGND.
22	PWMH	O	PWM Gate High signal.
23	VR	PWR	Internal 5V reference used to power internal drivers.
24	VDD[3]	PWR	Supply voltage.
25	V25	PWR	Internal 2.5 V reference used to power internal circuitry.
26	XTEMP	I	External temperature sensor input. Connect to external 2N3904 (Base Emitter junction).
27	DDC	I	Single wire DDC bus (Current sharing, inter device communication).
28	MGN	I	V_{OUT} margin control.
29	CFG	M	Configuration pin. Used to control the switching phase offset, sequencing and other management features.
30	EN	I	Enable. Active signal enables PWM switching.
31	SS	I, M	Soft start delay and ramp select. Sets the delay from when EN is asserted until the output voltage starts to ramp and the ramp time.
32	PG	O	Power good output.
EPAD	SGND	PWR	Exposed thermal pad. Connect to low impedance ground plane. Internal connection to SGND.

Notes:

1. I = Input, O = Output, PWR = Power or Ground. M = Multi-mode pins. (Refer to page 11).
2. The SYNC pin can be used as a logic pin, a clock input or a clock output.
3. V_{DD} is measured internally and the value is used to modify the PWM loop gain.

3. Typical Application Circuit

The following application circuit represents a typical implementation of the ZL2004.



Notes:
1. Ferrite bead is optional for input noise suppression.
2. The I²C/SMBus requires pull-up resistors. Please refer to the I²C/SMBus specifications for more details.
3. The DDC bus requires a pull-up resistor. The resistance will vary based on the capacitive loading of the bus (and on the number of devices connected). The 10 kΩ default value, assuming a maximum of 100 pF per device, provides the necessary 1 µs pull-up rise time. Please refer to section 6.11 for more details.

Figure 3. 12 V to 1.8 V / 20 A Application Circuit (4.5 V UVLO, 5 ms SS delay, 5 ms SS ramp)

4. ZL2004 Overview

4.1 Digital-DC Architecture

The ZL2004 is an innovative mixed-signal power conversion and power management IC based on Zilker Labs' patented Digital-DC technology that provides an integrated, high performance step-down converter for a wide variety of power supply applications.

Today's embedded power systems are typically designed for optimal efficiency at maximum load, reducing the peak thermal stress by limiting the total thermal dissipation inside the system. Unfortunately, many of these systems are often operated at load levels far below the peak where the power system has been optimized, resulting in reduced efficiency. While this may not cause thermal stress to occur, it does contribute to higher electricity usage and results in higher overall system operating costs.

Zilker Labs' efficiency-adaptive ZL2004 DC-DC controller helps mitigate this scenario by enabling the power converter to automatically change their operating state to increase efficiency and overall performance with little or no user interaction needed.

Its unique digital PWM loop utilizes an innovative mixed-signal topology to enable precise control of the power conversion process with no software required, resulting in a very flexible device that is also easy to use. An extensive set of power management functions is fully integrated and can be configured using simple pin connections or via the I^2C/SMBus hardware interface using standard PMBus commands. The user configuration can be saved in an on-chip non-volatile memory (NVM), allowing ultimate flexibility.

Once enabled, the ZL2004 is immediately ready to regulate power and perform power management tasks with no programming required. The ZL2004 can be configured by simply connecting its pins according to the tables provided in this document. Advanced configuration options and real-time configuration changes are available via the I^2C/SMBus interface if desired, and continuous monitoring of multiple operating parameters is possible with minimal interaction from a host controller. Integrated sub-regulation circuitry enables single supply operation from any supply between 4.5 V and 14 V with no secondary bias supplies needed.

Zilker Labs provides a comprehensive set of application notes to assist with power supply design and simulation. An evaluation board is also available to help the user become familiar with the device. This board can be evaluated as a stand-alone platform using pin configuration settings. Additionally, a Windows™-based GUI is provided to enable full configuration and monitoring capability via the I^2C/SMBus interface using an available computer and the included USB cable.

Please refer to www.zilkerlabs.com for access to the most up-to-date documentation or call your local Zilker Labs' sales office to order an evaluation kit.

4.2 Power Conversion Overview

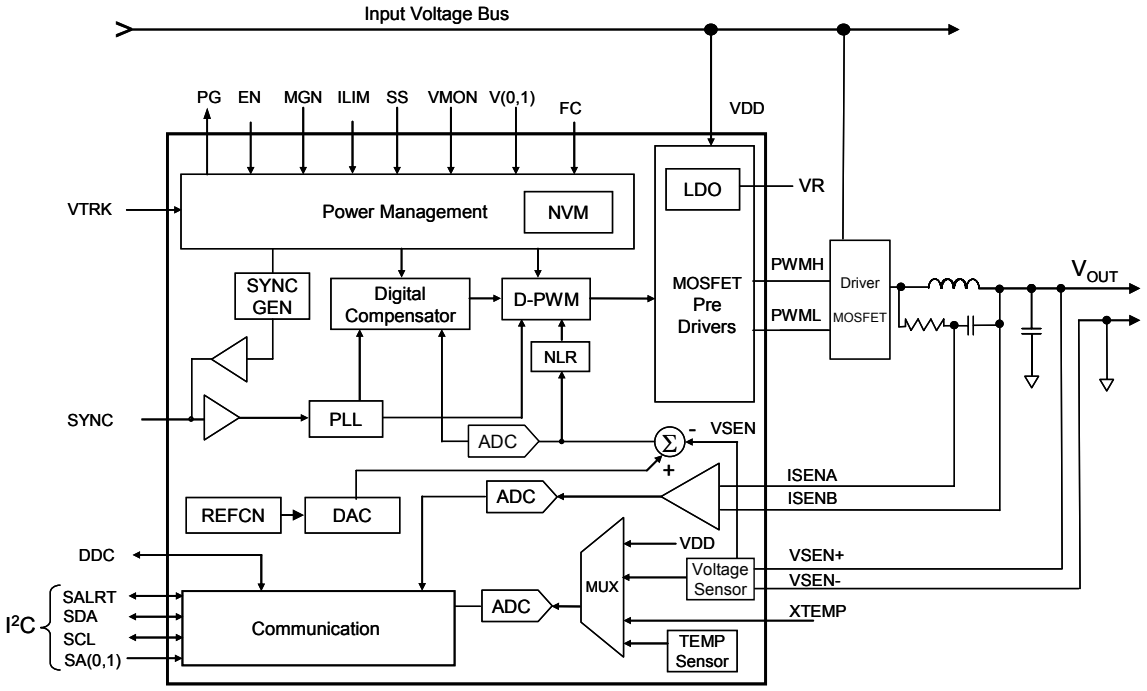


Figure 4. ZL2004 Block Diagram

The ZL2004 operates as a voltage-mode, synchronous buck converter with a selectable constant frequency pulse width modulator (PWM) control scheme that uses external driver, MOSFETs, capacitors, and an inductor to perform power conversion.

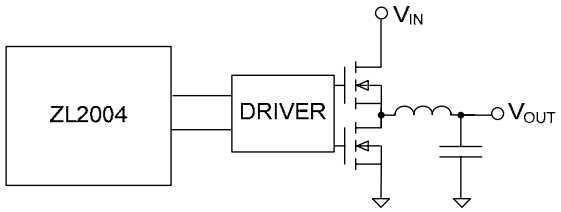


Figure 5. Synchronous Buck Converter

Figure 5 illustrates the basic synchronous buck converter topology showing the primary power train components. This converter is also called a step-down converter, as the output voltage must always be lower than the input voltage.

Dual output PWM ZL2004

The ZL2004 provides a dual PWM signal which removes the need of a tri-state function and significantly improves conversion performance.

The ZL2004 has been designed to drive the QH and QL independently, allowing greater control of the MOSFETs and higher overall performance. A special driver with two PWM inputs is required (ZL1505). Using two PWM signals (PWMH and PWML) offers more options during fault event and pre-bias conditions, eliminating the need for a tri-state driver and reducing the delays associated with this scheme.

The ZL2004 has several features to improve the power conversion efficiency. A non-linear response (NLR) loop improves the response time and reduces the output deviation as a result of a load transient. The ZL2004 monitors the power converter's operating conditions and continuously adjusts the turn-on and turn-off timing of the high-side and low-side MOSFETs to optimize the overall efficiency of the power supply. Adaptive performance optimization algorithms such as dead-time control, diode emulation,

and adaptive frequency are available to provide greater efficiency improvement.

The ZL2004 can also be used with a single-ended MOSFET driver. Simple parameter changes allow the device to use a single PWM to drive the logic input of such drivers. The trade-offs for using this mode may include reduced efficiency, reduced ramp-up timing accuracy, and degraded pre-bias protection.

4.3 Power Management Overview

The ZL2004 incorporates a wide range of configurable power management features that are simple to implement with no external components. Additionally, the ZL2004 includes circuit protection features that continuously safeguard the device and load from damage due to unexpected system faults. The ZL2004 can continuously monitor input voltage, output voltage/current, internal temperature, and the temperature of an external thermal diode. A Power Good output signal is also included to enable power-on reset functionality for an external processor.

All power management functions can be configured using either pin configuration techniques (see Figure 6) or via the I^2C/SMBus interface. Monitoring parameters can also be pre-configured to provide alerts for specific conditions. See Application Note AN33 for more details on SMBus monitoring.

4.4 Multi-mode Pins

In order to simplify circuit design, the ZL2004 incorporates patented multi-mode pins that allow the user to easily configure many aspects of the device with no programming. Most power management features can be configured using these pins. The multi-mode pins can respond to four different connections as shown in Table 5. These pins are sampled when power is applied or by issuing a PMBus Restore command (See Application Note AN33).

Pin-strap Settings: This is the simplest implementation method, as no external components are required. Using this method, each pin can take on one of three possible states: LOW, OPEN, or HIGH. These pins can be connected to the V25 pin for logic HIGH settings as this pin provides a regulated voltage higher than 2 V. Using a single pin, one of three settings can be selected. Using two pins, one of nine settings can be selected.

Table 5. Multi-mode Pin Configuration

Pin Tied To	Value
LOW (Logic LOW)	< 0.8 VDC
OPEN (N/C)	No connection
HIGH (Logic HIGH)	> 2.0 VDC
Resistor to SGND	Set by resistor value

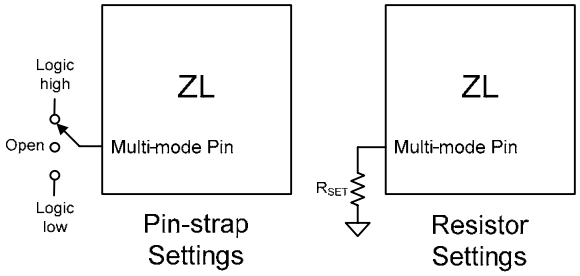


Figure 6. Pin-strap and Resistor Setting Examples

Resistor Settings: This method allows a greater range of adjustability when connecting a finite value resistor (in a specified range) between the multi-mode pin and SGND. Standard 1% resistor values are used, and only every fourth E96 resistor value is used so the device can reliably recognize the value of resistance connected to the pin while eliminating the error associated with the resistor accuracy. Up to 31 unique selections are available using a single resistor.

I^2C/SMBus Method: Almost any ZL2004 function can be configured via the I^2C/SMBus interface using standard PMBus commands. Additionally, any value that has been configured using the pin-strap or resistor setting methods can also be re-configured and/or verified via the I^2C/SMBus. See Application Note AN33 for more details.

The SMBus device address and VOUT_MAX are the only parameters that must be set by external pins. All other device parameters can be set via the I^2C/SMBus. The device address is set using the SA0 and SA1 pins. VOUT_MAX is determined as 10% greater than the voltage set by the V0 and V1 pins.

5. Power Conversion Functional Description

5.1 Internal Bias Regulators and Input Supply Connections

The ZL2004 employs two internal low dropout (LDO) regulators to supply bias voltages for internal circuitry, allowing it to operate from a single input supply. The internal bias regulators are as follows:

VR: The VR LDO provides a regulated 5 V bias supply for the MOSFET pre-driver circuits. It is powered from the VDD pin. A 4.7 µF filter capacitor is required at the VR pin.

V25: The V25 LDO provides a regulated 2.5 V bias supply for the main controller circuitry. It is powered from an internal 5 V node. A 10 µF filter capacitor is required at the V25 pin.

When the input supply (VDD) is higher than 5.5 V, the VR pin should not be connected to any other pins. It should only have a filter capacitor attached as shown in Figure 7. Due to the dropout voltage associated with the VR bias regulator, the VDD pin must be connected to the VR pin for designs operating from a supply below 5.5 V. Figure 7 illustrates the required connections for both cases.

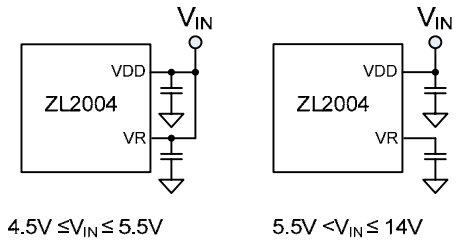


Figure 7. Input Supply Connections

Note: the internal bias regulators are not designed to be outputs for powering other circuitry. Do not attach external loads to any of these pins. The multi-mode pins may be connected to the V25 pin for logic HIGH settings.

5.2 Output Voltage Selection

Standard Mode

The output voltage may be set to any voltage between 0.6 V and 3.6 V provided that the input voltage is higher than the desired output voltage by an amount sufficient to prevent the device from exceeding its maximum duty cycle specification. Using the pin-strap method, V_{OUT} can be set to any of nine standard voltages as shown in Table 6.

Table 6. Pin-strap Output Voltage Settings

		V0		
		LOW	OPEN	HIGH
V1	LOW	0.6 V	0.8 V	1.0 V
	OPEN	1.2 V	1.5 V	1.8 V
	HIGH	2.5 V	3.3 V	3.6 V

The resistor setting method can be used to set the output voltage to levels not available in Table 6. Resistors R0 and R1 are selected to produce a specific voltage between 0.6 V and 3.6 V in 10 mV steps. Resistor R1 provides a coarse setting and resistor R0 provides a fine adjustment, thus eliminating the additional errors associated with using two 1% resistors (this typically adds 1.4% error).

To set V_{OUT} using resistors, follow the steps below to calculate an index value and then use Table 7 to select the resistor that corresponds to the calculated index value as follows:

1. Calculate Index1:
   Index1 = 4 x V_{OUT} (V_{OUT} in 10 mV steps)
2. Round the result down to the nearest whole number.
3. Select the value of R1 from Table 7 using the Index1 rounded value from step 2.
4. Calculate Index0:
   Index0 = 100 x V_{OUT} – (25 x Index1)
5. Select the value of R0 from Table 7 using the Index0 value from step 4.

Table 7. Resistors for Setting Output Voltage

Index	R0 or R1
0	10 kΩ
1	11 kΩ
2	12.1 kΩ
3	13.3 kΩ
4	14.7 kΩ
5	16.2 kΩ
6	17.8 kΩ
7	19.6 kΩ
8	21.5 kΩ
9	23.7 kΩ
10	26.1 kΩ
11	28.7 kΩ
12	31.6 kΩ

Index	R0 or R1
13	34.8 kΩ
14	38.3 kΩ
15	42.2 kΩ
16	46.4 kΩ
17	51.1 kΩ
18	56.2 kΩ
19	61.9 kΩ
20	68.1 kΩ
21	75 kΩ
22	82.5 kΩ
23	90.9 kΩ
24	100 kΩ

Example from Figure 8: For V_{OUT} = 1.33 V,

Index1 = 4 x 1.33 V = 5.32;
From Table 7, R1 = 16.2 kΩ

Index0 = (100 x 1.33 V) – (25 x 5) = 8;
From Table 7, R0 = 21.5 kΩ

The output voltage may also be set to any value between 0.6 V and 3.6 V using the I^2C interface. See Application Note AN33 for details.

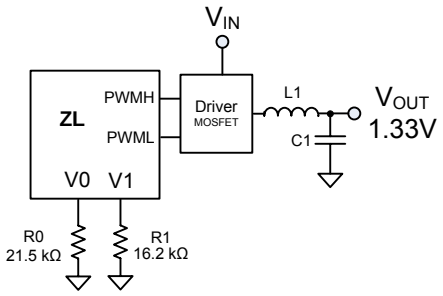


Figure 8. Output Voltage Resistor Setting Example

POLA Voltage Trim Mode

The output voltage mapping can be changed to match the voltage setting equations for POLA (*Point of Load Alliance*) and DOSA (*Distributed-power Open Standards Alliance*) standard modules.

The standard method for adjusting the output voltage for a POLA module is defined by the following equation:

$$R_{SET} = 10k\Omega \times \frac{0.69V}{V_{out} - 0.69V} - 1.43k\Omega$$

The resistor, R_{SET}, is external to the POLA module. See Figure 9.

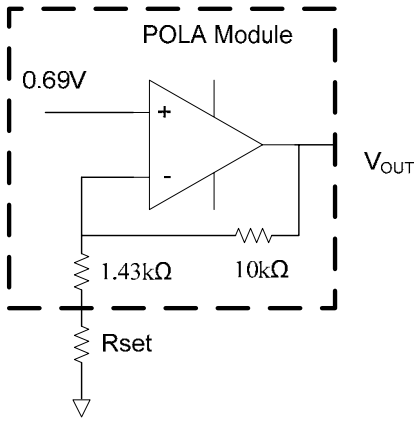


Figure 9. Output Voltage Setting on POLA Module

To stay compatible with this existing method for adjusting the output voltage and to keep the same external R_{SET} resistor when using the ZL2004, the module manufacturer should add a 10 kΩ resistor on the module as shown in Figure 10. Now, the same R_{SET} used for an analog POLA module will provide the same output voltage when using a digital POLA module based on the ZL2004.

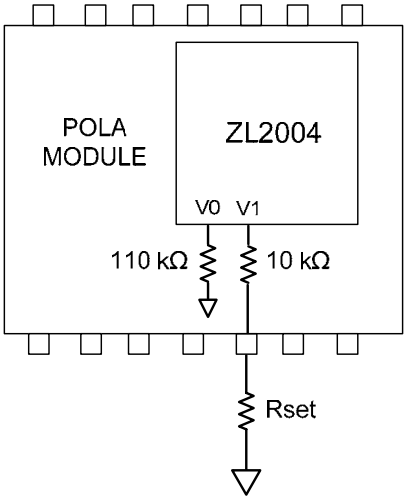


Figure 10. R_{SET} on a POLA Module

The POLA mode is activated through pin-strap by connecting a 110 kΩ resistor on V0 to SGND. The V1 pin is then used to adjust the output voltage as shown in Table 8.

The POLA mode can also be activated through PMBus commands. See Application Note AN33 for more details.

Table 8. POLA Mode V_{OUT} Settings
($R0 = 110\ k\Omega$, $R1 = R_{SET} + 10\ k\Omega$)

V_{OUT}	R_{SET} In series with 10kΩ resistor	V_{OUT}	R_{SET} In series with 10kΩ resistor
0.700 V	162 kΩ	0.991 V	21.5 kΩ
0.752 V	110 kΩ	1.000 V	19.6 kΩ
0.758 V	100 kΩ	1.100 V	16.2 kΩ
0.765 V	90.9 kΩ	1.158 V	13.3 kΩ
0.772 V	82.5 kΩ	1.200 V	12.1 kΩ
0.790 V	75.0 kΩ	1.250 V	9.09 kΩ
0.800 V	56.2 kΩ	1.500 V	7.50 kΩ
0.821 V	51.1 kΩ	1.669 V	5.62 kΩ
0.834 V	46.4 kΩ	1.800 V	4.64 kΩ
0.848 V	42.2 kΩ	2.295 V	2.87 kΩ
0.880 V	34.8 kΩ	2.506 V	2.37 kΩ
0.899 V	31.6 kΩ	3.300 V	1.21 kΩ
0.919 V	28.7 kΩ	3.600 V	0.909 kΩ
0.965 V	23.7 kΩ		

DOSA Voltage Trim Mode

On a DOSA module, the V_{OUT} setting follows this equation:

$$R_{SET} = \frac{6900}{V_{out} - 0.69V}$$

To maintain DOSA compatibility, the same scheme is used as with a POLA module except the 10 kΩ resistor is replaced with an 8.66 kΩ resistor as shown in Figure 11.

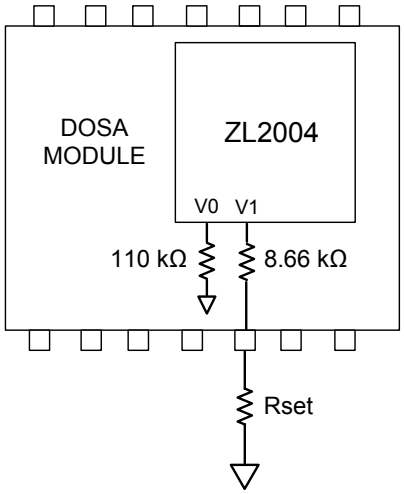


Figure 11. R_{SET} on a DOSA Module

The DOSA mode V_{OUT} settings are listed in Table 9.

Table 9. DOSA Mode V_{OUT} Settings
($R0 = 110\ k\Omega$, $R1 = R_{SET} + 8.66\ k\Omega$)

V_{OUT}	R_{SET} In series with 8.66kΩ resistor	V_{OUT}	R_{SET} In series with 8.66kΩ resistor
0.700 V	162 kΩ	0.991 V	22.6 kΩ
0.752 V	113 kΩ	1.000 V	21.0 kΩ
0.758 V	100 kΩ	1.100 V	17.8 kΩ
0.765 V	90.9 kΩ	1.158 V	14.7 kΩ
0.772 V	82.5 kΩ	1.200 V	13.3 kΩ
0.790 V	75.0 kΩ	1.250 V	10.5 kΩ
0.800 V	57.6 kΩ	1.500 V	8.87 kΩ
0.821 V	52.3 kΩ	1.669 V	6.98 kΩ
0.834 V	47.5 kΩ	1.800 V	6.04 kΩ
0.848 V	43.2 kΩ	2.295 V	4.32 kΩ
0.880 V	36.5 kΩ	2.506 V	3.74 kΩ
0.899 V	33.2 kΩ	3.300 V	2.61 kΩ
0.919 V	30.1 kΩ	3.600 V	1.50 kΩ
0.965 V	25.5 kΩ		

5.3 Start-up Procedure

The ZL2004 follows a specific internal start-up procedure after power is applied to the VDD pin. Table 10 describes the start-up sequence.

If the device is to be synchronized to an external clock source, the clock frequency must be stable prior to asserting the EN pin. The device requires approximately 5-10 ms to check for specific values stored in its internal memory. If the user has stored values in memory, those values will be loaded. The device will then check the status of all multi-mode pins and load the values associated with the pin settings.

Once this process is completed, the device is ready to accept commands via the I^2C/SMBus interface and the device is ready to be enabled. Once enabled, the device requires approximately 2 ms before its output voltage may be allowed to start its ramp-up process. If a soft-start delay period less than 2 ms has been configured (using PMBus commands), the device will default to a 2 ms delay period (with an accuracy of approx ±0.25 ms). If a delay period greater than 2 ms is configured, the device will wait for the configured delay period prior to starting to ramp its output.

After the delay period has expired, the output will begin to ramp towards its target voltage according to the pre-configured soft-start ramp time that has been set using the SS pin.

5.4 Soft Start Delay and Ramp Times

Soft Start Delay and Ramp Times

In some applications, it may be necessary to set a delay from when an enable signal is received until the output voltage starts to ramp to its target value. In addition, the designer may wish to precisely set the time required for V_{OUT} to ramp to its target value after the delay period has expired. These features may be used as part of an overall inrush current management strategy or to precisely control how fast a load IC is turned on. The ZL2004 gives the system designer several options for precisely and independently controlling both the delay and ramp time periods.

The soft-start delay period begins when the EN pin is asserted and ends when the delay time expires. The soft-start delay period is set using the SS pin.

The soft-start ramp timer enables a precisely controlled ramp to the nominal V_{OUT} value that begins once the delay period has expired. The ramp-up is guaranteed monotonic and its slope may be precisely set using the SS pin.

The soft start delay and ramp times can be set to standard values according to Table 11.

Table 10. ZL2004 Start-up Sequence

Step #	Step Name	Description	Time Duration
1	Power Applied	Input voltage is applied to the ZL2004's VDD pin	Depends on input supply ramp time
2	Internal Memory Check	The device will check for values stored in its internal memory. This step is also performed after a Restore command.	Approx 5-10 ms (device will ignore an enable signal or PMBus traffic during this period)
3	Multi-mode Pin Check	The device loads values configured by the multi-mode pins.	
4	Device Ready	The device is ready to accept an enable signal.	—
5	Pre-ramp Delay	The device requires approximately 2 ms following an enable signal and prior to ramping its output. Additional pre-ramp delay may be configured using the Delay pins.	Approximately 2 ms

Table 11. Soft Start Ramp Settings

R_{SS}	SS Delay	SS Ramp	UVLO
LOW	2 ms	2 ms	4.5 V
OPEN	5 ms	5 ms	
HIGH	10 ms	10 ms	
10 kΩ	2 ms	2 ms	4.5 V
11 kΩ		5 ms	
12.1 kΩ		10 ms	
13.3 kΩ	5 ms	2 ms	
14.7 kΩ		5 ms	
16.2 kΩ		10 ms	
17.8 kΩ		20 ms	
19.6 kΩ	10 ms	2 ms	
21.5 kΩ		5 ms	
23.7 kΩ		10 ms	
26.1 kΩ		20 ms	
28.7 kΩ	20 ms	2 ms	
31.6 kΩ		5 ms	
34.8 kΩ		10 ms	
38.3 kΩ		20 ms	
42.2 kΩ	2 ms	2 ms	10.8 V
46.4 kΩ		5 ms	
51.1 kΩ		10 ms	
56.2 kΩ		20 ms	
61.9 kΩ	5 ms	2 ms	
68.1 kΩ		5 ms	
75 kΩ		10 ms	
82.5 kΩ		20 ms	
90.9 kΩ	10 ms	2 ms	
100 kΩ		5 ms	
110 kΩ		10 ms	
121 kΩ		20 ms	
133 kΩ	20 ms	2 ms	
147 kΩ		5 ms	
162 kΩ		10 ms	
178 kΩ		20 ms	

The value of this resistor is measured upon start-up or Restore and will not change if the resistor is varied after power has been applied to the ZL2004. See Figure 12 for typical connections using resistors.

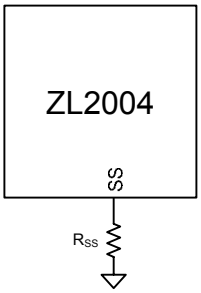


Figure 12. SS Pin Resistor Connections

If the desired soft start delay and ramp times are not one of the values listed in Table 11, the times can be set to a custom value via the I^2C/SMBus interface. When the SS delay time is set to 0 ms, the device will begin its ramp after the internal circuitry has initialized (approx. 2 ms). The soft-start ramp period may be set to values less than 2 ms, however it is generally recommended to set the soft-start ramp to a value greater than 500 µs to prevent inadvertent fault conditions due to excessive inrush current.

5.5 Power Good

The ZL2004 provides a Power Good (PG) signal that indicates the output voltage is within a specified tolerance of its target level and no fault condition exists. By default, the PG pin will assert if the output is within -10%/+15% of the target voltage. These limits and the polarity of the pin may be changed via the I^2C/SMBus interface. See Application Note AN33 for details.

A PG delay period is defined as the time from when all conditions within the ZL2004 for asserting PG are met to when the PG pin is actually asserted. This feature is commonly used instead of using an external reset controller to control external digital logic. By default, the ZL2004 PG delay is set equal to the soft-start ramp time setting. Therefore, if the soft-start ramp time is set to 10 ms, the PG delay will be set to 10 ms. The PG delay may be set independently of the soft-start ramp using the I^2C/SMBus as described in Application Note AN33.

5.6 Switching Frequency and PLL

The ZL2004 incorporates an internal phase-locked loop (PLL) to clock the internal circuitry. The PLL can be driven by an external clock source connected to the SYNC pin. When using the internal oscillator, the SYNC pin can be configured as a clock source for other Zilker Labs devices.

The SYNC pin is a unique pin that can perform multiple functions depending on how it is configured. The CFG pin is used to select the operating mode of the SYNC pin as shown in Table 12. Figure 13 illustrates the typical connections for each mode.

Table 12. SYNC Pin Function Selection

CFG Pin	SYNC Pin Function
LOW	SYNC is configured as an input
OPEN	Auto Detect mode
HIGH	SYNC is configured as an output f_{SW} = 400 kHz

Configuration A: SYNC OUTPUT

When the SYNC pin is configured as an output (CFG pin is tied HIGH), the device will run from its internal oscillator and will drive the resulting internal oscillator signal (preset to 400 kHz) onto the SYNC pin so other devices can be synchronized to it. The SYNC pin will not be checked for an incoming clock signal while in this mode.

Configuration B: SYNC INPUT

When the SYNC pin is configured as an input (CFG pin is tied LOW), the device will automatically check for a clock signal on the SYNC pin each time EN is asserted. The ZL2004's oscillator will then synchronize with the rising edge of the external clock.

The incoming clock signal must be in the range of 200 kHz to 1.4 MHz and must be stable when the enable pin is asserted. The clock signal must also exhibit the necessary performance requirements (see Table 3). In the event of a loss of the external clock signal, the output voltage may show transient over/undershoot.

If this happens, the ZL2004 will automatically switch to its internal oscillator and switch at a frequency close to the previous incoming frequency.

Configuration C: SYNC AUTO DETECT

When the SYNC pin is configured in auto detect mode (CFG pin is left OPEN), the device will automatically check for a clock signal on the SYNC pin after enable is asserted.

If a clock signal is present, The ZL2004's oscillator will then synchronize the rising edge of the external clock. Refer to SYNC INPUT description.

If no incoming clock signal is present, the ZL2004 will configure the switching frequency according to the state of the SYNC pin as listed in Table 13. In this mode, the ZL2004 will only read the SYNC pin connection during the start-up sequence. Changes to SYNC pin connections will not affect f_{SW} until the power (VDD) is cycled off and on.

Table 13. Switching Frequency Selection

SYNC Pin	Frequency
LOW	200 kHz
OPEN	400 kHz
HIGH	1 MHz
Resistor	See Table 14

If the user wishes to run the ZL2004 at a frequency not listed in Table 13, the switching frequency can be set using an external resistor, R_{SYNC}, connected between SYNC and SGND using Table 14.

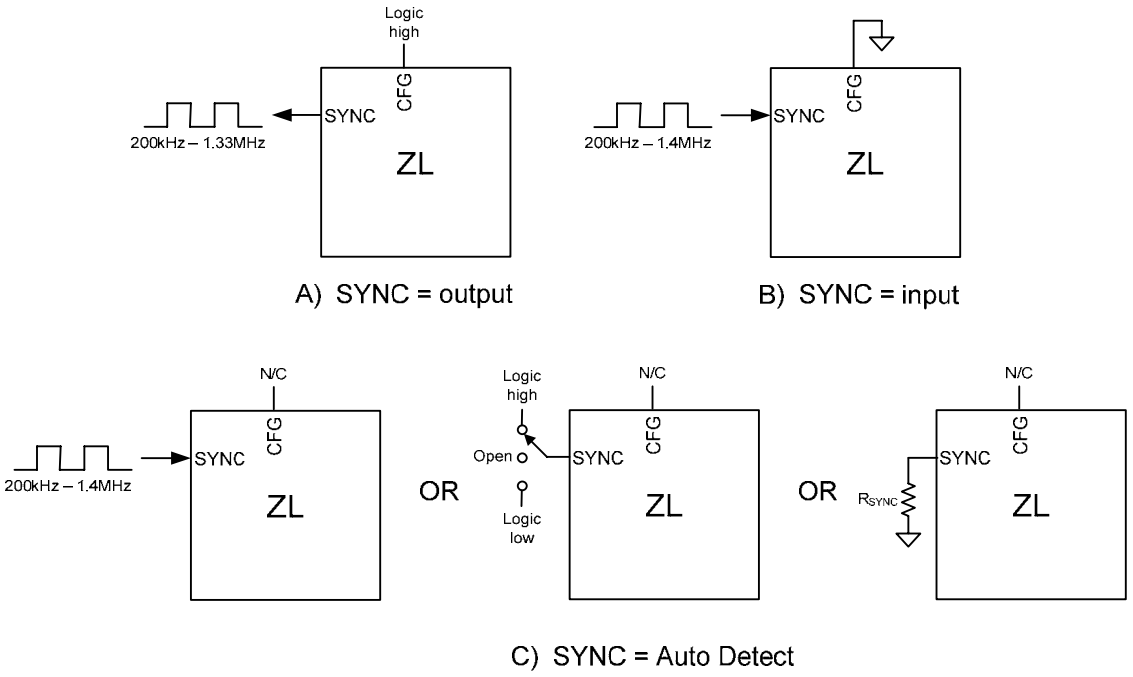


Figure 13. SYNC Pin Configurations

Table 14. R_{SYNC} Resistor Values

R_{SYNC}	f_{SW}
10 kΩ	200 kHz
11 kΩ	222 kHz
12.1 kΩ	242 kHz
13.3 kΩ	267 kHz
14.7 kΩ	296 kHz
16.2 kΩ	320 kHz
17.8 kΩ	364 kHz
19.6 kΩ	400 kHz
21.5 kΩ	421 kHz
23.7 kΩ	471 kHz

R_{SYNC}	f_{SW}
26.1 kΩ	533 kHz
28.7 kΩ	571 kHz
31.6 kΩ	615 kHz
34.8 kΩ	727 kHz
38.3 kΩ	800 kHz
46.4 kΩ	889 kHz
51.1 kΩ	1000 kHz
56.2 kΩ	1143 kHz
68.1 kΩ	1333 kHz

The switching frequency can also be set to any value between 200 kHz and 1.33 MHz using the I^2C/SMBus interface. The available frequencies below 1.4 MHz are defined by f_{SW} = 8 MHz/N, where $6 \leq N \leq 40$. See Application Note AN33 for details.

If a value other than f_{SW} = 8 MHz/N is entered using a PMBus command, the internal circuitry will select the switching frequency value using N as a whole number to achieve a value close to the entered value. For example, if 810 kHz is entered, the device will select 800 kHz (N=10).

When multiple Zilker Labs devices are used together, connecting the SYNC pins together will force all devices to synchronize with each other. The CFG pin of one device must set its SYNC pin as an output and the remaining devices must have their SYNC pins set as Auto Detect.

Note: The switching frequency read back using the appropriate PMBus command will differ slightly from the selected values in Table 14. The difference is due to hardware quantization.

5.7 Power Train Component Selection

The ZL2004 is a synchronous buck converter that uses external Driver, MOSFETs, inductor and capacitors to perform the power conversion process. The proper selection of the external components is critical for optimized performance.

To select the appropriate external components for the desired performance goals, the power supply requirements listed in Table 15 must be known.

Table 15. Power Supply Requirements

Parameter	Range	Example Value
Input voltage (V_{IN})	4.5 – 14.0 V	12 V
Output voltage (V_{OUT})	0.6 – 3.6 V	1.2 V
Output current (I_{OUT})	0 to ~25 A	20 A
Output voltage ripple (V_{orip})	< 3% of V_{OUT}	1% of V_{OUT}
Output load step (I_{ostep})	< Io	50% of I_o
Output load step rate	—	10 A/µS
Output deviation due to load step	—	± 50 mV
Maximum PCB temp.	120°C	85°C
Desired efficiency	—	85%
Other considerations	Various	Optimize for small size

5.7.1 Design Goal Trade-offs

The design of the buck power stage requires several compromises among size, efficiency, and cost. The inductor core loss increases with frequency, so there is a trade-off between a small output filter made possible by a higher switching frequency and getting better power supply efficiency. Size can be decreased by increasing the switching frequency at the expense of efficiency. Cost can be minimized by using through-hole inductors and capacitors; however these components are physically large.

To start the design, select a switching frequency based on Table 16. This frequency is a starting point and may be adjusted as the design progresses.

Table 16. Circuit Design Considerations

Frequency Range	Efficiency	Circuit Size
200–400 kHz	Highest	Larger
400–800 kHz	Moderate	Smaller
800 kHz – 1.4 MHz	Lower	Smallest

5.7.2 Driver Selection

The ZL1505 is the recommended driver IC. The ZL1505 with integrated 30V bootstrap Schottky diode has independent PWMH and PWML inputs to take advantage of the dynamic dead-time control on the ZL2004.

5.7.3 Inductor Selection

The output inductor selection process must include several trade-offs. A high inductance value will result in a low ripple current (I_{opp}), which will reduce output capacitance and produce a low output ripple voltage, but may also compromise output transient load performance. Therefore, a balance must be struck between output ripple and optimal load transient performance. A good starting point is to select the output inductor ripple equal to the expected load transient step magnitude (I_{ostep}):

$$I_{opp} = I_{ostep}$$

Now the output inductance can be calculated using the following equation, where V_{INM} is the maximum input voltage:

$$L_{OUT} = \frac{V_{OUT} \times \left(1 - \frac{V_{OUT}}{V_{INM}}\right)}{f_{sw} \times I_{opp}}$$

The average inductor current is equal to the maximum output current. The peak inductor current (I_{Lpk}) is calculated using the following equation where I_{OUT} is the maximum output current:

$$I_{Lpk} = I_{OUT} + \frac{I_{opp}}{2}$$

Select an inductor rated for the average DC current with a peak current rating above the peak current computed above.

In over-current or short-circuit conditions, the inductor may have currents greater than 2X the normal maximum rated output current. It is desirable to use an inductor that still provides some inductance to protect the load and the MOSFETs from damaging currents in this situation.

Once an inductor is selected, the DCR and core losses in the inductor are calculated. Use the DCR specified in the inductor manufacturer's datasheet.

$$P_{LDCR} = DCR \times I_{Lrms}^{2}$$

I_{Lrms} is given by

$$I_{Lrms} = \sqrt{I_{OUT}^{2} + \frac{(I_{opp})^{2}}{12}}$$

where I_{OUT} is the maximum output current. Next, calculate the core loss of the selected inductor. Since this calculation is specific to each inductor and manufacturer, refer to the chosen inductor datasheet. Add the core loss and the ESR loss and compare the total loss to the maximum power dissipation recommendation in the inductor datasheet.

5.7.4 Output Capacitor Selection

Several trade-offs must also be considered when selecting an output capacitor. Low ESR values are needed to have a small output deviation during transient load steps (V_{osag}) and low output voltage ripple (V_{orip}). However, capacitors with low ESR, such as semi-stable (X5R and X7R) dielectric ceramic capacitors, also have relatively low capacitance values. Many designs can use a combination of high capacitance devices and low ESR devices in parallel.

For high ripple currents, a low capacitance value can cause a significant amount of output voltage ripple. Likewise, in high transient load steps, a relatively large amount of capacitance is needed to minimize the output voltage deviation while the inductor current ramps up or down to the new steady state output current value.

As a starting point, apportion one-half of the output ripple voltage to the capacitor ESR and the other half to capacitance, as shown in the following equations:

$$C_{OUT} = \frac{I_{opp}}{8 \times f_{sw} \times \frac{V_{orip}}{2}}$$

$$ESR = \frac{V_{orip}}{2 \times I_{opp}}$$

Use these values to make an initial capacitor selection, using a single capacitor or several capacitors in parallel.

After a capacitor has been selected, the resulting output voltage ripple can be calculated using the following equation:

$$V_{orip} = I_{opp} \times ESR + \frac{I_{opp}}{8 \times f_{sw} \times C_{OUT}}$$

Because each part of this equation was made to be less than or equal to half of the allowed output ripple voltage, the V_{orip} should be less than the desired maximum output ripple.

5.7.5 Input Capacitor

It is highly recommended that dedicated input capacitors be used in any point-of-load design, even when the supply is powered from a heavily filtered 5 or 12 V "bulk" supply from an off-line power supply. This is because of the high RMS ripple current that is drawn by the buck converter topology. This ripple (I_{CINrms}) can be determined from the following equation:

$$I_{CINrms} = I_{OUT} \times \sqrt{D \times (1 - D)}$$

Without capacitive filtering near the power supply circuit, this current would flow through the supply bus and return planes, coupling noise into other system circuitry. The input capacitors should be rated at 1.2X the ripple current calculated above to avoid overheating of the capacitors due to the high ripple current, which can cause premature failure. Ceramic capacitors with X7R or X5R dielectric with low ESR and 1.1X the maximum expected input voltage are recommended.

5.7.6 QL Selection

The bottom MOSFET should be selected primarily based on the device's $R_{DS(ON)}$ and secondarily based on its gate charge. To choose QL, use the following equation and allow 2–5% of the output power to be dissipated in the $R_{DS(ON)}$ of QL (lower output voltages and higher step-down ratios will be closer to 5%):

$$P_{QL} = 0.05 \times V_{OUT} \times I_{OUT}$$

Calculate the RMS current in QL as follows:

$$I_{botrms} = I_{Lrms} \times \sqrt{1 - D}$$

Calculate the desired maximum $R_{DS(ON)}$ as follows:

$$R_{DS(ON)} = \frac{P_{QL}}{(I_{botrms})^2}$$

Note that the $R_{DS(ON)}$ given in the manufacturer's datasheet is measured at 25°C. The actual $R_{DS(ON)}$ in the end-use application will be much higher. For example, a Vishay Si7114 MOSFET with a junction temperature of 125°C has an $R_{DS(ON)}$ that is 1.4 times higher than the value at 25°C. Select a candidate MOSFET, and calculate the required gate drive current as follows:

$$I_g = f_{SW} \times Q_g$$

Keep in mind that the total allowed gate drive current for both QH and QL is 80 mA.

MOSFETs with lower $R_{DS(ON)}$ tend to have higher gate charge requirements, which increases the current and resulting power required to turn them on and off. Since the MOSFET gate drive circuits are integrated in the ZL1505, this power is dissipated in the ZL1505 according to the following equation:

$$P_{QL} = f_{sw} \times Q_g \times V_{INM}$$

5.7.7 QH Selection

In addition to the $R_{DS(ON)}$ loss and gate charge loss, QH also has switching loss. The procedure to select QH is similar to the procedure for QL. First, assign 2–5% of the output power to be dissipated in the $R_{DS(ON)}$ of QH using the equation for QL above. As was done with QL, calculate the RMS current as follows:

$$I_{toprms} = I_{Lrms} \times \sqrt{D}$$

Calculate a starting $R_{DS(ON)}$ as follows, in this example using 5%:

$$P_{QH} = 0.05 \times V_{OUT} \times I_{OUT}$$

$$R_{DS(ON)} = \frac{P_{QH}}{(I_{toprms})^2}$$

Select a MOSFET and calculate the resulting gate drive current. Verify that the combined gate drive current from QL and QH does not exceed 80 mA.

Next, calculate the switching time using:

$$t_{SW} = \frac{Q_g}{I_{gdr}}$$

where Q_g is the gate charge of the selected QH and I_{gdr} is the peak gate drive current available from the ZL1505.

Although the ZL1505 has a typical gate drive current of 3.2 A, use the minimum guaranteed current of 2 A for a conservative design. Using the calculated switching time, calculate the switching power loss in QH using:

$$P_{swtop} = V_{INM} \times t_{sw} \times I_{OUT} \times f_{sw}$$

The total power dissipated by QH is given by the following equation:

$$P_{QHtot} = P_{QH} + P_{swtop}$$

5.7.8 MOSFET Thermal Check

Once the power dissipations for QH and QL have been calculated, the MOSFET's junction temperature can be estimated. Using the junction-to-case thermal resistance (R_{th}) given in the MOSFET manufacturer's datasheet and the expected maximum printed circuit board temperature, calculate the junction temperature as follows:

$$T_{j\max} = T_{pcb} + (P_Q \times R_{th})$$

5.7.9 Current Sensing Components

Once the current sense method has been selected (Refer to Section 5.8, "Current Limit Threshold Selection,"), the components are selected as follows.

When using the inductor DCR sensing method, the user must also select an R/C network comprised of R1 and CL (see Figure 14).

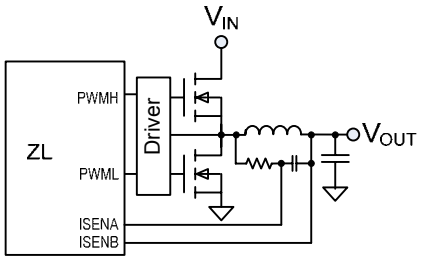


Figure 14. DCR Current Sensing

For the voltage across C_L to reflect the voltage across the DCR of the inductor, the time constant of the inductor must match the time constant of the RC network. That is:

$$\tau_{RC} = \tau_{L/DCR}$$

$$R_1 \cdot C_L = \frac{L}{DCR}$$

For L, use the average of the nominal value and the minimum value. Include the effects of tolerance, DC Bias and switching frequency on the inductance when determining the minimum value of L. Use the typical value for DCR.

The value of R_1 should be as small as feasible and no greater than 5 kΩ for best signal-to-noise ratio. The designer should make sure the resistor package size is appropriate for the power dissipated and include this loss in efficiency calculations. In calculating the minimum value of R_1, the average voltage across C_L (which is the average $I_{OUT} \cdot DCR$ product) is small and can be neglected. Therefore, the minimum value of R_1 may be approximated by the following equation:

$$R_{1-\min} = \frac{D\left(V_{IN-\max} - V_{OUT}\right)^2 + \left(1-D\right)\cdot V_{OUT}{}^2}{P_{R1\,pkg-\max} \cdot \delta_P},$$

where $P_{R1pkg\text{-max}}$ is the maximum power dissipation specification for the resistor package and δ_P is the derating factor for the same parameter (eg.: $P_{R1pkg\text{-max}}$ = 0.0625W for 0603 package, δ_P = 50% @ 85°C). Once $R_{1\text{-min}}$ has been calculated, solve for the maximum value of C_L from

$$C_{L-\max} = \frac{L}{R_{1-\min} \cdot DCR}$$

and choose the next-lowest readily available value (eg.: For $C_{L\text{-max}}$ = 1.86µF, C_L = 1.5µF is a good choice). Then substitute the chosen value into the same equation and re-calculate the value of R_1. Choose the 1% resistor standard value closest to this re-calculated value of R_1. The error due to the mismatch of the two time constants is

$$\varepsilon_\tau = \left(1 - \frac{R_1 \cdot C_L \cdot DCR}{L_{avg}}\right) \cdot 100\%$$

The value of R_2 should be simply five times that of R_1:

$$R_2 = 5 \cdot R_1$$

5.8 Current Limit Threshold Selection

It is recommended that the user include a current limiting mechanism in their design to protect the power supply from damage and prevent excessive current from being drawn from the input supply in the event that the output is shorted to ground or an overload condition is imposed on the output. Current limiting is accomplished by sensing the current through the circuit during a portion of the duty cycle.

Output current sensing can be accomplished by measuring the voltage across a series resistive sensing element according to the following equation:

$$V_{LIM} = I_{LIM} \times R_{SENSE}$$

Where:

I_{LIM} is the desired maximum current that should flow in the circuit

R_{SENSE} is the resistance of the sensing element

V_{LIM} is the voltage across the sensing element at the point the circuit should start limiting the output current.

The ZL2004 supports "lossless" current sensing, by measuring the voltage across a resistive element that is already present in the circuit. This eliminates additional efficiency losses incurred by devices that must use an additional series resistance in the circuit.

To set the current limit threshold, the user must first select a current sensing method. The ZL2004 incorporates one method for current sensing, inductor DC resistance (DCR) sensing; Figure 14 shows a simplified schematic for DCR method.

The current sensing method and current limit threshold can be selected using the ILIM pin using Table 17.

In addition to selecting the current sensing method, the ZL2004 gives the power supply designer several choices for the fault response during over or under current condition. The user can select the number of violations allowed before declaring fault, a blanking time and the action taken when a fault is detected.

The blanking time represents the time when no current measurement is taken. This is to avoid taking a reading just after a current load step (less accurate due to potential ringing). It is a configurable parameter.

ZL2004 provides an adjustable maximum full scale sensing range. The range can be adjusted from 25 mV to 50 mV using pin-strap or resistor setting method described in Table 17 and Table 18.

Table 17 includes default parameters for the number of violations and the blanking time using pin-strap.

Table 17. Pin-strap Settings for Current Sensing

ILIM Pin	Current Limiting Configuration	Number of Violations Allowed[2]	Current Limit Threshold V_{LIM}	Maximum Current Sensing Range
LOW	Output-referenced, down-slope sensing (Inductor DCR sensing) Blanking time: 224 ns	5	25 mV	25 mV
OPEN	Output-referenced, down-slope sensing (Inductor DCR sensing) Blanking time: 224 ns	5	35 mV	35 mV
HIGH	Output-referenced, down-slope sensing (Inductor DCR sensing) Blanking time: 224 ns	5	50 mV	50 mV
Resistor[1]	Depends on resistor value used; see Table 18			

Notes:
1. 10 kΩ < R_{ILIM0} < 100 kΩ
2. The number of violations allowed prior to issuing a fault response.

Table 18. Resistor Configured Current Sensing Value

R_{ILIM}	Current Sensing Method	Current Limit Threshold Setting V_{LIM}	Maximum Current Sensing Range
10 kΩ	Output-referenced, down-slope sensing (Inductor DCR sensing) Blanking time: 224 ns Number of violation allowed[1]: 5	0 mV	25 mV
11 kΩ		5 mV	
12.1 kΩ		10 mV	
13.3 kΩ		15 mV	
14.7 kΩ		20 mV	
16.2 kΩ		25 mV	
17.8 kΩ	Output-referenced, down-slope sensing (Inductor DCR sensing) Blanking time: 224 ns Number of violation allowed[1]: 5	0 mV	35 mV
19.6 kΩ		5 mV	
21.5 kΩ		10 mV	
23.7 kΩ		15 mV	
26.1 kΩ		20 mV	
28.7 kΩ		25 mV	
31.6 kΩ		30 mV	
34.8 kΩ		35 mV	
38.3 kΩ	Output-referenced, down-slope sensing (Inductor DCR sensing) Blanking time: 224 ns Number of violation allowed[1]: 5	0 mV	50 mV
42.2 kΩ		5 mV	
46.4 kΩ		10 mV	
51.1 kΩ		15 mV	
56.2 kΩ		20 mV	
61.9 kΩ		25 mV	
68.1 kΩ		30 mV	
75 kΩ		35 mV	
82.5 kΩ		40 mV	
90.9 kΩ		45 mV	
100 kΩ		50 mV	

Notes:
1. The number of violations allowed prior to issuing a fault response.

Once the sensing method has been selected, the user must select the voltage threshold (VLIM), the desired current limit threshold, and the resistance of the sensing element.

The threshold voltage can be selected in 5 mV increments by connecting a resistor, R_{ILIM}, between the ILIM pin and ground according to Table 18. This method is preferred if the user does not desire to use or does not have access to the I²C/SMBus interface and the desired threshold value is contained in Table 18.

The current limit threshold can also be set to a custom value via the I²C/SMBus interface. Please refer to Application Note AN33 for further details.

5.9 Loop Compensation

The ZL2004 operates as a voltage-mode synchronous buck controller with a fixed frequency PWM scheme. Although the ZL2004 uses a digital control loop, it operates much like a traditional analog PWM controller. Figure 15 is a simplified block diagram of the ZL2004 control loop, which differs from an analog control loop only by the constants in the PWM and compensation blocks. As in the analog controller case, the compensation block compares the output voltage to the desired voltage reference and compensation zeroes are added to keep the loop stable. The resulting integrated error signal is used to drive the PWM logic, converting the error signal to a duty cycle to drive the external MOSFETs.

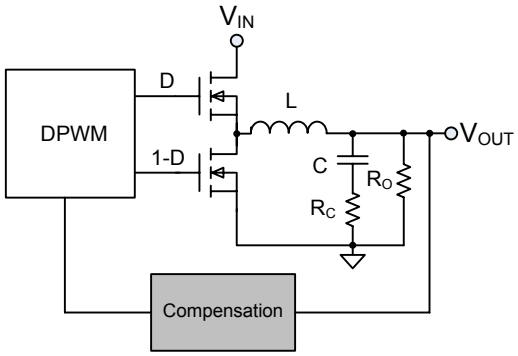


Figure 15. Control Loop Block Diagram

In the ZL2004, the compensation zeros are set by configuring the FC pin or via the I²C/SMBus interface once the user has calculated the required settings. This method eliminates the inaccuracies due to the component tolerances associated with using external resistors and capacitors required with traditional analog controllers. Utilizing the loop compensation settings shown in Table 19 will yield a conservative crossover frequency at a fixed fraction of the switching frequency ($f_{SW}/20$) and 60° of phase margin.

Step 1: Using the following equation, calculate the resonant frequency of the LC filter, f_n.

$$f_n = \frac{1}{2\pi\sqrt{L \times C}}$$

Step 2: Calculate the ESR zero frequency (f_{ZESR}).

$$f_{zesr} = \frac{1}{2\pi CRc}$$

Step 3: Based on Table 19, determine the FC setting.

5.10 Adaptive Loop Compensation

Loop compensation can be a time-consuming process, forcing the designer to accommodate design trade-offs related to performance and stability across a wide range of operating conditions. The ZL2004 offers an adaptive compensation mode that enables the user to increase the stability over a wider range of loading conditions by automatically adapting the loop compensation coefficients for changes in load current.

Setting the loop compensation coefficients through the I²C/SMBus interface allows for a second set of coefficients to be stored in the device in order to utilize adaptive loop compensation. This algorithm uses the two sets of compensation coefficients to determine optimal compensation settings as the output load changes. Please refer to Application Note AN33 for further details.

5.11 Non-linear Response (NLR) Settings

The ZL2004 incorporates a non-linear response (NLR) loop that decreases the response time and the output voltage deviation in the event of a sudden output load current step. The NLR loop incorporates a secondary error signal processing path that bypasses the primary error loop when the output begins to transition outside of the standard regulation limits. This scheme results in a higher equivalent loop bandwidth than what is possible using a traditional linear loop.

When a load current step function imposed on the output causes the output voltage to drop below the lower regulation limit, the NLR circuitry will force a positive correction signal that will turn on the upper MOSFET and quickly force the output to increase. Conversely, a negative load step (i.e. removing a large load current) will cause the NLR circuitry to force a negative correction signal that will turn on the lower MOSFET and quickly force the output to decrease. The ZL2004 has been pre-configured with appropriate NLR settings that correspond to the loop compensation settings in Table 19.

Table 19. Pin-strap Settings for Loop Compensation

NLR	f_n Range	f_{zesr} Range	FC Pin
Off	$f_{sw}/60 < f_n < f_{sw}/30$	$f_{zesr} > f_{sw}/10$	10 kΩ
		$f_{sw}/10 > f_{zesr} > f_{sw}/30$	11 kΩ
		$f_{sw}/30 > f_{zesr} > f_{sw}/60$	12.1 kΩ
	$f_{sw}/120 < f_n < f_{sw}/60$	$f_{zesr} > f_{sw}/10$	13.3 kΩ
		$f_{sw}/10 > f_{zesr} > f_{sw}/30$	14.7 kΩ
		$f_{sw}/30 > f_{zesr} > f_{sw}/60$	16.2 kΩ
	$f_{sw}/240 < f_n < f_{sw}/120$	$f_{zesr} > f_{sw}/10$	17.8 kΩ
		$f_{sw}/10 > f_{zesr} > f_{sw}/30$	19.6 kΩ
		$f_{sw}/30 > f_{zesr} > f_{sw}/60$	21.5 kΩ
On	$f_{sw}/60 < f_n < f_{sw}/30$	$f_{zesr} > f_{sw}/10$	23.7 kΩ
		$f_{sw}/10 > f_{zesr} > f_{sw}/30$	26.1 kΩ
		$f_{sw}/30 > f_{zesr} > f_{sw}/60$	28.7 kΩ
	$f_{sw}/120 < f_n < f_{sw}/60$	$f_{zesr} > f_{sw}/10$	31.6 kΩ
		$f_{sw}/10 > f_{zesr} > f_{sw}/30$	34.8 kΩ
		$f_{sw}/30 > f_{zesr} > f_{sw}/60$	38.3 kΩ
	$f_{sw}/240 < f_n < f_{sw}/120$	$f_{zesr} > f_{sw}/10$	42.2 kΩ
		$f_{sw}/10 > f_{zesr} > f_{sw}/30$	46.4 kΩ
		$f_{sw}/30 > f_{zesr} > f_{sw}/60$	51.1 kΩ

5.12 Efficiency Optimized Driver Dead-time Control

The ZL2004 utilizes a closed loop algorithm to optimize the dead-time applied between the gate drive signals for the top and bottom FETs. In a synchronous buck converter, the MOSFET drive circuitry must be designed such that the top and bottom MOSFETs are never in the conducting state at the same time. Potentially damaging currents flow in the circuit if both top and bottom MOSFETs are simultaneously on for periods of time exceeding a few nanoseconds. Conversely, long periods of time in which both MOSFETs are off reduce overall circuit efficiency by allowing current to flow in their parasitic body diodes.

It is therefore advantageous to minimize this dead-time to provide optimum circuit efficiency. In the first order model of a buck converter, the duty cycle is determined by the equation:

$$D \approx \frac{V_{OUT}}{V_{IN}}$$

However, non-idealities exist that cause the real duty cycle to extend beyond the ideal. Dead-time is one of those non-idealities that can be manipulated to improve efficiency. The ZL2004 has an internal algorithm that constantly adjusts dead-time non-overlap to minimize duty cycle, thus maximizing efficiency.

This circuit will null out dead-time differences due to component variation, temperature, and loading effects.

This algorithm is independent of application circuit parameters such as MOSFET type, gate driver delays, rise and fall times and circuit layout.

In addition, it does not require drive or MOSFET voltage or current waveform measurements.

5.13 Adaptive Diode Emulation

Most power converters use synchronous rectification to optimize efficiency over a wide range of input and output conditions. However, at light loads the synchronous MOSFET will typically sink current and introduce additional energy losses associated with higher peak inductor currents, resulting in reduced efficiency. Adaptive diode emulation mode turns off the low-side FET gate drive at low load currents to prevent the inductor current from going negative, reducing the energy losses and increasing overall efficiency. Diode emulation is available to single-phase devices only.

Note: the overall bandwidth of the device may be reduced when in diode emulation mode. It is recommended that diode emulation is disabled prior to applying significant load steps.

5.14 Adaptive Frequency Control

Since switching losses contribute to the efficiency of the power converter, reducing the switching frequency will reduce the switching losses and increase efficiency. The ZL2004 includes Adaptive Frequency Control mode, which effectively reduces the observed switching frequency as the load decreases.

Adaptive frequency mode is enabled by setting bit 0 of MISC_CONFIG to 1 and is only available while the device is operating within Adaptive Diode Emulation Mode. As the load current is decreased, diode emulation mode decreases the GL on-time to prevent negative inductor current from flowing. As the load is decreased further, the GH pulse width will begin to decrease while maintaining the programmed frequency, f_{PROG} (set by the FREQ_SWITCH command).

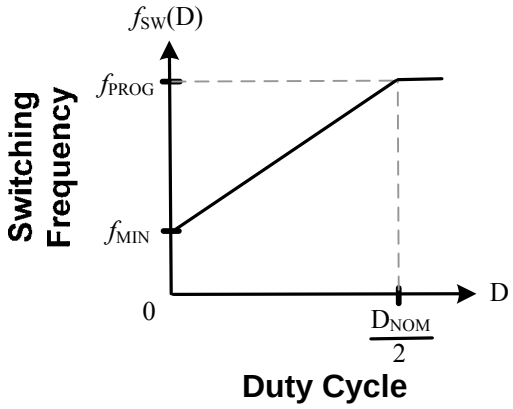


Figure 16. Adaptive Frequency

Once the GH pulse width (D) reaches 50% of the nominal duty cycle, D_{NOM} (determined by Vin and Vout), the switching frequency will start to decrease according to the following equation:

If $D < \frac{D_{NOM}}{2}$ then

$$f_{SW}(D) = \left(\frac{2(f_{SW} - f_{MIN})}{D_{NOM}}\right)D + f_{MIN}$$

Otherwise $f_{SW}(D) = f_{PROG}$

This is illustrated in Figure 16. Due to quantizing effects inside the IC, the ZL2004 will decrease its frequency in steps between f_{SW} and f_{MIN}. The quantity and magnitude of the steps will depend on the difference between f_{SW} and f_{MIN} as well as the frequency range.

It should be noted that adaptive frequency mode is not available for current sharing groups and is not allowed when the device is placed in auto-detect mode and a clock source is present on the SYNC pin, or if the device is outputting a clock signal on its SYNC pin.

6. Power Management Functional Description

6.1 Input Undervoltage Lockout

The input undervoltage lockout (UVLO) prevents the ZL2004 from operating when the input falls below a preset threshold, indicating the input supply is out of its specified range. The UVLO threshold (V_{UVLO}) can be set between 4.5V and 10.8 V using the SS pin. The simplest implementation is to connect the SS pin as shown in Table 11.

The UVLO voltage can also be set to any value between 2.85 V and 16 V via the I^2C/SMBus interface.

Once an input undervoltage fault condition occurs, the device can respond in a number of ways as follows:

1. Continue operating without interruption.
2. Continue operating for a given delay period, followed by shutdown if the fault still exists. The device will remain in shutdown until instructed to restart.
3. Initiate an immediate shutdown until the fault has been cleared. The user can select a specific number of retry attempts.

The default response from a UVLO fault is an immediate shutdown of the device. The device will continuously check for the presence of the fault condition. If the fault condition is no longer present, the ZL2004 will be re-enabled.

Please refer to Application Note AN33 for details on how to configure the UVLO threshold or to select specific UVLO fault response options via the I^2C/SMBus interface.

6.2 Output Overvoltage Protection

The ZL2004 offers an internal output overvoltage protection circuit that can be used to protect sensitive load circuitry from being subjected to a voltage higher than its prescribed limits. A hardware comparator is used to compare the actual output voltage (seen at the VSEN pin) to a threshold set to 15% higher than the target output voltage (the default setting). If the VSEN voltage exceeds this threshold, the PG pin will de-assert and the device can then respond in a number of ways as follows:

1. Initiate an immediate shutdown until the fault has been cleared. The user can select a specific number of retry attempts.
2. Turn off the high-side MOSFET and turn on the low-side MOSFET. The low-side MOSFET remains ON until the device attempts a restart.

The default response from an overvoltage fault is to immediately shut down. The device will continuously check for the presence of the fault condition, and when the fault condition no longer exists the device will be re-enabled.

For continuous overvoltage protection when operating from an external clock, the only allowed response is an immediate shutdown.

Refer to AN33 for details on how to select specific overvoltage fault response options.

6.3 Output Pre-Bias Protection

An output pre-bias condition exists when an externally applied voltage is present on a power supply's output before the power supply's control IC is enabled. Certain applications require that the converter not be allowed to sink current during start up if a pre-bias condition exists at the output. The ZL2004 provides pre-bias protection by sampling the output voltage prior to initiating an output ramp.

If a pre-bias voltage lower than the target voltage exists after the pre-configured delay period has expired, the target voltage is set to match the existing pre-bias voltage and both drivers are enabled. The output voltage is then ramped to the final regulation value at the ramp rate set by the SS pin.

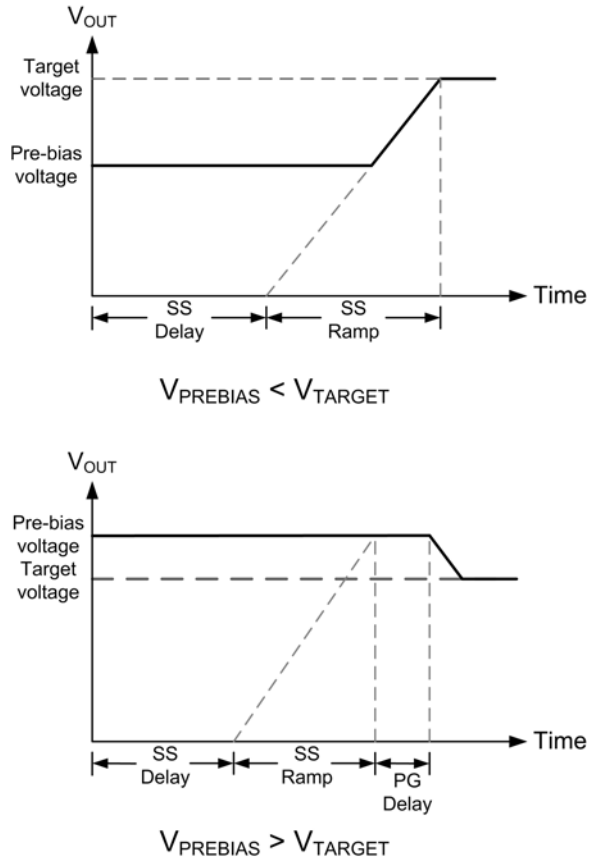


Figure 17. Output Responses to Pre-bias Voltages

The actual time the output will take to ramp from the pre-bias voltage to the target voltage will vary depending on the pre-bias voltage but the total time elapsed from when the delay period expires and when the output reaches its target value will match the pre-configured ramp time. See Figure 17.

If a pre-bias voltage higher than the target voltage exists after the pre-configured delay period has expired, the target voltage is set to match the existing pre-bias voltage and both drivers are enabled with a PWM duty cycle that would ideally create the pre-bias voltage. Once the pre-configured soft-start ramp period has expired, the PG pin will be asserted (assuming the pre-bias voltage is not higher than the overvoltage limit). The PWM will then adjust its duty cycle to match the original target voltage and the output will ramp down to the pre-configured output voltage.

If a pre-bias voltage higher than the overvoltage limit exists, the device will not initiate a turn-on sequence and will declare an overvoltage fault condition to exist. In this case, the device will respond based on the output overvoltage fault response method that has been selected. See Section 6.2 "Output Overvoltage Protection," for response options due to an overvoltage condition.

Pre-bias protection is not offered for current sharing groups that also have tracking enabled.

6.4 Output Overcurrent Protection

The ZL2004 can protect the power supply from damage if the output is shorted to ground or if an overload condition is imposed on the output. Once the current limit threshold has been selected (see Section 5.8 "Current Limit Threshold Selection"), the user may determine the desired course of action in response to the fault condition. The following overcurrent protection response options are available:

1. Initiate a shutdown and attempt to restart an infinite number of times with a preset delay period between attempts.
2. Initiate a shutdown and attempt to restart a preset number of times with a preset delay period between attempts.
3. Continue operating for a given delay period, followed by shutdown if the fault still exists.
4. Continue operating through the fault (this could result in permanent damage to the power supply).
5. Initiate an immediate shutdown.

The default response from an overcurrent fault is an immediate shutdown of the device. The device will continuously check for the presence of the fault condition, and if the fault condition no longer exists the device will be re-enabled.

Refer to AN33 for details on how to select specific overcurrent fault response options.

6.5 Thermal Overload Protection

The ZL2004 includes an on-chip thermal sensor that continuously measures the internal temperature of the die and shuts down the device when the temperature exceeds the preset limit. The default temperature limit is set to 125°C in the factory, but the user may set the limit to a different value if desired. See Application Note AN33 for details. Note that setting a higher thermal limit via the I^2C/SMBus interface may result in permanent damage to the device. Once the device has been disabled due to an internal temperature fault, the user may select one of several fault response options as follows:

1. Initiate a shutdown and attempt to restart an infinite number of times with a preset delay period between attempts.
2. Initiate a shutdown and attempt to restart a preset number of times with a preset delay period between attempts.
3. Continue operating for a given delay period, followed by shutdown if the fault still exists.
4. Continue operating through the fault (this could result in permanent damage to the power supply).
5. Initiate an immediate shutdown.

If the user has configured the device to restart, the device will wait the preset delay period (if configured to do so) and will then check the device temperature. If the temperature has dropped below a threshold that is approx 15°C lower than the selected temperature fault limit, the device will attempt to re-start. If the temperature still exceeds the fault limit the device will wait the preset delay period and retry again.

The default response from a temperature fault is an immediate shutdown of the device. The device will continuously check for the fault condition, and once the fault has cleared the ZL2004 will be re-enabled.

6.6 Voltage Tracking

Numerous high performance systems place stringent demands on the order in which the power supply voltages are turned on. This is particularly true when powering FPGAs, ASICs, and other advanced processor devices that require multiple supply voltages to power a single die. In most cases, the I/O interface operates at a higher voltage than the core and therefore the core supply voltage must not exceed the I/O supply voltage according to the manufacturers' specifications.

The ZL2004 integrates a lossless tracking scheme that allows its output to track a voltage that is applied to the VTRK pin with no external components required. The VTRK pin is an analog input that, when tracking mode is enabled, configures the voltage applied to the VTRK pin to act as a reference for the device's output regulation.

Figure 18 illustrates the typical connection and the two tracking modes:

1. *Coincident*. This mode configures the ZL2004 to ramp its output voltage at the same rate as the voltage applied to the VTRK pin.
2. *Ratiometric*. This mode configures the ZL2004 to ramp its output voltage at a rate that is a percentage of the voltage applied to the VTRK pin. The default setting is 50%, but an external resistor string may be used to configure a different tracking ratio.

The master ZL2004 device in a tracking group is defined as the device that has the highest target output voltage within the group. This master device will control the ramp rate of all tracking devices and is not configured for tracking mode. A delay of at least 10 ms must be configured into the master device using the SS pin and the user may also configure a specific ramp rate using the SS pin.

Any device that is configured for tracking mode will ignore its soft-start delay and ramp time settings (SS pin) and its output will take on the turn-on/turn-off characteristics of the reference voltage present at the VTRK pin.

The tracking mode for all other devices can be set by connecting a resistor from the SS pin to ground according to Table 20. All of the ENABLE pins in the tracking group must be connected together and driven by a single logic source. CFG pin needs also to have been set to the appropriate value to enable tracking mode using pin-strap.

Tracking mode can also be configured via the I²C/SMBus interface by using the TRACK_CONFIG command.

Note that current sharing groups that are also configured to track another voltage do not offer pre-bias protection; a minimum load should therefore be enforced to avoid the output voltage from being held up by an outside force. Additionally, a device set up for tracking must have both Alternate Ramp Control and Precise Ramp-Up Delay disabled.

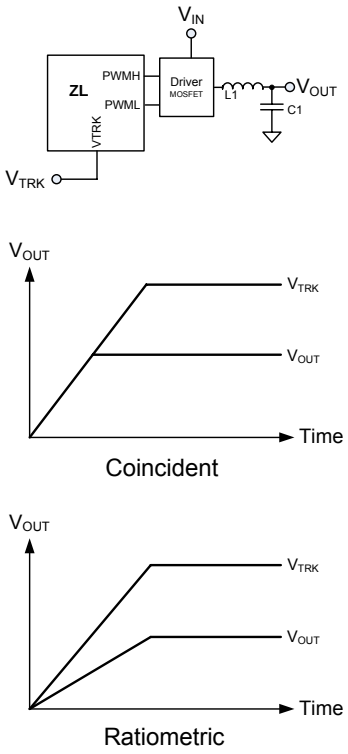


Figure 18. Tracking Modes

6.7 Voltage Margining

The ZL2004 offers a simple means to vary its output higher or lower than its nominal voltage setting in order to determine whether the load device is capable of operating over its specified supply voltage range. The MGN command is set by driving the MGN pin or through the I²C/SMBus interface. The MGN pin is a TTL-compatible input that is continuously monitored and can be driven directly by a processor I/O pin or other logic-level output.

The ZL2004's output will be forced higher than its nominal set point when the MGN command is set HIGH, and the output will be forced lower than its nominal set point when the MGN command is set LOW. Default margin limits of V_{NOM} ±5% are pre-loaded in the factory, but the margin limits can be modified through the I²C/SMBus interface to as high as V_{NOM} + 10% or as low as 0 V, where V_{NOM} is the nominal output voltage set point determined by the V0 and V1 pins. A safety feature prevents the user from configuring the output voltage to exceed V_{NOM} + 10% under any conditions.

The margin limits and the MGN command can both be set individually through the I²C/SMBus interface. Additionally, the transition rate between the nominal output voltage and either margin limit can be configured through the I²C interface. Please refer to Application Note AN33 for detailed instructions on modifying the margining configurations.

6.8 External Voltage Monitoring

The voltage monitoring (VMON) pin is available to monitor the voltage supply for the external driver IC. If the voltage falls below a predefined threshold value (adjustable through a PMBus command), the device will fault and stop sending PWM signals. A 1/16 external resistor divider is required to keep the maximum voltage on this pin to less than 1.15 V.

Table 20. Tracking Mode Configuration

R_{SS}	UVLO	Tracking Ratio	Upper Track Limit	Ramp-up / Ramp-down Behavior
19.6 kΩ	4.5 V	100%	Limited by target voltage	Output not allowed to decrease before PG
21.5 kΩ				Output will always follow VTRK
23.7 kΩ			Limited by VTRK pin voltage	Output not allowed to decrease before PG
26.1 kΩ				Output will always follow VTRK
28.7 kΩ		50%	Limited by target voltage	Output not allowed to decrease before PG
31.6 kΩ				Output will always follow VTRK
34.8 kΩ			Limited by VTRK pin voltage	Output not allowed to decrease before PG
38.3 kΩ				Output will always follow VTRK
42.2 kΩ	10.8 V	100%	Limited by target voltage	Output not allowed to decrease before PG
46.4 kΩ				Output will always follow VTRK
51.1 kΩ			Limited by VTRK pin voltage	Output not allowed to decrease before PG
56.2 kΩ				Output will always follow VTRK
61.9 kΩ		50%	Limited by target voltage	Output not allowed to decrease before PG
68.1 kΩ				Output will always follow VTRK
75 kΩ			Limited by VTRK pin voltage	Output not allowed to decrease before PG
82.5 kΩ				Output will always follow VTRK

6.9 I²C/SMBus Communications

The ZL2004 provides an I²C/SMBus digital interface that enables the user to configure all aspects of the device operation as well as monitor the input and output parameters. The ZL2004 can be used with any standard 2-wire I²C host device. In addition, the device is compatible with SMBus version 2.0 and includes an SALRT line to help mitigate bandwidth limitations related to continuous fault monitoring. Pull-up resistors are required on the I²C/SMBus. The ZL2004 accepts most standard PMBus commands. When controlling the device with PMBus commands, it is recommended that the enable pin is tied to SGND.

6.10 I²C/SMBus Device Address Selection

When communicating with multiple SMBus devices using the I²C/SMBus interface, each device must have its own unique address so the host can distinguish between the devices. The device address can be set according to the pin-strap options listed in Table 21. Address values are right-justified.

Table 21. SMBus Device Address Selection

		SA0		
		LOW	OPEN	HIGH
SA1	LOW	0x20	0x21	0x22
	OPEN	0x23	0x24	0x25
	HIGH	0x26	0x27	Reserved

If additional device addresses are required, a resistor can be connected to the SA0 pin according to Table 22 to provide up to 25 unique device addresses. In this case, the SA1 pin should be tied to SGND.

If more than 25 unique device addresses are required or if other SMBus address values are desired, both the SA0 and SA1 pins can be configured with a resistor to SGND according to the following equation and Table 23.

SMBus address = 25 x (SA1 index) + (SA0 index) (in decimal)

Table 22. SMBus Address Values

R_{SA}	SMBus Address	R_{SA}	SMBus Address
10 kΩ	0x00	34.8 kΩ	0x0D
11 kΩ	0x01	38.3 kΩ	0x0E
12.1 kΩ	0x02	42.2 kΩ	0x0F
13.3 kΩ	0x03	46.4 kΩ	0x10
14.7 kΩ	0x04	51.1 kΩ	0x11
16.2 kΩ	0x05	56.2 kΩ	0x12
17.8 kΩ	0x06	61.9 kΩ	0x13
19.6 kΩ	0x07	68.1 kΩ	0x14
21.5 kΩ	0x08	75 kΩ	0x15
23.7 kΩ	0x09	82.5 kΩ	0x16
26.1 kΩ	0x0A	90.9 kΩ	0x17
28.7 kΩ	0x0B	100 kΩ	0x18
31.6 kΩ	0x0C		

Using this method, the user can theoretically configure up to 625 unique SMBus addresses, however the SMBus is inherently limited to 128 devices so attempting to configure an address higher than 128 (0x80) will cause the device address to repeat (i.e, attempting to configure a device address of 129 (0x81) would result in a device address of 1. Therefore, the user should use index values 0-4 on the SA1 pin and the full range of index values on the SA0 pin, which will provide 125 device address combinations.

Table 23. SMBus Address Index Values

R_{SA}	SA0 or SA1 Index	R_{SA}	SA0 or SA1 Index
10 kΩ	0	34.8 kΩ	13
11 kΩ	1	38.3 kΩ	14
12.1 kΩ	2	42.2 kΩ	15
13.3 kΩ	3	46.4 kΩ	16
14.7 kΩ	4	51.1 kΩ	17
16.2 kΩ	5	56.2 kΩ	18
17.8 kΩ	6	61.9 kΩ	19
19.6 kΩ	7	68.1 kΩ	20
21.5 kΩ	8	75 kΩ	21
23.7 kΩ	9	82.5 kΩ	22
26.1 kΩ	10	90.9 kΩ	23
28.7 kΩ	11	100 kΩ	24
31.6 kΩ	12		

6.11 Digital-DC Bus

The Digital-DC Communications (DDC) bus is used to communicate between Zilker Labs Digital-DC devices. This dedicated bus provides the communication channel between devices for features such as sequencing, fault spreading, and current sharing. The DDC pin on all Digital-DC devices in an application should be connected together. A pull-up resistor is required on the DDC bus in order to guarantee the rise time as follows:

Rise time = $R_{PU} * C_{LOAD} \approx 1$ µs,

where R_{PU} is the DDC bus pull-up resistance and C_{LOAD} is the bus loading. The pull-up resistor may be tied to VR or to an external 3.3V or 5V supply as long as this voltage is present prior to or during device power-up. As rules of thumb, each device connected to the DDC bus presents approx 10 pF of capacitive loading, and each inch of FR4 PCB trace introduces approx 2 pF. The ideal design will use a central pull-up resistor that is well-matched to the total load capacitance. In power module applications, the user should consider whether to place the pull-up resistor on the module or on the PCB of the end application. The minimum pull-up resistance should be limited to a value that enables any device to assert the bus to a voltage that will ensure a logic 0 (typically 0.8 V at the device monitoring point) given the pull-up voltage (5 V if tied to VR) and the pull-down current capability of the ZL2004 (nominally 4 mA).

6.12 Phase Spreading

When multiple point of load converters share a common DC input supply, it is desirable to adjust the clock phase offset of each device such that not all devices start to switch simultaneously. Setting each converter to start its switching cycle at a different point in time can dramatically reduce input capacitance requirements and efficiency losses. Since the peak current drawn from the input supply is effectively spread out over a period of time, the peak current drawn at any given moment is reduced and the power losses proportional to the I_{RMS}^2 are reduced dramatically.

In order to enable phase spreading, all converters must be synchronized to the same switching clock. The CFG pin is used to set the configuration of the SYNC pin for each device as described in Section 5.6 "Switching Frequency and PLL" on Page 17.

Selecting the phase offset for the device is accomplished by selecting a device address according to the following equation:

Phase offset = device address x 45°

For example:

- A device address of 0x00 or 0x20 would configure no phase offset
- A device address of 0x01 or 0x21 would configure 45° of phase offset
- A device address of 0x02 or 0x22 would configure 90° of phase offset

The phase offset of each device may also be set to any value between 0° and 360° in 22.5° increments via the I^2C/SMBus interface. Refer to Application Note AN33 for further details.

6.13 Output Sequencing

A group of Zilker Labs devices may be configured to power up in a predetermined sequence. This feature is especially useful when powering advanced processors, FPGAs, and ASICs that require one supply to reach its operating voltage prior to another supply reaching its operating voltage in order to avoid latch-up from occurring. Multi-device sequencing can be achieved by configuring each device through the I^2C/SMBus interface or by using Zilker Labs patented autonomous sequencing mode.

Autonomous sequencing mode configures sequencing by using events transmitted between devices over the DDC bus. This mode is not available on current sharing rails.

The sequencing order is determined using each device's SMBus address. Using autonomous sequencing mode (configured using the CFG pin), the devices must be assigned sequential SMBus addresses with no missing addresses in the chain. This mode will also constrain each device to have a phase offset according to its SMBus device address as described in Section 6.12 "Phase Spreading".

Table 24. CFG Pin Configurations for Sequencing and Tracking

R_{CFG}	SYNC Pin Configuration	Sequencing Configuration
10 kΩ	Input	Sequencing is disabled, Tracking is Disabled.
11 kΩ	Auto detect	
12.1 kΩ	Output	
14.7 kΩ	Input	The ZL2004 is configured as the first device in a nested sequencing group. Turn on order is based on the device SMBus address. Tracking is Disabled.
16.2 kΩ	Auto detect	
17.8 kΩ	Output	
21.5 kΩ	Input	The ZL2004 is configured as a last device in a nested sequencing group. Turn on order is based on the device SMBus address. Tracking is Disabled.
23.7 kΩ	Auto detect	
26.1 kΩ	Output	
31.6 kΩ	Input	The ZL2004 is configured as the middle device in a nested sequencing group. Turn on order is based on the device SMBus address. Tracking is Disabled.
34.8 kΩ	Auto detect	
38.3 kΩ	Output	
46.4 kΩ	Input	Sequencing is disabled, Tracking is Enabled
51.1 kΩ	Auto detect	
56.2 kΩ	Output	

The sequencing group will turn on in order starting with the device with the lowest SMBus address and will continue through to turn on each device in the address chain until all devices connected have been turned on. When turning off, the device with the highest SMBus address will turn off first followed in reverse order by the other devices in the group.

Sequencing is configured by connecting a resistor from the CFG pin to ground as described in Table 24. The CFG pin is also used to set the configuration of the SYNC pin as well as to determine the sequencing method and order. Please refer to 5.6 "Switching Frequency and PLL" for more details on the operating parameters of the SYNC pin.

Multiple device sequencing may also be achieved by issuing PMBus commands to assign the preceding device in the sequencing chain as well as the device that will follow in the sequencing chain. This method places fewer restrictions on the device SMBus address (no need of sequential address) and also allows the user to assign any phase offset to any device irrespective of its SMBus address.

The Enable pins of all devices in a sequencing group must be tied together and driven high to initiate a sequenced turn-on of the group. Enable must be driven low to initiate a sequenced turnoff of the group.

Refer to Application Note AN33 for details on sequencing via the I^2C/SMBus interface.

6.14 Fault Spreading

Digital DC devices can be configured to broadcast a fault event over the DDC bus to the other devices in the group. When a non-destructive fault occurs and the device is configured to shut down on a fault, the device will shut down and broadcast the fault event over the DDC bus. The other devices on the DDC bus will shut down together if configured to do so, and will attempt to re-start in their prescribed order if configured to do so.

6.15 Active Current Sharing

Paralleling multiple ZL2004 devices can be used to increase the output current capability of a single power rail. By connecting the DDC pins of each device together and configuring the devices as a current sharing rail, the units will share the current equally within a few percent.

Figure 19 shows a typical connection for three devices.

The ZL2004 uses a low-bandwidth, first-order digital current sharing technique to balance the unequal device output loading by aligning the load lines of member devices to a reference device.

Droop resistance is used to add artificial resistance in the output voltage path to control the slope of the load line curve, calibrating out the physical parasitic mismatches due to power train components and PCB layout.

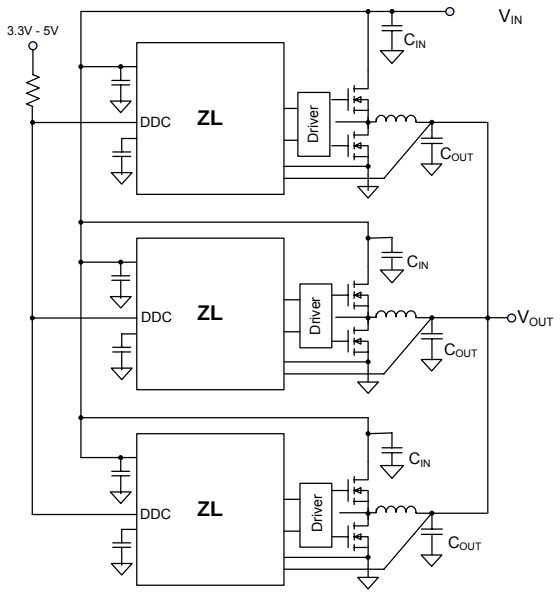


Figure 19. Current Sharing Group

Upon system start-up, the device with the lowest member position as selected in ISHARE_CONFIG is defined as the reference device. The remaining devices are members. The reference device broadcasts its current over the DDC bus. The members use the reference current information to trim their voltages (V_{MEMBER}) to balance the current loading of each device in the system.

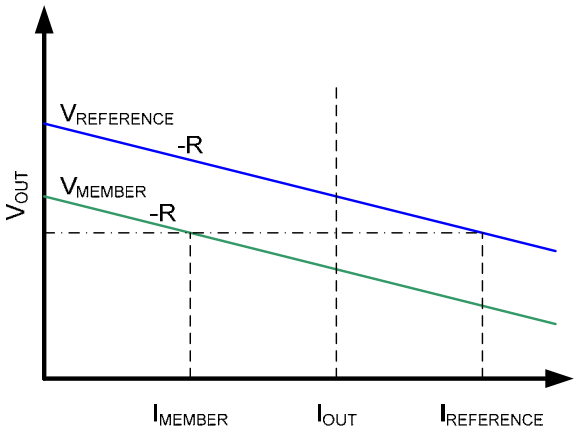


Figure 20. Active Current Sharing

Figure 20 shows that, for load lines with identical slopes, the member voltage is increased towards the reference voltage which closes the gap between the inductor currents.

The relation between reference and member current and voltage is given by the following equation:

$$V_{member} = V_{OUT} + R \times \left(I_{REFERENCE} - I_{MEMBER} \right)$$

where *R* is the value of the droop resistance.

The ISHARE_CONFIG command is used to configure the device for active current sharing. The default setting is a stand-alone non-current sharing device. A current sharing rail can be part of a system sequencing group.

For fault configuration, the current share rail is configured in a quasi-redundant mode. In this mode, when a member device fails, the remaining members will continue to operate and attempt to maintain regulation. The device with the lowest member position will become the reference. If fault spreading is enabled, the current share rail failure is not broadcast until the entire current share rail fails.

Up to eight (8) devices can be configured in a given current sharing rail.

6.16 Phase Adding/Dropping

The ZL2004 allows multiple power converters to be connected in parallel to supply higher load currents than can be addressed using a single-phase design. In doing so, the power converter is optimized at a load current range that requires all phases to be operational. During periods of light loading, it may be beneficial to disable one or more phases in order to eliminate the current drain and switching losses associated with those phases, resulting in higher efficiency.

The ZL2004 offers the ability to add and drop phases using a simple command in response to an observed load current change, enabling the system to continuously optimize overall efficiency across a wide load range. All phases in a current share rail are considered active prior to the current sharing rail ramp to power-good.

Phases can be dropped after power-good is reached. Any member of the current sharing rail can be dropped. If the reference device is dropped, the remaining active device with the lowest member position will become the new reference.

Additionally, any change to the number of members of a current sharing rail will precipitate autonomous phase distribution within the rail where all active phases realign their phase position based on their order within the number of active members.

If the members of a current sharing rail are forced to shut down due to an observed fault, all members of the rail will attempt to re-start simultaneously after the fault has cleared.

6.17 Monitoring via I²C/SMBus

A system controller can monitor a wide variety of different ZL2004 system parameters through the I²C/SMBus interface. The device can monitor for fault conditions by monitoring the SALRT pin, which will be asserted when any number of pre-configured fault conditions occur.

The device can also be monitored continuously for any number of power conversion parameters including but not limited to the following:

- Input voltage
- Output voltage
- Output current
- Internal junction temperature
- Temperature of an external device
- Switching frequency
- Duty cycle

The PMBus Host should respond to SALRT as follows:

1. ZL device pulls SALRT Low.
2. PMBus Host detects that SALRT is now low, performs transmission with Alert Response Address to find which ZL device is pulling SALRT low
3. PMBus Host talks to the ZL device that has pulled SALRT low. The actions that the host performs are up to the System Designer.

If multiple devices are faulting, SALRT will still be low after doing the above steps and will require transmission with the Alert Response Address repeatedly until all faults are cleared.

Please refer to Application Note AN33 for details on how to monitor specific parameters via the I^2C/SMBus interface.

6.18 Temperature Monitoring Using the XTEMP Pin

The ZL2004 supports measurement of an external device temperature using either a thermal diode integrated in a processor, FPGA or ASIC, or using a discrete diode-connected 2N3904 NPN transistor. Figure 21 illustrates the typical connections required.

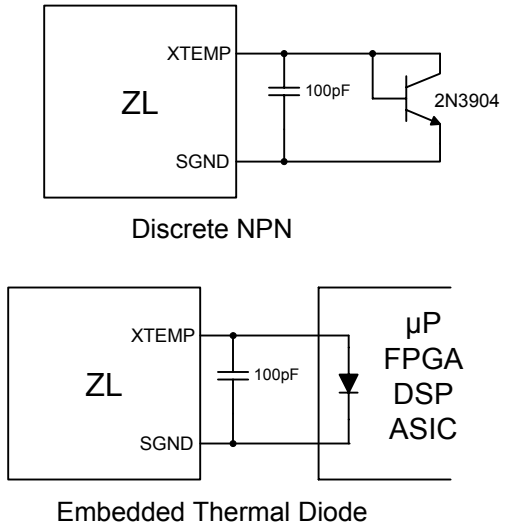


Figure 21. External Temperature Monitoring

6.19 *Snapshot*™ Parameter Capture

The ZL2004 offers a special mechanism that enables the user to capture parametric data during normal operation or following a fault. The Snapshot functionality is enabled by setting bit 1 of MISC_CONFIG to 1.

The Snapshot feature enables the user to read the parameters listed in Table 25 via a block read transfer through the SMBus. This can be done during normal operation, although it should be noted that reading the 22 bytes will occupy the SMBus for some time.

The SNAPSHOT_CONTROL command enables the user to store the snapshot parameters to Flash memory in response to a pending fault as well as to read the stored data from Flash memory after a fault has occurred. Table 26 describes the usage of this command. Automatic writes to Flash memory following a fault are triggered when any fault threshold level is exceeded, provided that the specific fault's response is to shut down (writing to Flash memory is not allowed if the device is configured to re-try following the specific fault condition).

Table 25. Snapshot Parameters

Byte	Description	Format
31:22	Reserved	Linear
21:20	Vin	Linear
19:18	Vout	Vout Linear
17:16	Iout,avg	Linear
15:14	Iout,peak	Linear
13:12	Duty cycle	Linear
11:10	Internal temp	Linear
9:8	External temp	Linear
7:6	fsw	Linear
5	Vout status	Byte
4	Iout status	Byte
3	Input status	Byte
2	Temp status	Byte
1	CML status	Byte
0	Mfr specific status	Byte

It should also be noted that the device's V_{DD} voltage must be maintained during the time when the device is writing the data to Flash memory; a process that requires between 700-1400 µs depending on whether the data is set up for a block write. Undesirable results may be observed if the device's V_{DD} supply drops below 3.0 V during this process.

Table 26. SNAPSHOT_CONTROL Command

Data Value	Description
1	Copies current SNAPSHOT values from Flash memory to RAM for immediate access using SNAPSHOT command.
2	Writes current SNAPSHOT values to Flash memory. Only available when device is disabled.

In the event that the device experiences a fault and power is lost, the user can extract the last SNAPSHOT parameters stored during the fault by writing a 1 to SNAPSHOT_CONTROL (transfers data from Flash memory to RAM) and then issuing a SNAPSHOT command (reads data from RAM via SMBus).

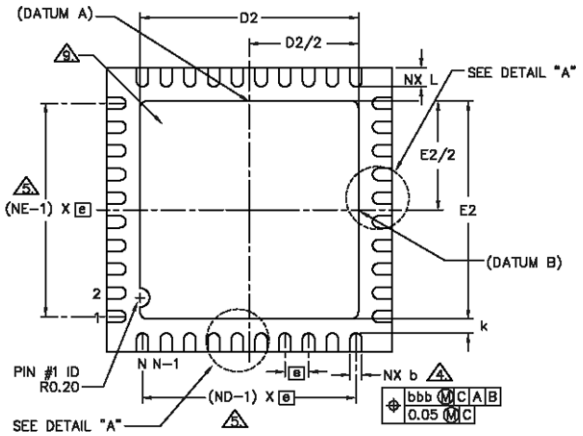
6.20 Non-Volatile Memory and Device Security Features

The ZL2004 has internal non-volatile memory where user configurations are stored. Integrated security measures ensure that the user can only restore the device to a level that has been made available to them. Refer to Section 5.3"Start-up Procedure," for details on how the device loads stored values from internal memory during start-up. During the initialization process, the ZL2004 checks for stored values contained in its internal non-volatile memory. The ZL2004 offers two internal memory storage units that are accessible by the user as follows:

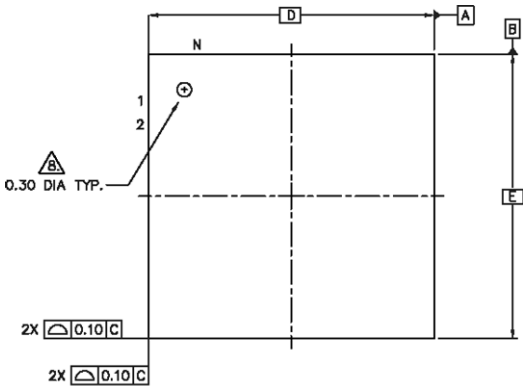
1. *Default Store*: A power supply module manufacturer may want to protect the module from damage by preventing the user from being able to modify certain values that are related to the physical construction of the module. In this case, the module manufacturer would use the Default Store and would allow the user to restore the device to its default setting but would restrict the user from restoring the device to the factory settings.
2. *User Store*: The manufacturer of a piece of equipment may want to provide the ability to modify certain power supply settings while still protecting the equipment from modifying values that can lead to a system level fault. The equipment manufacturer would use the User Store to achieve this goal.

Please refer to Application Note AN33 for details on how to set specific security measures via the I^2C/SMBus interface.

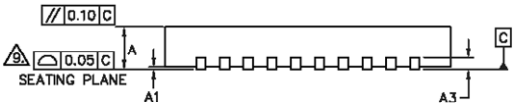
7. Package Dimensions



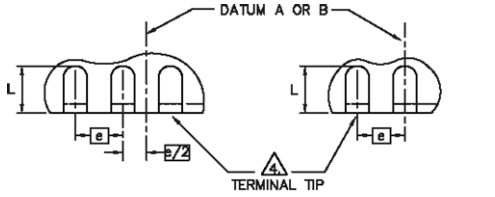
BOTTOM VIEW



TOP VIEW



SIDE VIEW



EVEN TERMINAL/SIDE ODD TERMINAL/SIDE

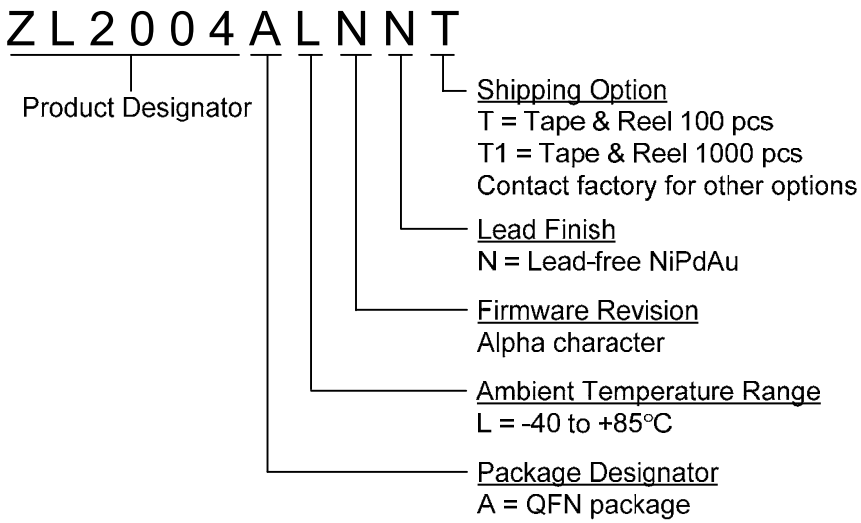
DETAIL "A"

Notes:

1. Dimensions and tolerances conform to ASME Y14.5M – 1994.
2. All dimensions are in millimeters, θ is in degrees.
3. N is the total number of terminals.
4. Dimension b applies to metalized terminal and is measured between 0.15 and 0.33 mm from terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension b should not be measured in that radius area.
5. ND and NE refer to the number of terminals on each D and E side respectively.
6. Max package warpage is 0.05 mm.
7. Maximum allowable burrs is 0.076 mm in all directions.
8. Pin #1 ID on top will be laser marked.
9. Bilateral coplanarity zone applies to the exposed heat sink slug as well as the terminals.
10. This drawing conforms to JEDEC registered outline MO- 220.

SYMBOL	DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A		0.85	0.90	
A1	0.00	0.01	0.05	
A3		0.20 REF		
θ	0	-	12	2
k		0.20 MIN		
D		5.0 BSC		
E		5.0 BSC		
e		0.50 BSC		
N		32		3
ND		8		5
NE		8		5
L	0.30	0.40	0.50	
b	0.18	0.23	0.30	4
D2	3.35	3.50	3.75	
E2	3.35	3.50	3.75	

8. Ordering Information



9. Related Tools and Documentation

The following application support documents and tools are available to help simplify your design.

Item	Description
ZL2004EVK1	Evaluation Board – 40A single phase
AN33	Application Note: Digital-DC PMBus Command Set
AN34	Application Note: Digital-DC Current Sharing
AN35	Application Note: Digital-DC Control Loop Compensation

10. Revision History

Rev. #	Description	Date
1.0	Data sheet initial release	March 2008
1.1	Removed DDC Address references from Section 6.11	April 2008
1.2	Updated Ordering Information Improved readability in current sharing description	May 2008
1.3	Added comment that a device set up for tracking must have both Alternate Ramp Control and Precise Ramp-Up Delay disabled on Page 32. Clarified DDC pull-up voltage requirement on Page 35.	June 2008
1.4	Corrected frequency values in Table 14. Corrected Figure 14. Updated Adaptive Frequency Control description on Page 28. Removed Bootstrap Capacitor Selection section. Added Driver Selection section.	August 2008
FN6846.0	Assigned file number FN6846 to datasheet as this will be the first release with an Intersil file number. Replaced header and footer with Intersil header and footer. Updated disclaimer information to read “Intersil and it’s subsidiaries including Zilker Labs, Inc.” No changes to datasheet content	February 2009

Zilker Labs, Inc.
4301 Westbank Drive
Building A-100
Austin, TX 78746

Tel: 512-382-8300
Fax: 512-382-8329

www.zilkerlabs.com

This document contains information on a product under development. Specifications are subject to change without notice. Pricing, specifications and availability are subject to change without notice. Please see www.zilkerlabs.com for updated information. This product is not intended for use in connection with any high-risk activity, including without limitation, air travel, life critical medical operations, nuclear facilities or equipment, or the like.

The reference designs contained in this document are for reference and example purposes only. THE REFERENCE DESIGNS ARE PROVIDED "AS IS" AND "WITH ALL FAULTS" AND INTERSIL CORPORATION AND IT'S SUBSIDIARIES INCLUDING ZILKER LABS, INC. DISCLAIMS ALL WARRANTIES, WHETHER EXPRESS OR IMPLIED. ZILKER LABS SHALL NOT BE LIABLE FOR ANY DAMAGES, WHETHER DIRECT, INDIRECT, CONSEQUENTIAL (INCLUDING LOSS OF PROFITS), OR OTHERWISE, RESULTING FROM THE REFERENCE DESIGNS OR ANY USE THEREOF. Any use of such reference designs is at your own risk and you agree to indemnify Intersil Corporation and it's subsidiaries including Zilker Labs, Inc. for any damages resulting from such use.