FEATURES

- Wide input application 1.5V—16V
- Single 3.3V or single 5V application
- Output Voltage Range: 0.6V to 0.75*Vin
- 0.5% accurate Reference Voltage
- Programmable Switching Frequency up to 1.5MHz
- Programmable Soft-Start
- Enable input with Voltage Monitoring Capability
- Remote Sense Amplifier with True Converter Voltage Sensing
- Thermally compensated Hiccup Mode Over Current Protection
- Over-voltage protection
- Pre-Bias Start up
- Body Braking to improve transient
- Integrated MOSFET drivers and Bootstrap diode
- Operating temp: -40°C<Tj<125°C
- Thermal Shut Down
- Power Good Output with Window Comparator
- Small Size 7.7mmx7.7mm LGA
- Pb-Free (RoHS Compliant)

DESCRIPTION

The iP1827 ***iPOWIR***™ is an easy-to-use, fully integrated and highly efficient DC/DC regulator. The onboard PWM controller and MOSFETs make iP1827 a space-efficient solution, providing accurate power delivery for low output voltage and high current applications.

iP1827 is a versatile regulator which offers programmability of switching frequency and current limit while operating in wide input and output voltage range.

The switching frequency is programmable from 250kHz to 1.5MHz for an optimum solution.

It also features important protection functions, such as Pre-Bias startup, hiccup current limit and thermal shutdown to give required system level security in the event of fault conditions.

APPLICATIONS

- Server Application
- Netcom Applications
- Embedded Telecom Systems
- Distributed Point of Load Power Architectures

BASIC APPLICATION

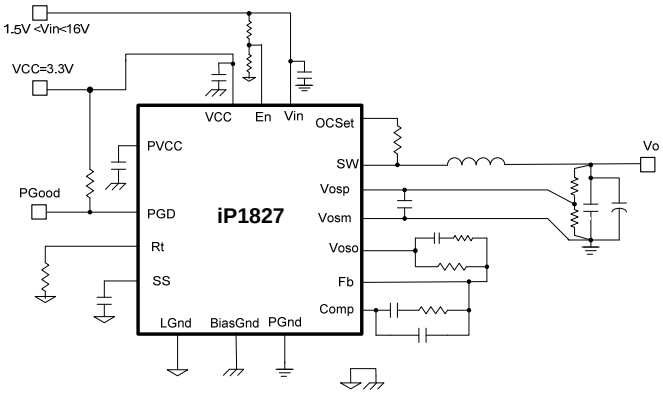


Figure 1 : iP1827 Basic Application Circuit

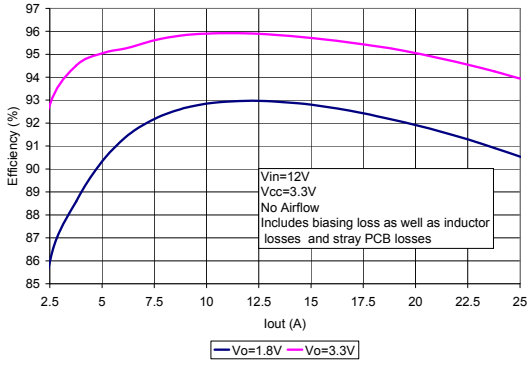


Figure 2: iP1827 Efficiency

PIN DIAGRAM

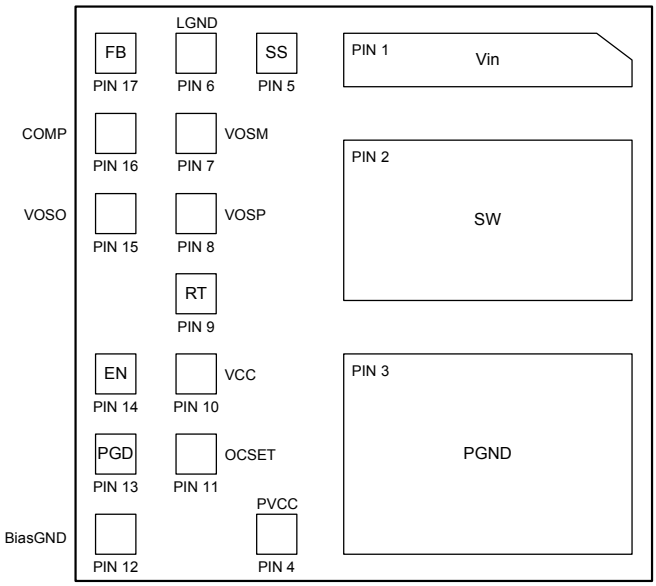


Figure 3: iP1827 Package Bottom View
7.65mm x 7.65mm LGA

ORDERING INFORMATION

Package	Tape and Reel Qty	Part Number
LGA (7.65mm x 7.65mm body)	2000	**iP1827TRPbF**

FUNCTIONAL BLOCK DIAGRAM

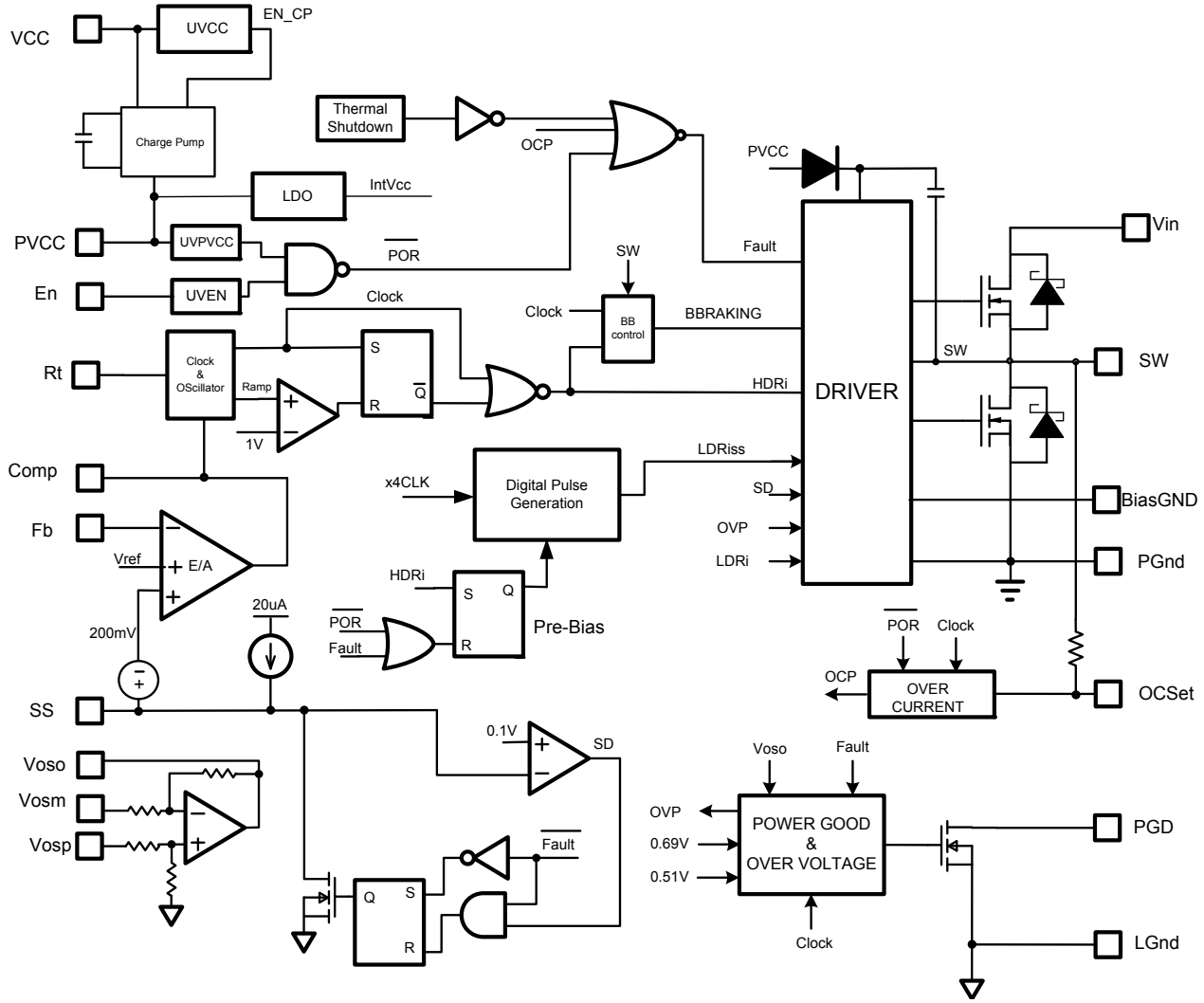


Figure 4: iP1827 Simplified Block Diagram

TYPICAL APPLICATION DIAGRAM

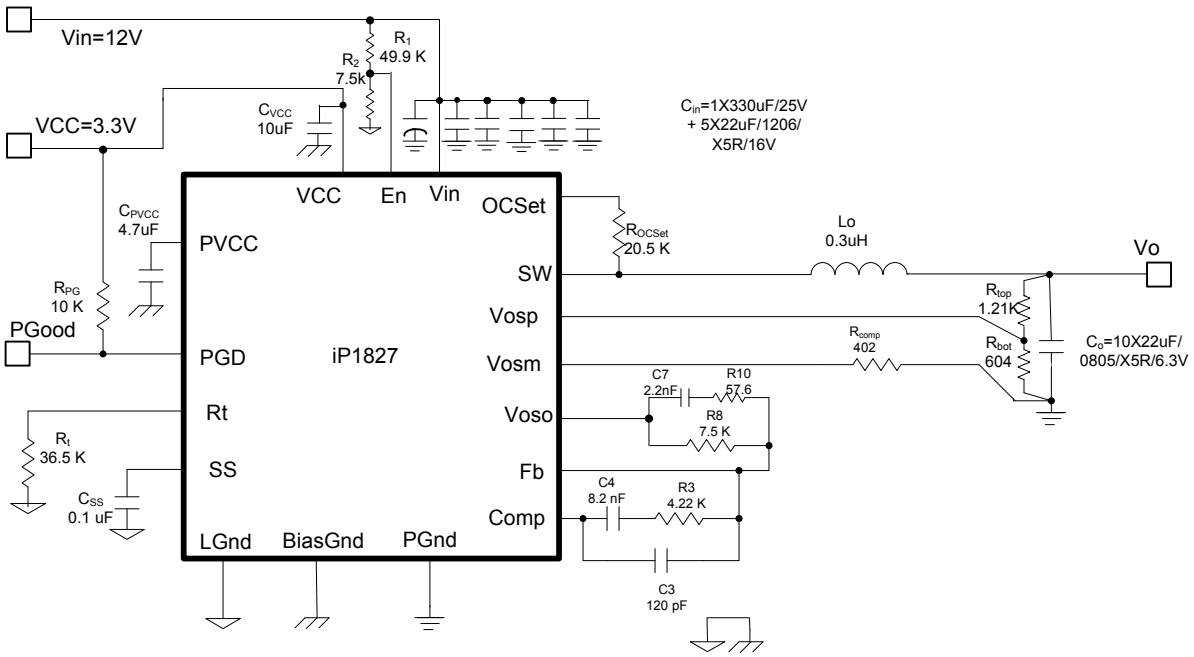


Figure 5: iP1827 Application Circuit Diagram for a 12V to 1.8V, 25A Point of Load Converter

PIN DESCRIPTIONS

PIN #	PIN NAME	PIN DESCRIPTION
1	VIN	Input voltage for power stage. Bypass capacitors between VIN and PGND should be connected very close to this pin and PGND (pin 3).
2	SW	Switch node. This pin is connected to the output inductor.
3	PGND	Power ground. This pin should be connected to the system's power ground plane. Bypass capacitors between VIN and PGND should be connected very close to VIN pin (pin 1) and this pin.
4	PVCC	Output of internal charge pump. Connect a 4.7uF to 10uF capacitor from this pin to local bias PGND (pin 12), very close to the pins. External 5V may also be connected to this pin for operation from 5V bias.
5	SS	Soft start; a capacitor from SS and LGND sets the startup timing.
6	LGND	Signal ground for internal reference and control circuitry.
7	VOSM	Remote Sense Amplifier input. Connect to ground at the load.
8	VOSP	Remote Sense Amplifier input. Connect to output at the load.
9	RT	Use an external resistor from this pin to GND to set the switching frequency, very close to the pin.
10	VCC	Input bias voltage for internal IC. This also powers the charge pump circuit in the IC. Connect a 10uF capacitor from this pin to local bias PGND (pin 12), very close to the pins. For 5V bias operation, this pin should be tied to ground.
11	OCSET	Current Limit setpoint. A resistor may be connected from this pin to SW pin to set thresholds lower than those allowed by maximum current rating of the device.
12	BIASGND	This pin serves as a ground for the MOSFET drivers. It should be connected to the negative terminal of the bias voltage at the VCC and/or PVCC capacitors.
13	PGD	Power Good status pin. Output is open collector. Connect a pull up resistor from this pin to VCC.
14	EN	Enable pin to turn on and off the IC.
15	VOSO	Remote Sense Amplifier Output; also forms an input to the power good comparator and overvoltage comparator.
16	COMP	Output of error amplifier. An external resistor and capacitor network is typically connected from this pin to FB to provide loop compensation.
17	FB	Inverting input to the error amplifier. This pin is connected directly to the output of the regulator or to the output of the remote sense amplifier, via resistor divider to set the output voltage and provide feedback to the error amplifier.

ABSOLUTE MAXIMUM RATINGS

VIN	-0.3V to 25V
VCC	-0.3V to 3.9V
PVCC	-0.3V to 8V (Note 2)
SW	-0.3V to 25V (DC), -4V to 25V (AC, 100ns)
BOOT	-0.3V to 33V
Input/output pins, except PGD, Vosp and Voso	-0.3V to VCC + 0.3V
PGD, Vosp and Voso	-0.3V to PVCC + 0.3V (Note 2)
PGND to LGND, BIASGND to LGND, Vosm to LGND	-0.3V to + 0.3V
Storage Temperature Range	-55°C to 150°C
Junction Temperature Range	-40°C to 150°C
ESD Classification	JEDEC Class 1C (1KV)
Moisture Sensitivity level	JEDEC Level 3@250°C

Note 1: Must not exceed 8V.
Note 2: PVCC must not exceed 7.5V for Junction Temperature between -10°C and -40°C.

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied. These devices are ESD sensitive, observe handling precautions to prevent electrostatic discharge damage.

ELECTRICAL SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

SYMBOL	DEFINITION	MIN	MAX	UNITS
VIN	Input Voltage	1.5	16	V
PVCC	Supply Voltage	4.5	7.5	
VCC	Supply Voltage	3.13	3.46	
Boot to SW	Supply Voltage	4.5	7.5	
V_O	Output Voltage	0.6	0.75 Vin	
I_O	Output Current	0	25	A
Fs	Switching Frequency	225	1650	kHz
T_J	Junction Temperature	-40	125	°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, these specification apply over, 1.5V < Vin < 16V, 3.13V < Vcc < 3.46V. 0°C < T_J < 125°C. Typical values are specified at T_A = 25°C.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Power Loss						
Power Loss	P_{LOSS}	V_{in} = 12V, V_{CC} = 3.3V, V_O = 1.8V, I_O = 25A, Fs = 600kHz, L=0.3uH, T_A = 25°C		4.2		W
MOSFET $R_{ds(on)}$						
Top Switch	Rds(on)_Top	$V_{Boot} - V_{SW}$ = 5V, I_D = 5A, Tj = 25°C		4.8	6	mΩ
Bottom Switch		PVCC = 5V, I_D = 25A, Tj = 25°C		2.3	2.7	
		VCC = 3.3V, I_D = 25A, Tj = 25°C		1.8	2.2	
Reference Voltage						
Feedback Voltage	V_{FB}			0.6		V
Accuracy		40°C < Tj < 105°C	-0.5		+0.5	%
		-40°C < Tj < 125°C, Note 3	-1.5		+1.5	
Supply Current						
VCC Supply Current (Standby)	$I_{CC(Standby)}$	Enable low, No Switching, VCC = 3.3V		400	600	uA
VCC Supply Current (Dyn)	$I_{CC(Dyn)}$	Enable high, Fs = 500kHz, VCC = 3.3V			75	mA
PVCC Supply Current (Standby)	$I_{PCC(Standby)}$	Enable low, No Switching, PVCC = 5V		150	200	uA
PVCC Supply Current (Dyn)	$I_{PCC(Dyn)}$	Enable high, Fs = 500kHz, PVCC = 5V			30	mA
Under Voltage Lockout						
PVCC – Start – Threshold	PVCC_UVLO_Start	PVCC Rising Trip Level	4.0	4.2	4.4	V
PVCC – Stop – Threshold	PVCC_UVLO_Stop	PVCC Falling Trip Level	3.7	3.9	4.1	

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
VCC – Start – Threshold	VCC_UVLO_Start	VCC Rising Trip Level	2.6	2.8	3.1	V
VCC – Stop – Threshold	VCC_UVLO_Stop	VCC Falling Trip Level	2	2.2	2.5	
Enable – Start – Threshold	Enable_UVLO_Start	Supply ramping up	1.14	1.2	1.36	
Enable – Stop – Threshold	Enable_UVLO_Stop	Supply ramping down	0.9	1.0	1.06	
Oscillator						
Rt Voltage				1		V
Frequency Range	F_S		450	500	550	kHz
			1350	1500	1650	
Ramp Offset	Ramp (os)	Note 3		0.4		V
Min Pulse Width	Dmin (ctrl)	Note 3			50	ns
Fixed Off Time		Note 3		130	200	ns
Max Duty Cycle	Dmax		75			%
Error Amplifier						
Input Bias Current	IFb(E/A)		-1		+1	µA
Input Bias Current	IVp(E/A)		-1		+1	µA
Sink Current	Isink(E/A)		0.6	0.9	1.2	mA
Source Current	Isource(E/A)		5	8	12	mA
Slew Rate	SR	Note 3	7	12	20	V/µs
Gain-Bandwidth Product	GBWP	Note 3	20	30	40	MHz
DC Gain	Gain	Note 3	100	110	120	dB
Maximum Voltage	Vmax(E/A)		1.7	2	2.3	V
Minimum Voltage	Vmin(E/A)				100	mV
Remote Sense Differential Amplifier						
Unity Gain Bandwidth	BW_RS	Note 3	3	6.4	9	MHz
DC Gain	Gain_RS	Note 3		110		dB
Offset Voltage	Offset_RS		-3	0	3	mV
Source Current	Isource_RS		3	9	20	mA
Sink Current	Isink_RS		0.4	1	2	mA
Slew Rate	Slew_RS	Note 3, Cload = 100pF	2	4	8	V/µs
VOSEN+ input impedance	Rin_RS+		70	120	200	kohm
VOSEN- input impedance	Rin_RS-	Note 3	70	120	200	kohm
Maximum Voltage	Vmax_RS	V(PVCC) – V(Vosp)	0.5	1	1.5	V
Minimum Voltage	Min_RS			50		mV
Soft Start						
Soft Start Charge Current	Iss_Charg		14	20	26	µA
Clamp Voltage	Vss (Clamp)		3	3.3	3.6	µA
Offset Voltage	Vss (offset)		100	170	250	mV

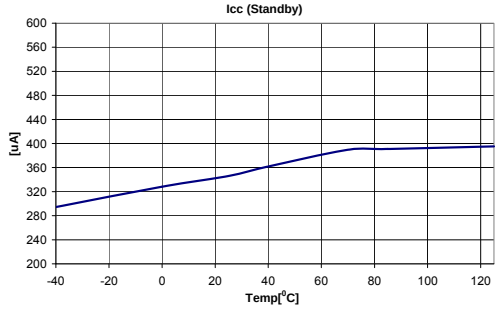
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Shutdown Output Threshold	SD				0.1	V
Bootstrap Diode						
Forward Voltage		I(Boot) = 30mA, Note 3	360	520	960	mV
Switch Node						
SW Leakage Current	Isw	SW = 0V, Enable = 0V			3	µA
Charge Pump (PVCC)						
Output Voltage	PVCC	VCC = 3.3V, Fs = 1500 kHz, Cload = 2.2uF	5.7	6.15	6.5	V
Oscillator Frequency	Fs_CP			Fs		kHz
Body Braking						
BB Threshold	BB_threshold	Fb > Vref, Sw duty cycle		0		%
Power Good						
Power Good Lower Threshold	VPG (lower)	Voso rising	0.48	0.51	0.54	V
Lower Threshold Delay	VPG (lower)_Dly	Voso rising		256/Fs		s
PGood Voltage Low	PG (voltage)	I_{PGood} = -5mA			0.5	V
Leakage Current	$I_{LEAKAGE}$			0	1	µA
Over Voltage Protection (OVP)						
OVP Trip Threshold	OVP (trip)	Voso rising	0.67	0.7	0.73	V
OVP Fault Prop Delay	OVP (delay)	Voso rising, Note 3			200	ns
Over-Current Protection						
OC Trip Current	I_{TRIP}	OC set pin left floating, PVCC = 6.5V, TJ = 85°C	36	40	44	A
SS Off Time	SS_Hiccup	Note 3		4096/ Fs		s
Thermal Shutdown						
Thermal Shutdown		Note 3		145		°C
Hysteresis		Note 3		20		°C

Notes

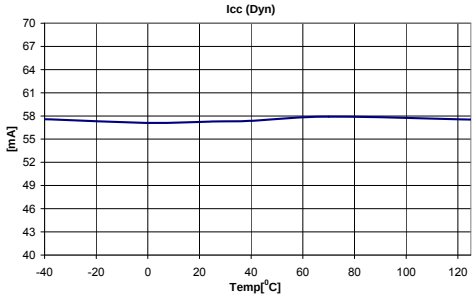
3. Guaranteed by design but not tested in production.

TYPICAL OPERATING CHARACTERISTICS (-40°C - 125°C)

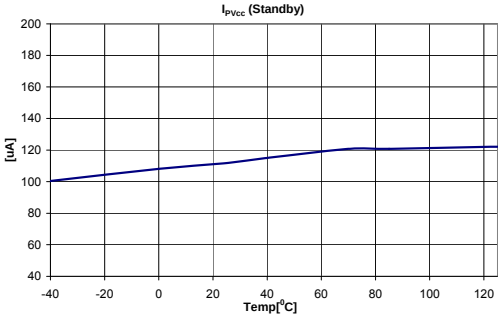
Icc (Standby)



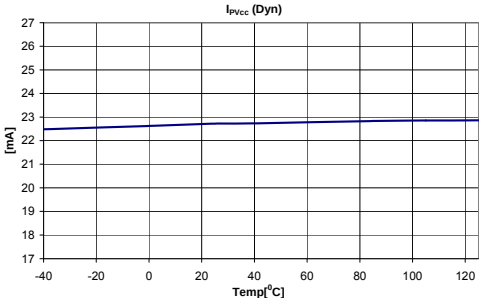
Icc (Dyn)



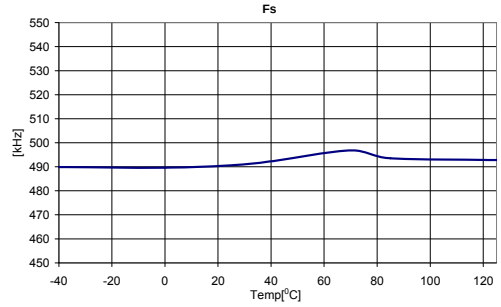
I_{PVcc} (Standby)



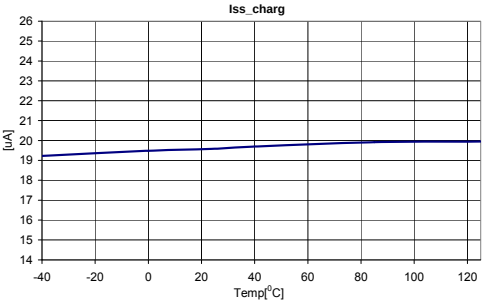
I_{PVcc} (Dyn)



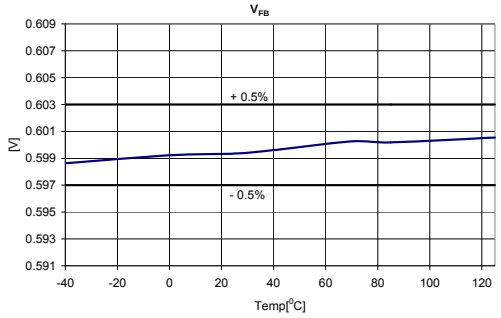
Fs



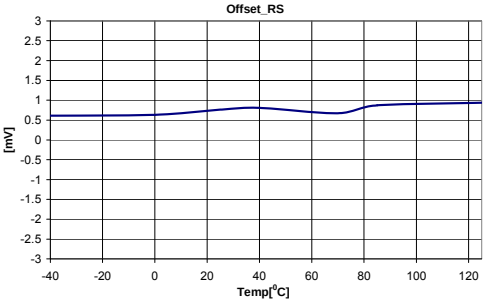
Iss_charg



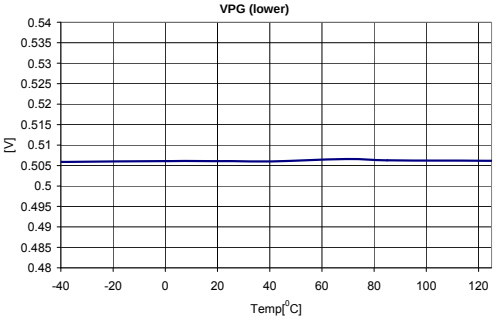
V_{FB}



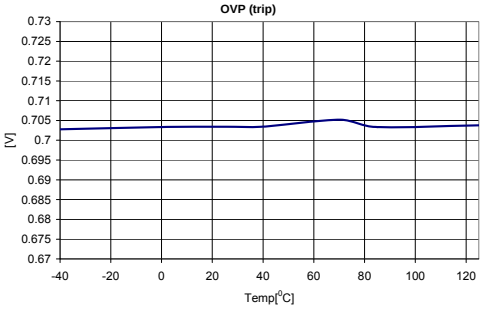
Offset_RS



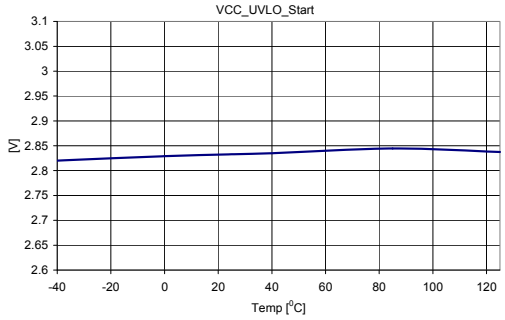
VPG (lower)

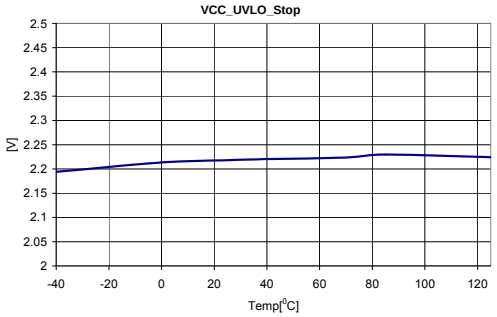


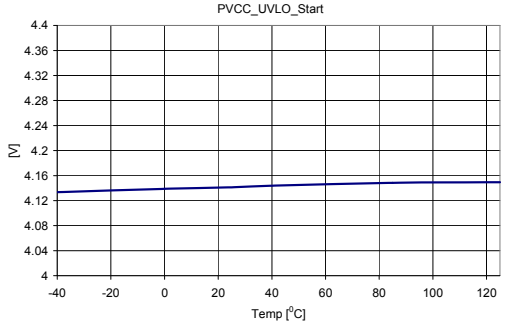
OVP (trip)

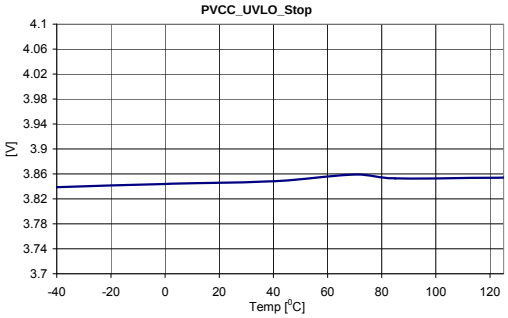


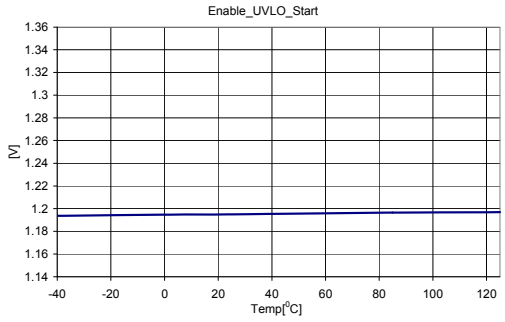
TYPICAL OPERATING CHARACTERISTICS (-40°C - 125°C)

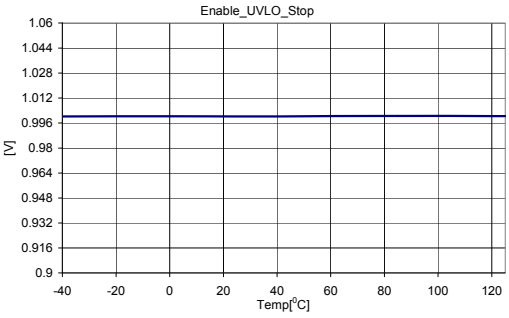


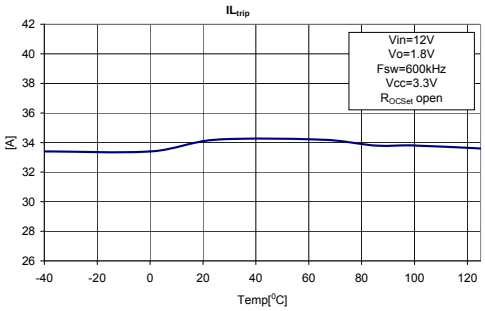


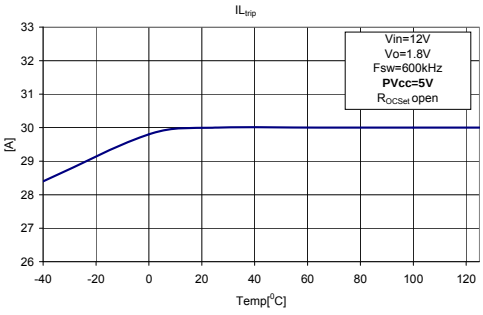




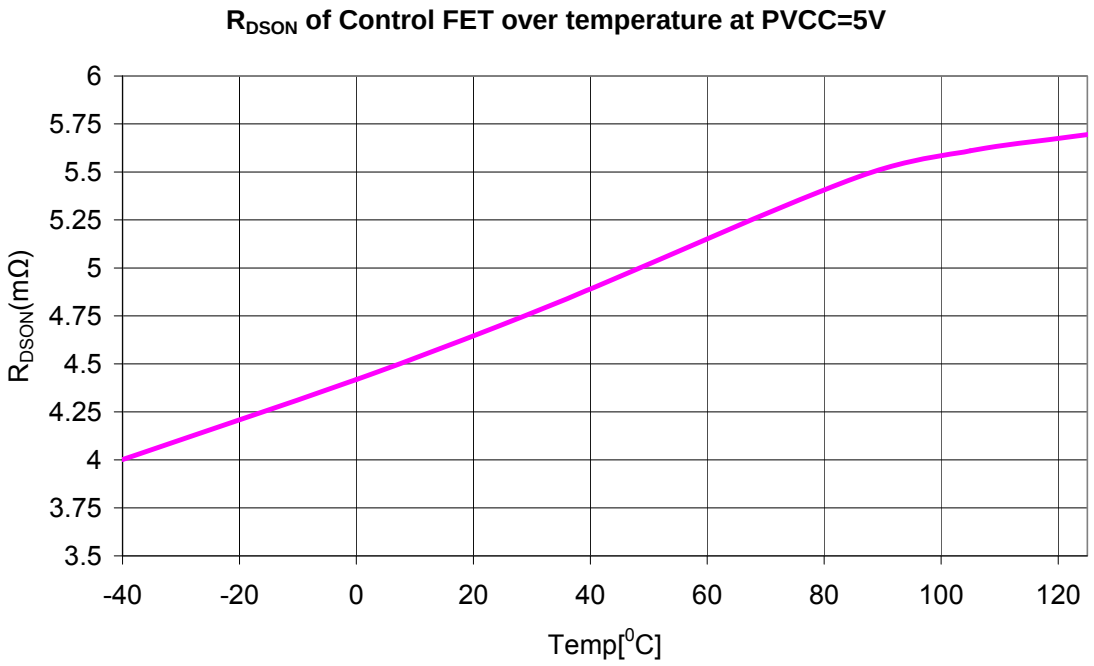


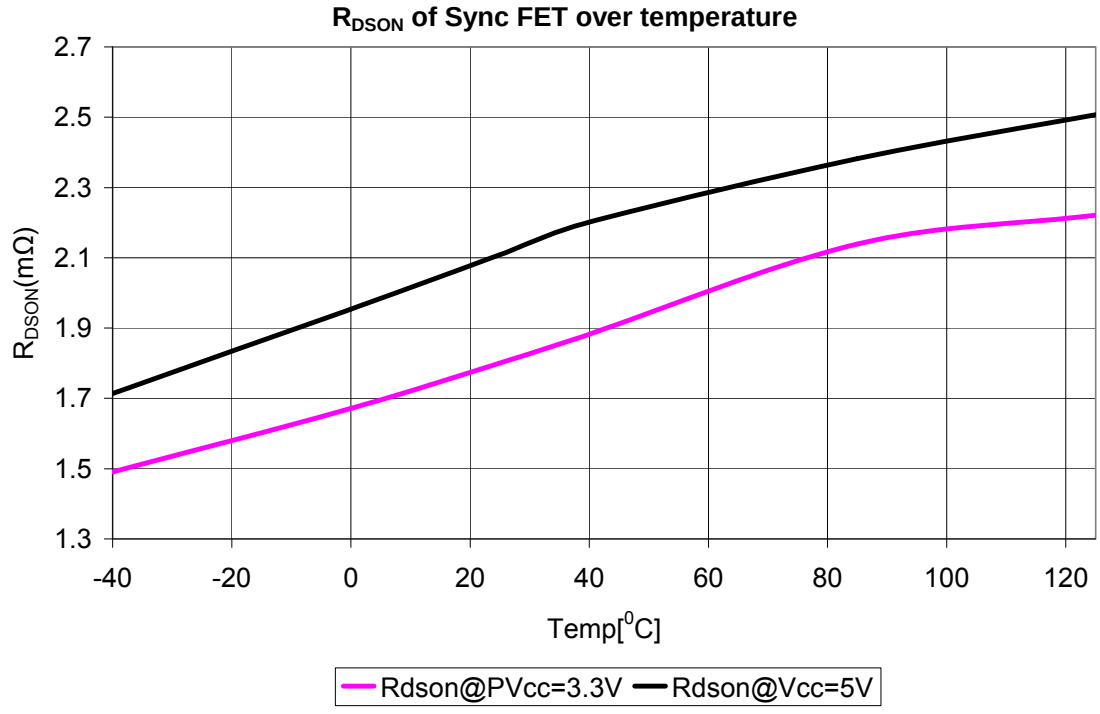






TYPICAL OPERATING CHARACTERISTICS (-40°C - 125°C)





THEORY OF OPERATION

INTRODUCTION

The iP1827 uses a PWM voltage mode control scheme with external compensation to provide good noise immunity and maximum flexibility in selecting inductor values and capacitor types.

The switching frequency is programmable from 250kHz to 1.5MHz and provides the capability of optimizing the design in terms of size and performance.

iP1827 provides precisely regulated output voltage programmed from 0.6V to 0.75*Vin using two external resistors. The iP1827 is capable of operating with either a 3.3V Vcc bias voltage (3.13V to 3.46V) or a PVcc bias voltage from 4.5V to 7.5V, allowing an extended operating input voltage range from 1.5V to 16V.

The device utilizes the on-resistance of the low side MOSFET as the current sense element; this method enhances the converter's efficiency and reduces cost by eliminating the need for external current sense resistor.

iP1827 includes two low $R_{ds(on)}$ MOSFETs using IR's HEXFET technology. These are specifically designed for high efficiency applications.

BIASING THE IP1827

The iP1827 offers flexibility in choosing the bias supply voltage as it is capable of operating with a 5V bias voltage as well as a 3.3V bias voltage (Figure 1 and Figure 32) If it is preferred to use a 5V bias voltage, this should be applied between the PVcc pin and the local bias PGnd (pin 12), with the Vcc pin tied to the local bias PGnd also.

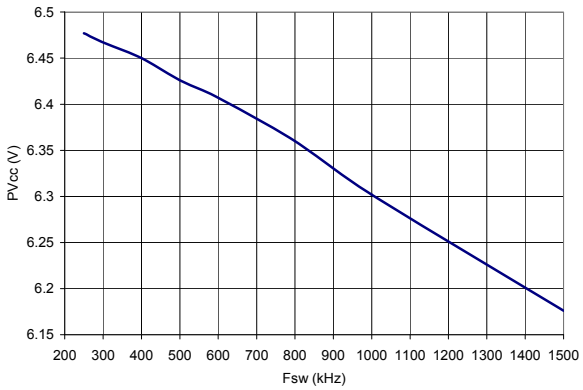


Figure 6: PVcc v/s Switching Frequency (Fsw) with Vcc=3.3V

Alternatively, if operation from 3.3V bias is desired, the 3.3V supply should be applied between Vcc and the local bias PGnd. An internal charge-pump whose output is tied to PVcc, roughly doubles this Vcc voltage. This should be preferred for high current applications which may benefit from the lower Rds(on) on account of the higher PVcc (almost 6.3V, from Figure 6), which forms the supply to the gate drivers.

UNDER-VOLTAGE LOCKOUT AND POR

The under-voltage lockout circuit monitors the input supply PVcc and the Enable input. It ensures that the MOSFET driver outputs remain in the off state whenever either of these two signals drop below the set thresholds. Normal operation resumes once PVcc and Enable rise above their thresholds.

The POR (Power On Ready) signal is generated when all these signals reach the valid logic level (see system block diagram). When the POR is asserted the soft start sequence starts (see soft start section).

ENABLE

The Enable feature allows another level of flexibility for start up. The Enable has precise threshold which is internally monitored by Under-Voltage Lockout (UVLO) circuit. Therefore, the iP1827 will turn on only when the voltage at the Enable pin exceeds this threshold, typically, 1.2V.

If the input to the Enable pin is derived from the bus voltage by a suitably programmed resistive divider, it can be ensured that the iP1827 does not turn on until the bus voltage reaches the desired level. Only after the bus voltage reaches or exceeds this level will the voltage at Enable pin exceed its threshold, thus enabling the iP1827. Therefore, in addition to being a logic input pin to enable the iP1827, the Enable feature, with its precise threshold, also allows the user to implement an Under-Voltage Lockout for the bus voltage V_{in}. This is desirable particularly for high output voltage applications, where we might want the iP1827 to be disabled at least until V_{in} exceeds the desired output voltage level.

Figure 7a shows the startup sequence with the Enable used to implement a precise under-voltage lockout for V_{in}. Figure 7b. shows the recommended start-up sequence for iP1827, when Enable is used as a logic input.

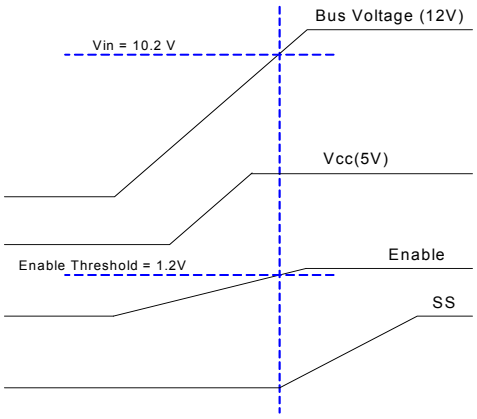


Figure 7a: Normal Start up, Device turns on when the Bus voltage reaches 10.2V

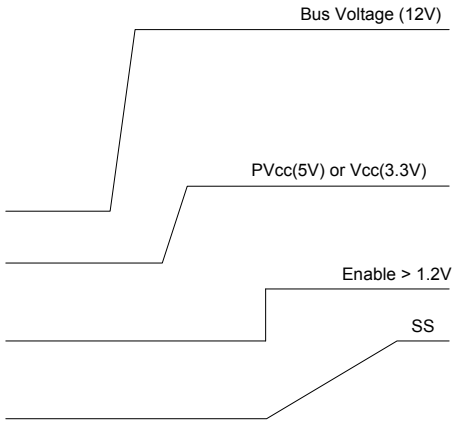


Figure 7b: Recommended startup sequence with Vcc or PVcc

PRE-BIAS STARTUP

iP1827 is able to start up into pre-charged output, which prevents oscillation and disturbances of the output voltage.

The output starts in asynchronous fashion and keeps the synchronous MOSFET off until the first gate signal for control MOSFET is generated, following which, the synchronous MOSFET starts with a narrow duty cycle of 12.5% and gradually increases its duty cycle in steps of 12.5%, with 32 cycles at each step until the end of pre-bias.

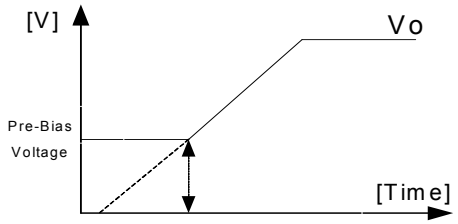


Figure 8: Pre-Bias startup

At the end of the pre-bias stage, the synchronous MOSFET is switched complementary to the Control MOSFET. Figure 8 shows a typical Pre-Bias condition at start up.

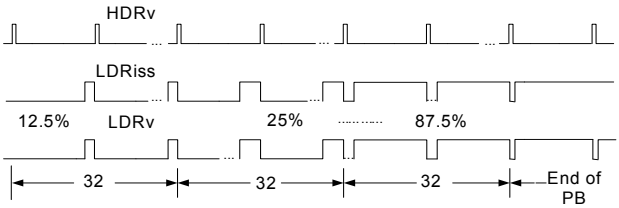


Figure 9: Pre-Bias startup pulses

SOFT-START

The iP1827 has a programmable soft-start to control the output voltage rise and to limit the current surge at the start-up. To ensure correct start-up, the soft-start sequence initiates when the Enable and Vcc rise above their UVLO thresholds and generate the Power On Ready (POR) signal. The internal current source (typically 20uA) charges the external capacitor Css linearly from 0V to Vcc. Figure 10 shows the waveforms during the soft start.

The start up time can be estimated by:

$$T_{start} = \frac{(0.8 - 0.2) * C_{SS}}{I_{ss}} \qquad (1)$$

During the soft start the OCP is enabled to protect the device for any short circuit and over current condition.

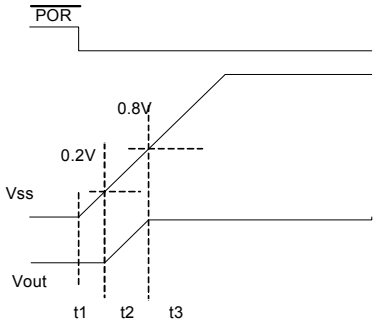


Figure 10: Theoretical operation waveforms during soft-start

OPERATING FREQUENCY

The switching frequency can be programmed between 250kHz – 1500kHz by connecting an external resistor from R_T pin to Gnd. Table 1 tabulates the oscillator frequency versus R_T.

TABLE 1: SWITCHING FREQUENCY VS. EXTERNAL RESISTOR (R_T)

Fsw (kHz)	R_T (kohm)
250	88.7
300	73.2
400	54.9
450	48.7
500	44.2
600	36.5
800	27.4
1000	22.1
1500	14

SHUTDOWN

The iP1827 can be shutdown by pulling the Enable pin below its 1 V threshold. This will tri-state both, the high side driver as well as the low side driver.

TEMPERATURE-COMPENSATED OVER-CURRENT PROTECTION

The over current protection is performed by sensing current through the $R_{DS(on)}$ of low side MOSFET. This method enhances the converter's efficiency and reduces cost by eliminating a current sense resistor. As shown in Figure 11, an external resistor (R_{OCSet}) is connected between OCSet pin and the switch node (SW) which sets the current limit set point.

An internal current source sources current (I_{OCSet}) out of the *OCSet* pin. The internal current source develops a voltage across *ROCSet*. When the low side MOSFET is turned on, the inductor current flows through Q2 and results in a voltage at OCSet which is given by:

$$V_{OCSet} = (I_{OCSet} * R_{OCSet}) - (R_{DS(on)} * I_L) \qquad (2)$$

An over current is detected if the OCSet pin goes below ground. Hence, at the current limit threshold, V_{OCset}=0. Then, for a current limit setting I_{Ltrip}, R_{OCSet} is calculated as follows:

$$R_{OCSet} = \frac{R_{DS(on)} * I_{Ltrip}}{I_{OCSet}} \qquad (3)$$

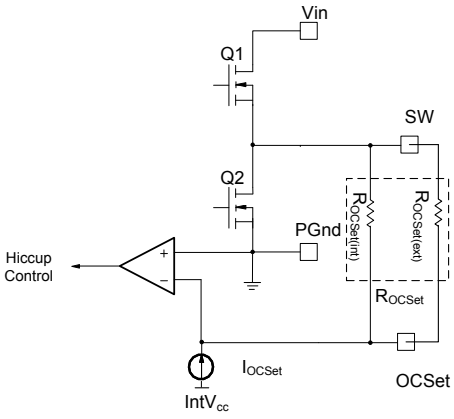


Figure 11: Connection of over-current sensing resistor

It should be noted that the iP1827 uses a temperature compensated overcurrent protection scheme, i.e., I_{OCSet} varies with temperature with the same temperature coeffecient as $R_{DS(on)}$, so that I_{Ltrip} depends only on Rocset and is independent of temperature.

The value of Rocset calculated above is realized as a parallel combination of an internal 2.7K resistor and an external resistor connected between the Rocset and SW pins. Table 2 shows the selection of the external Rocset resistor for various values of the trip load current I_{otrip} at Vcc = 3.3V.

An overcorrect detection trips the OCP comparator, latches OCP signal and cycles the soft start function in hiccup mode. The hiccup is performed by shorting the soft-start capacitor to ground and counting the number of switching cycles. The Soft Start pin is held low until 4096 cycles have been completed. Following this, the OCP signal resets and the converter recovers. After every soft start cycle, the converter stays in this mode until the overload or short circuit is removed.

For the iP1827, the Sync FET is turned OFF on the falling edge of a PWMSet or Clock signal that has duration of 25% of the switching period. For operation at the maximum duty cycle, the OCP circuit samples current for 40 ns, starting 40 ns after the low drive signal for the Sync FET > 70% of PVcc.

TABLE 2: OVERCURRENT SETTING VS. EXTERNAL ROCSET

I_{otrip} (A)	External Rocset (kohm)
15	2.61
16	2.94
17	3.24
18	3.65
19	4.02
20	4.53
21	4.99
22	5.62
23	6.34
24	7.15
25	8.06
26	9.09
27	10.5
28	12.1
29	14.3
30	16.9
31	20.5
32	26.1
33	34
34	48.7
35	80.6
36	226
37	Open

For operating duty cycles less than the maximum duty cycle of 75%, the OCP circuit still samples current for typically 40ns, but starts sampling 40 ns after the rising edge of PWMSet. Thus, for low duty cycle operation, the inductor current is sensed close to the valley. This allows a longer delay after the falling edge of the switch node, than the corresponding delay for an over-current sensing scheme which samples the current at the peak of the inductor current. This longer delay serves to filter out any noise on the switch node and hence on the OCSet pin, making this method more immune to false tripping.

THERMAL SHUTDOWN

Temperature sensing is provided inside iP1827. The trip threshold is typically set to 145°C. When the trip threshold is exceeded, thermal shutdown turns off both MOSFETs and discharges the soft start capacitor. Automatic restart is initiated when the sensed temperature drops within the operating range. There is a 20°C hysteresis in the thermal shutdown threshold.

TRIMMABLE RISING EDGE DEADBAND

The iP1827 has a rising edge deadband that is post-package trimmable. It is typically trimmed to 5ns-10ns which is an optimal range to minimize switching transition loss and at the same time, prevent cross conduction.

REMOTE VOLTAGE SENSING

True differential remote sensing in the feedback loop is critical to high current applications where the output voltage across the load may differ from the output voltage measured locally across an output capacitor at the output inductor, and to applications that require die voltage sensing.

The Vosp and Vosm pins of the iP1827 form the inputs to a remote sense differential amplifier with high speed, low input offset (post-package trimmed to +/-3mV) and low input bias current which ensure accurate voltage sensing and fast transient response in such applications.

It should be noted, however, that the output Voso of the difference amplifier also forms the input toa power good comparator and overvoltage comparator, both referenced to an upper threshold of 0.7V as discussed in the next section. Hence, in applications where Vo > 0.6V, it is necessary to use a resistive divider network after Vo to attenuate the sensed output voltage signal between the remote Vo and the remote ground to 0.6V, which is then applied between Vosp and Vosm.

In applications where only local sensing is required for feedback, the remote voltage sensing pins of the iP1827 may be dedicated to sensing the output for power good indication and overvoltage protection.

POWER GOOD OUTPUT AND OVER-VOLTAGE PROTECTION

The IC continually monitors the output voltage via output of the remote sense amplifier (Voso pin). The Voso voltage forms an input to a window comparator whose upper and lower thresholds are 0.7V and 0.51V respectively. Hence, the Power Good signal is flagged when the Voso pin voltage is within PGood window, i.e., between 0.51V and 0.69V, as shown in Figure 12a. The PGood pin is open drain and it needs to be externally pulled high. High state indicates that output is in regulation. Figure 12a also shows the PGood timing diagram with a 256 cycle delay between the Voso voltage entering within the thresholds defined by the PGood window and PGood going high

If the output voltage exceeds the over voltage threshold 0.7V, an over voltage trip signal is asserted; this will turn off the high side driver and turn on the low side driver until the Voso voltage drops below the 0.7V threshold. Both drivers are then turned off until a reset is performed by cycling Vcc (or PVcc/Enable) or until another OVP event occurs turning on the low side driver again.

Figure 12b shows the response in over-voltage condition.

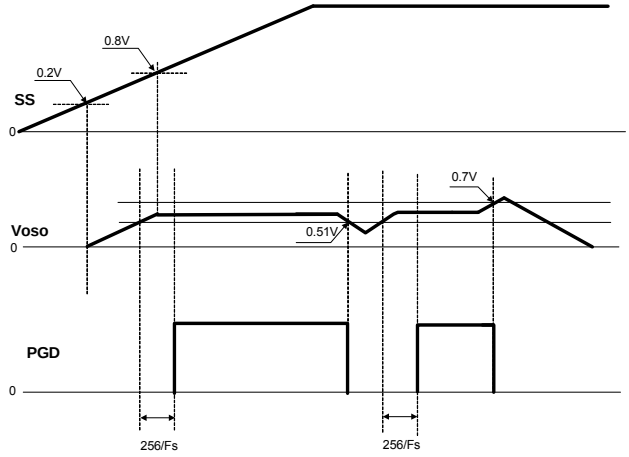


Figure 12a: iP1827 Power Good Signal Timing Diagram

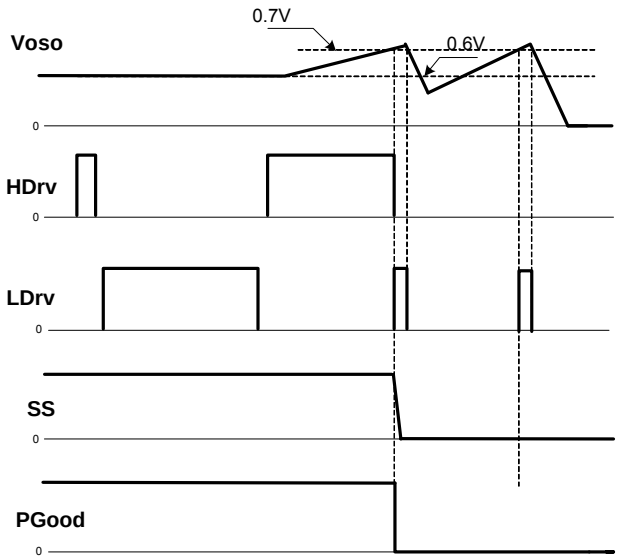


Figure 12b: iP1827 Signal Timing for OVP

BODY BRAKING™

The Body Braking feature of the iP1827 allows improved transient response to step-down load transients. A severe step-down load transient would cause an overshoot in the output voltage and drive the Comp pin voltage down until control saturation occurs demanding 0% duty cycle, and the PWM input to the Control FET driver is kept OFF. When the first such skipped pulse occurs, the iP1827 enters the Body Braking mode, wherein the Sync FET is also turned OFF. The inductor current then decays by freewheeling through the body diode of the Sync FET. Thus, with Body Braking, the forward voltage drop of the body diode provides an additional voltage to discharge the inductor current faster to the light load value as shown in equations 4 and 5 below:

$$\frac{di_L}{dt} = -\frac{V_o + V_D}{L}, \text{ with body braking} \qquad (4)$$

$$\frac{di_L}{dt} = -\frac{V_o}{L}, \text{without body braking} \qquad (5)$$

where V_D= forward voltage drop of the body diode of the Sync FET.

The Body Braking mechanism is kept OFF during pre-bias operation. Also, in the event of an extremely severe load step-down transient causing an OVP, the Body Brake is overridden by the OVP latch, which turns on the Sync FET.

MINIMUM ON TIME CONSIDERATIONS

The minimum ON time is the shortest amount of time for which the Control FET may be reliably turned on, and this depends on the internal timing delays. For the iP1827, the minimum on-time is specified as 50 ns maximum. Any design or application using the iP1827 must require a pulse width that is at least equal to this minimum on-time and preferably higher than 100 ns. This is necessary for the circuit to operate without jitter and pulse-skipping, which can cause high inductor current ripple and high output voltage ripple.

MAXIMUM DUTY RATIO CONSIDERATIONS

For the iP1827, the upper limit on the operating duty ratio is set by the duration of the PWMSet pulse or by the 200 ns fixed off-time, whichever is higher. Since the PWMSet pulse has a 25% duty cycle, this limits the maximum duty ratio at which the iP1827 can operate, to 75%. At switching frequencies above 1.25 MHz, however, the maximum duty ratio is set by the 200 ns fixed off-time. Thus, at switching frequencies above 1.25 MHz, higher the switching frequency, the lower is the maximum duty ratio at which the iP1827 can operate. Figure 13 shows a plot of the maximum duty ratio v/s the switching frequency, with 200 ns off-time.

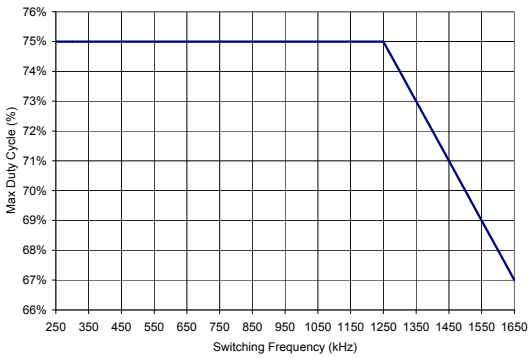


Figure 13: Maximum duty cycle v/s switching frequency.

TRAILING EDGE PULSE WIDTH MODULATION WITH RAMP-SLOPE MODULATION

The iP1827 employs trailing edge Pulse width modulation. However, unlike conventional trailing edge modulators, which compare the PWM ramp with the output of the error amplifier or the Comp voltage, in the modulation scheme used in the iP1827, the slope of the PWM ramp is modulated by the Comp voltage and this modulated ramp is then compared to a fixed reference voltage. The advantage of this scheme is that comparison always takes place at a fixed reference irrespective of the duty cycle of operation. Conventional modulators suffer from increased noise susceptibility at the lower duty cycles, since the comparison takes place at the Comp voltage level which is close to the bottom of the PWM ramp for low duty cycle operation.

Figure 14 shows theoretical waveforms for the PWM ramp and the PWM output in response to a changing Comp voltage. Figure 15 shows the variation of the modulator gain (F_m) with the duty cycle (D).

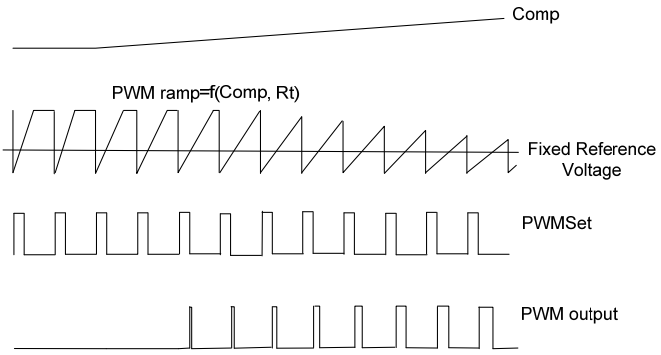


Figure 14: Theoretical waveforms for the new PWM scheme

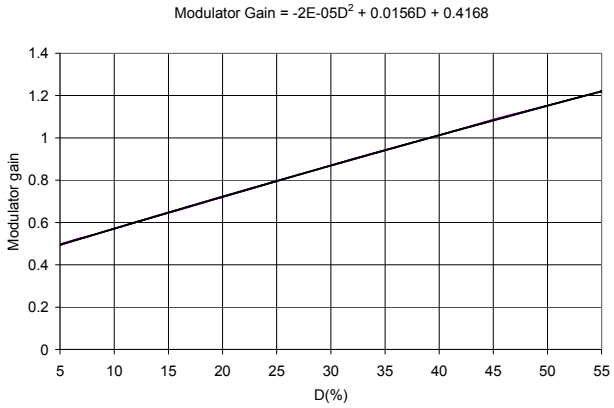


Figure 15: Modulator gain (F_m) v/s Duty Ratio (D%)

DESIGN PROCEDURE

APPLICATION INFORMATION

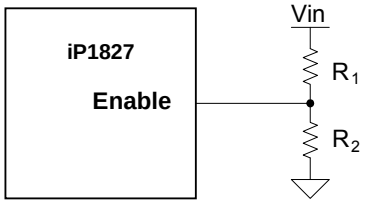
Design Example

The following example is a typical application for iP1827. The application circuit is shown on page 1.

V_{in} = 12V (13.2V max)
V_o = 1.8V
I_o = 25A
ΔV_o (transient) ≤ ±90mV for ΔIo = 10.5A @ 2.5A/µs
ΔV_o (ripple) ≤ ±13.5mV (±0.75%)
F_s = 600kHz

ENABLING THE IP1827

As explained earlier, the precise threshold of the Enable lends itself well to implementation of a UVLO for the Bus Voltage.



For a typical Enable threshold of V_{EN} = 1.2 V

$$V_{in(\min)} * \frac{R_2}{R_1 + R_2} = V_{EN} = 1.2 \qquad (6)$$

$$R_2 = R_1 \frac{V_{EN}}{V_{in(\min)} - V_{EN}} \qquad (7)$$

For a $V_{in\ (min)}$ = 10.2V, R_1 = 49.9K and R_2 = 7.5K is a good choice.

PROGRAMMING THE FREQUENCY

For F_s = 600 kHz, select R_t = 36.5 kΩ, using Table 1.

OUTPUT VOLTAGE PROGRAMMING

Output voltage is programmed by the reference voltage and external voltage divider. If the remote sense feature is used, the divider is connected to the Vosp and Vosm pins. If only local sensing is used for feedback, with the remote sense amplifier used only in the over-voltage protection, circuit, the resistive divider should be connected to the Fb pin.

For this design, with high output current requirements, we choose to use the true differential remote sense feature. The Fb pin is the inverting input of the error amplifier, which is internally referenced to 0.6V. This references the output of the remote sense amplifier to 0.6V also. In order to satisfy this condition, the voltage between the Vosp and Vosm pins of the error amplifier should be 0.6V when the output is at its desired value. The output voltage is defined by using the following equation:

$$V_o = V_{ref} * \left(1 + \frac{R_{top}}{R_{bot}}\right) \qquad (8)$$

when an external resistor divider is connected to the output as shown in Figure 16.

Equation (8) can be rewritten as:

$$R_{top} = R_{bot} * \left(\frac{V_o - V_{ref}}{V_{ref}}\right) \qquad (9)$$

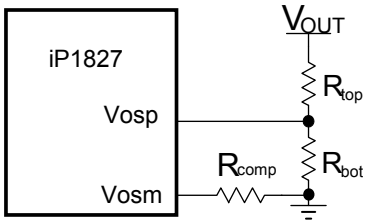


Figure 16: Typical application of the iP1827 for programming the output voltage

For our design, R_{bot} is selected to be 604 ohm.

This selection is based on a trade-off between two considerations:

1) The resistive divider should be as low impedance as possible in order to have minimal impact on the impedance seen at the Vosp and Vosm pins.
2) The resistive divider should have high enough impedance so as to minimize the bleed current from the output.

Hence, from Equation (9), R_{top} = 1.21K.

In order to ensure that the Vosp and Vosm see balanced impedances, it is advisable to use R_{comp} such that:

$$R_{comp} = R_{top} \parallel R_{bot} = 402\ \Omega \qquad (10)$$

SOFT-START PROGRAMMING

The soft-start timing can be programmed by selecting the soft-start capacitance value. From (1), for a desired start-up time of the converter, the soft start capacitor can be calculated by using:

$$C_{SS}(\mu\text{F}) = T_{start}\ (\text{ms}) \times 0.033 \qquad (11)$$

Where T_{start} is the desired start-up time (ms).

For a start-up time of 3ms, the soft-start capacitor will be 0.099µF. Choose a 0.1µF ceramic capacitor.

INPUT CAPACITOR SELECTION

The ripple current generated during the on time of the upper MOSFET should be provided by the input capacitor. The RMS value of this ripple is expressed by:

$$I_{RMS} = I_o * \sqrt{D*(1-D)} \qquad (12)$$

$$D = \frac{V_o}{V_{in}} \qquad (13)$$

Where:

D is the Duty Cycle
I_{RMS} is the RMS value of the input capacitor current.
Io is the output current.
For I_o=25A and D = 0.15, the I_{RMS} = 8.93A.

Ceramic capacitors are recommended due to their peak current capabilities. They also feature low ESR and ESL at higher frequency which enables better efficiency. For this application, it is advisable to have 5x22uF 16V ceramic capacitors ECJ-3YX1C106K from Panasonic. In addition to these, although not mandatory, a 1X330uF, 25V SMD capacitor EEV-FK1E331P may also be used as a bulk capacitor and is recommended if the input power supply is not located close to the converter.

INDUCTOR SELECTION

The inductor is selected based on output power, operating frequency and efficiency requirements. A low inductor value causes large ripple current, resulting in the smaller size, and a faster response to a load transient but poor efficiency and high output noise. Generally, the selection of the inductor value can be reduced to the desired maximum ripple current in the inductor. The optimum point is usually found between 20% and 50% ripple of the output current.

For the buck converter, the inductor value for the desired operating ripple current can be determined using the following relation:

$$V_{in} - V_o = L * \frac{\Delta i}{\Delta t};\quad \Delta t = D * \frac{1}{F_s}$$
$$L = (V_{in} - V_o) * \frac{V_o}{V_{in} * \Delta i * F_s} \qquad (14)$$

Where:

V_{in} = Maximum input voltage
V_0 = Output Voltage
Δi = Inductor Ripple Current
F_s = Switching Frequency
Δ_t – Turn on time
D – Duty Cycle

If $\Delta i \approx 35\%(I_o)$, then the output inductor is calculated to be 0.29µH. Select L = 0.3µH.

The 59PR9874N from Vitec provides a compact inductor suitable for this application.

OUTPUT CAPACITOR SELECTION

The voltage ripple and transient requirements determine the output capacitors type and values. The criteria are normally based on the value of the Effective Series Resistance (ESR). However the actual capacitance value and the Equivalent Series Inductance (ESL) are other contributing components. These components can be described as:

$$\Delta V_o = \Delta V_{o(ESR)} + \Delta V_{o(ESL)} + \Delta V_{o(C)}$$

$$\Delta V_{o(ESR)} = \Delta I_L * ESR$$

$$\Delta V_{o(ESL)} = \left(\frac{V_{in} - V_o}{L}\right) * ESL \qquad (15)$$

$$\Delta V_{o(C)} = \frac{\Delta I_L}{8 * C_o * F_s}$$

ΔV_0 = Output Voltage Ripple

ΔI_L = Inductor Ripple Current

Since the output capacitor has a major role in the overall performance of the converter and determines the result of transient response, selection of the capacitor is critical. The iP1827 can perform well with all types of capacitors.

As a rule, the capacitor must have low enough ESR to meet output ripple and load transient requirements.

The goal for this design is to meet the voltage ripple requirement in the smallest possible capacitor size. Therefore it is advisable to select ceramic capacitors due to their low ESR and ESL and small size. Fifteen of the Panasonic ECJ-2FB0J226ML (22uF, 6.3V, 3mOhm) capacitors are a good choice.

FEEDBACK COMPENSATION

The iP1827 is a voltage mode controller. The control loop is a single voltage feedback path including error amplifier and error comparator. To achieve fast transient response and accurate output regulation, a compensation circuit is necessary. The goal of the compensation network is to provide an open-loop transfer function with the highest 0 dB crossing frequency and adequate phase margin (greater than 45°).

The output LC filter introduces a double pole, -40dB/decade gain slope above its corner resonant frequency, and a total phase lag of 180° (see Figure 16). The resonant frequency of the LC filter is expressed as follows:

$$F_{LC} = \frac{1}{2 * \pi \sqrt{L_o * C_o}} \qquad (16)$$

Figure 17 shows gain and phase of the LC filter. Since we already have 180° phase shift from the output filter alone, the system runs the risk of being unstable.

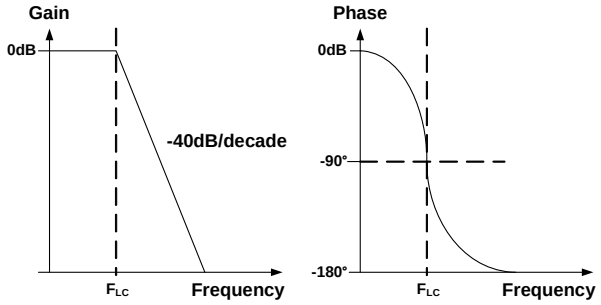


Figure 17: Gain and Phase of LC filter

The iP1827 uses a voltage-type error amplifier with high-gain (110dB) and wide-bandwidth. The output of the amplifier is available for DC gain control and AC phase compensation.

The error amplifier can be compensated either in type II or type III compensation.

Local feedback with Type II compensation is shown in Figure 18.

This method requires that the output capacitor should have enough ESR to satisfy stability requirements. In general the output capacitor's ESR generates a zero typically at 5kHz to 50kHz which is essential for an acceptable phase margin.

The ESR zero of the output capacitor is expressed as follows:

$$F_{ESR} = \frac{1}{2 * \pi * ESR * C_o} \qquad (17)$$

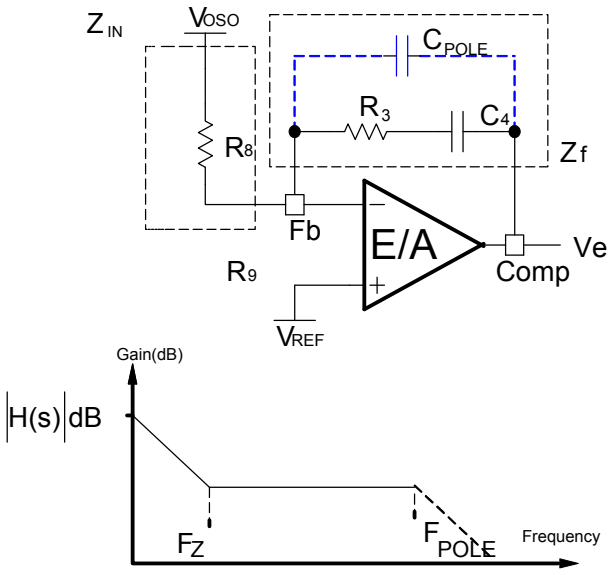


Figure 18: Type II compensation network and its asymptotic gain plot

The transfer function (V_e/V_{oso}) is given by:

$$\frac{V_e}{V_{oso}} = H(s) = -\frac{Z_f}{Z_{IN}} = -\frac{1+sR_3C_4}{sR_8C_4} \qquad (18)$$

The (s) indicates that the transfer function varies as a function of frequency. This configuration introduces a gain and zero, expressed by:

$$|H(s)| = \frac{R_3}{R_8} \qquad (19)$$

$$F_z = \frac{1}{2\pi * R_3 * C_4} \qquad (20)$$

First select the desired zero-crossover frequency (F_o):

$$F_o > F_{ESR} \text{ and } F_o \le (1/5 \sim 1/10) * F_s$$

Use the following equation to calculate R_3:

$$R_3 = \frac{F_o * F_{ESR} * R_8}{V_{in} * F_m * \beta * F_{LC}^2} \qquad (21)$$

Where:

V_{in} = Maximum Input Voltage
F_o = Crossover Frequency
F_{ESR} = Zero Frequency of the Output Capacitor
F_{LC} = Resonant Frequency of the Output Filter
R_8 = Feedback Resistor
$\beta = V_{ref}/V_o$
F_m=Modulator gain

To cancel one of the LC filter poles, place the zero before the LC filter resonant frequency pole:

$$F_z = 75\% \ F_{LC}$$

$$F_z = 0.75 * \frac{1}{2\pi\sqrt{L_o * C_o}} \qquad (22)$$

Use equations (20), (21) and (22) to calculate C_4.

One more capacitor is sometimes added in parallel with C_4 and R_3. This introduces one more pole which is mainly used to suppress the switching noise.

The additional pole is given by:

$$F_P = \frac{1}{2\pi * R_3 * \frac{C_4 * C_{POLE}}{C_4 + C_{POLE}}} \qquad (23)$$

The pole sets to one half of the switching frequency which results in the capacitor C_{POLE}:

$$C_{POLE} = \frac{1}{\pi * R_3 * F_s - \frac{1}{C_4}} \cong \frac{1}{\pi * R_3 * F_s} \qquad (24)$$

For a general solution for unconditional stability for any type of output capacitors, and a wide range of ESR values, we should implement local feedback with a type III compensation network. The typically used compensation network for voltage-mode controller is shown in Figure 19.

Again, the transfer function is given by:

$$\frac{V_e}{V_{oso}} = H(s) = -\frac{Z_f}{Z_{IN}}$$

By replacing Z_{in} and Z_f according to Figure 19, the transfer function can be expressed as:

$$H(s) = -\frac{(1+sR_3C_4)[1+sC_7(R_8+R_{10})]}{sR_8(C_4+C_3)\left[1+sR_3\left(\frac{C_4*C_3}{C_4+C_3}\right)\right](1+sR_{10}C_7)} \quad \ldots.(25)$$

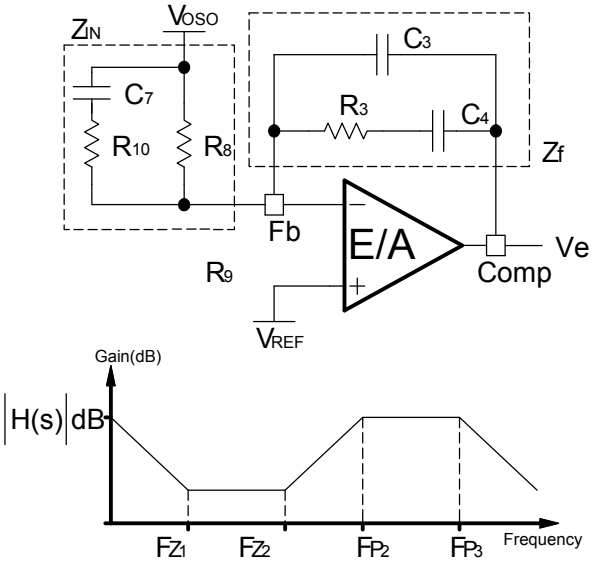


Figure 19: Type III Compensation network and its asymptotic gain plot

The compensation network has three poles and two zeros and they are expressed as follows:

$$F_{P1} = 0 \quad (26)$$

$$F_{P2} = \frac{1}{2\pi * R_{10} * C_7} \quad (27)$$

$$F_{P3} = \frac{1}{2\pi * R_3\left(\frac{C_4 * C_3}{C_4 + C_3}\right)} \cong \frac{1}{2\pi * R_3 * C_3} \quad (28)$$

$$F_{Z1} = \frac{1}{2\pi * R_3 * C_4} \quad (29)$$

$$F_{Z2} = \frac{1}{2\pi * C_7 * (R_8 + R_{10})} \cong \frac{1}{2\pi * C_7 * R_8} \quad (30)$$

Cross over frequency is expressed as:

$$F_o = R_3 * C_7 * V_{in} * \beta * F_m * \frac{1}{2\pi * L_o * C_o} \quad (31)$$

Based on the frequency of the zero generated by the output capacitor and its ESR, relative to crossover frequency, the compensation type can be different. The table below shows the compensation types for relative locations of the crossover frequency.

Compensator Type	F_{ESR} v/s F_0	Output Capacitor
Type II	$F_{LC} < F_{ESR} < F_0 < F_S/2$	Electrolytic Tantalum
Type III	$F_{LC} < F_0 < F_{ESR}$	Tantalum Ceramic

The higher the crossover frequency, the potentially faster the load transient response will be. However, the crossover frequency should be low enough to allow attenuation of switching noise. Typically, the control loop bandwidth or crossover frequency is selected such that:

$$F_o \le (1/5 \sim 1/10) * F_s$$

The DC gain should be large enough to provide high DC-regulation accuracy. The phase margin should be greater than 45° for overall stability.

For this design we have:

V_{in} = 12V
V_o = 1.8V
β = V_{ref}/V_o=0.333
Modulator gain = F_m = 0.65, from Figure 15
V_{ref} = 0.6V
L_o = 0.3uH
C_o = 10x22uF, ESR = 3mOhm each

It must be noted here that the value of the capacitance used in the compensator design must be the small signal value. For instance, the small signal capacitance of the 22uF capacitor used in this design is 12uF at 1.8V DC bias and 600kHz frequency. It is this value that must be used for all computations related to the compensation. The small signal value may be obtained from the manufacturer's datasheets, design tools or SPICE models. Alternatively, they may also be inferred from measuring the power stage transfer function of the converter and measuring the double pole frequency F_{LC} and using equation (16) to compute the small signal C_o.

These result in:

***F_{LC}*=26.53kHz**
***F_{ESR}*=4.4MHz**
***$F_s/2$*=300kHz**

Select crossover frequency ***F_o*=110 kHz**

Since $F_{LC}<F_o<F_s/2<F_{ESR}$, Type III is selected to place the pole and zeros.

Detailed calculation of compensation Type III:

Desired Phase Margin Θ = 80°

$$F_{Z2} = F_o\sqrt{\frac{1-\sin\ \Theta}{1+\sin\ \Theta}} = 9.62\ \ \text{kHz}$$

$$F_{P2} = F_o\sqrt{\frac{1+\sin\ \Theta}{1-\sin\ \Theta}} = 1257.31\ \ \text{kHz}$$

$$F_{Z1} = 0.5 * F_{Z2} = 4.81\ \ \text{kHz}$$

$$F_{P3} = 0.5 * F_s = 300\ \ \text{kHz}$$

Select: C_7 = 2.2nF

Calculate: R_3, C_3 and C_4:

$$R_3 = \frac{2\pi * F_o * L_o * C_o}{C_7 * V_{in} * F_m * \beta};\ R_3 = 4.42\ \ \text{kΩ}$$

Select: R_3 = 4.22 kΩ

$$C_4 = \frac{1}{2\pi * F_{Z1} * R_3};\ C_4 = 7.84\ \text{nF},\ \ \text{Select}:\ C_4 = 8.2\ \text{nF}$$

$$C_3 = \frac{1}{2\pi * F_{P3} * R_3};\ C_3 = 125.71\ \text{pF},\ \ \text{Select}:\ C_3 = 120\ \text{pF}$$

Calculate: R_{10}, R_8 and R_9:

$$R_{10} = \frac{1}{2\pi * C_7 * F_{P2}};\ \ R_{10} = 60\ \Omega,\ \ \text{Select}:\ R_{10} = 57.6\ \Omega$$

$$R_8 = \frac{1}{2\pi * C_7 * F_{Z2}} - R_{10};\ R_8 = 7.46\ \text{kΩ},$$

Select: R_8 = 7.5 kΩ

PROGRAMMING THE CURRENT-LIMIT

The Current-Limit threshold can be set by connecting a resistor (R_{OCSet}) from the SW pin to the OCSet pin. The resistor can be selected by using Table 2.

In order to set a trip current of 31A, we may select R_{OCSet} = 20.5K, using Table 2.

SETTING THE POWER GOOD THRESHOLD

A window comparator internally sets a lower Power Good threshold at 0.51V and an upper Power Good threshold at 0.7V. When the voltage at the Voso pin is within the window set by these thresholds, PGood is asserted.

The power good output PGD is an open drain output. Hence, it is necessary to use a pull up resistor R_{PG} from PGD pin to Vcc. The value of the pull-up resistor must be chosen such as to limit the current flowing into the PGD pin, when the output voltage is not in regulation, to less than 5mA. A typical value used is 10kΩ.

It must be noted that if the voltage on Voso exceeds the upper threshold 0.7V, not only is PGD de-asserted, but also an overvoltage fault is flagged, following which, even if the overvoltage condition gets resolved, the converter can be re-started only by cycling Vcc or Enable.

TYPICAL OPERATING WAVEFORMS

Vin=12.0V, Vcc=3.3V, Vo=1.8V, Io=0A - 25A, Room Temperature, no airflow

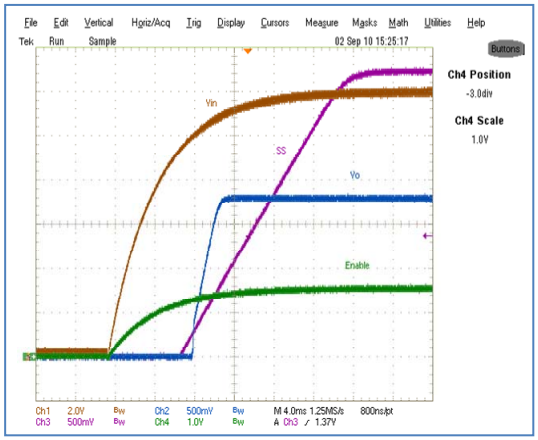


Figure 20: Start up at 25A Load
Ch_1:V_{in}, Ch_2:V_o, Ch_3:V_{ss}, Ch_4:Enable

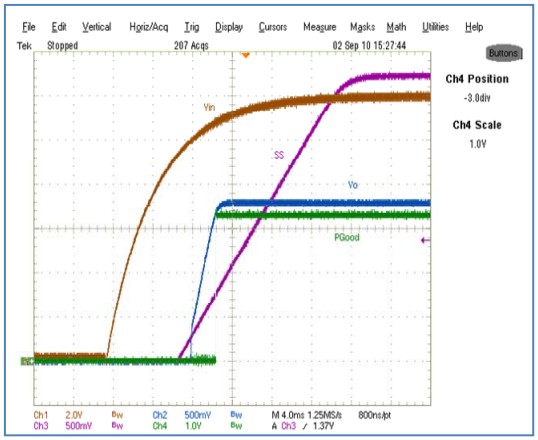


Figure 21: Start up at 25A Load,
Ch_1:V_{in}, Ch_2:V_o, Ch_3:V_{ss}, Ch_4:V_{PGood}

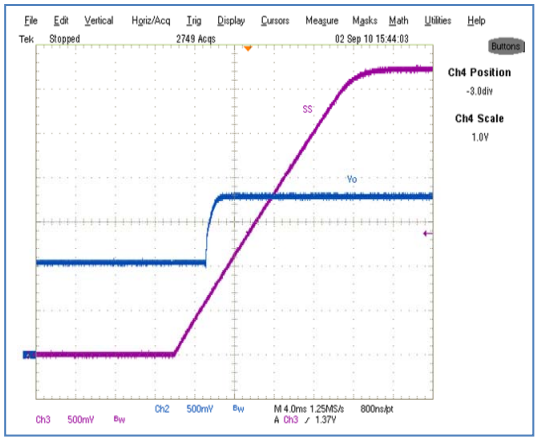


Figure 22 : Start up with 1V Pre Bias , 0A Load, Ch_2:V_o, Ch_3:V_{SS}

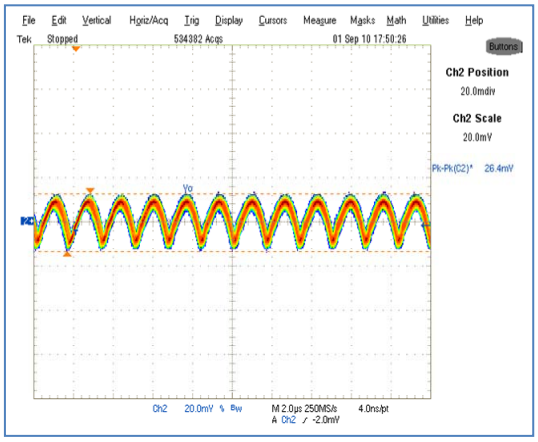


Figure 23: Output Voltage Ripple, 25A load Ch_2: V_{out}

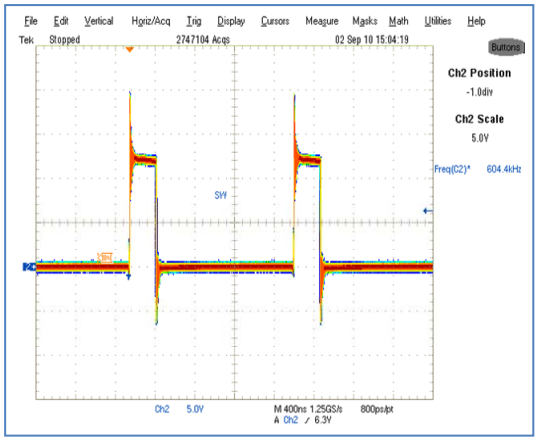


Figure 24 : Inductor node at 25A load
Ch_2:LX

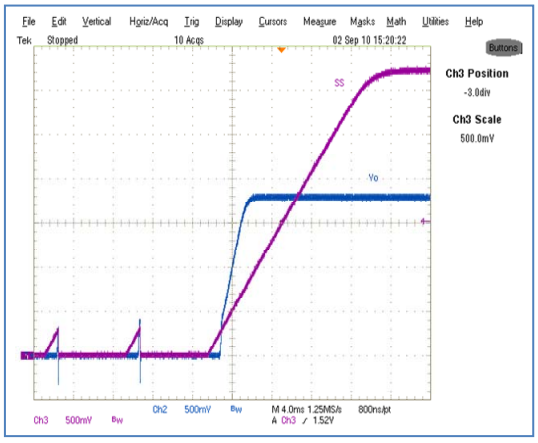
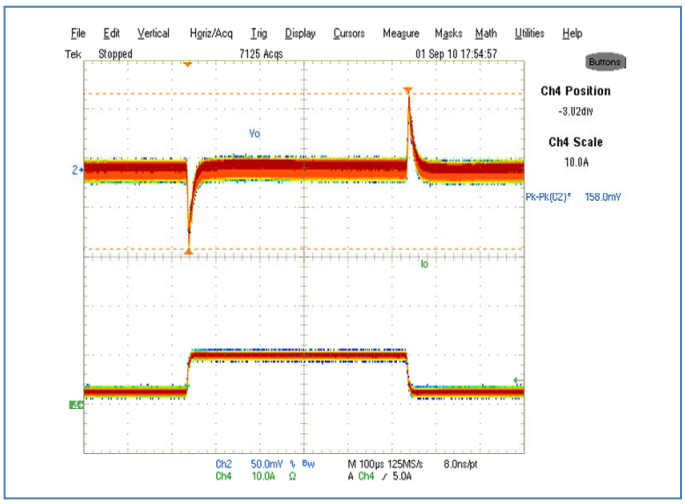
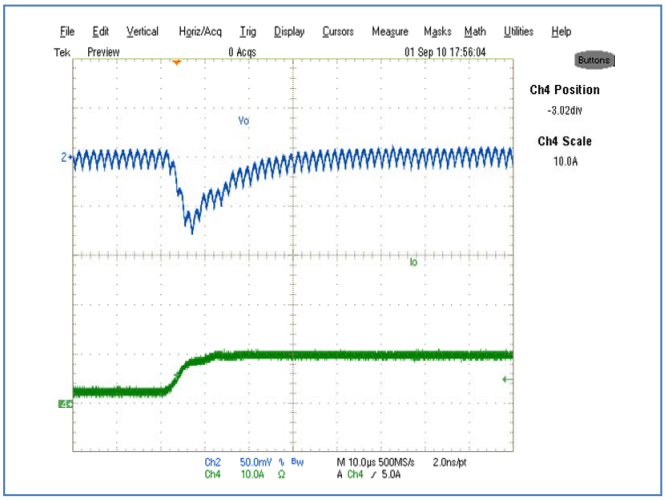


Figure 25: Short (Hiccup) Recovery
Ch_2:V_{out} , Ch_3:V_{ss}

TYPICAL OPERATING WAVEFORMS

Vin=12.0V, Vcc=3.3V, Vo=1.8V, Io=3.5A - 14A, Room Temperature, no airflow





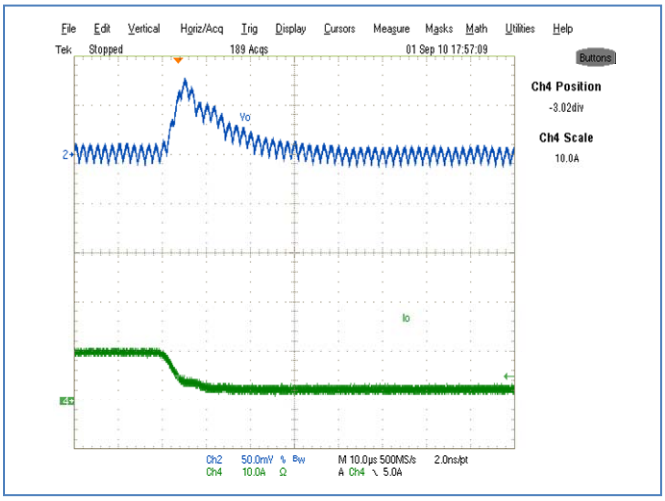
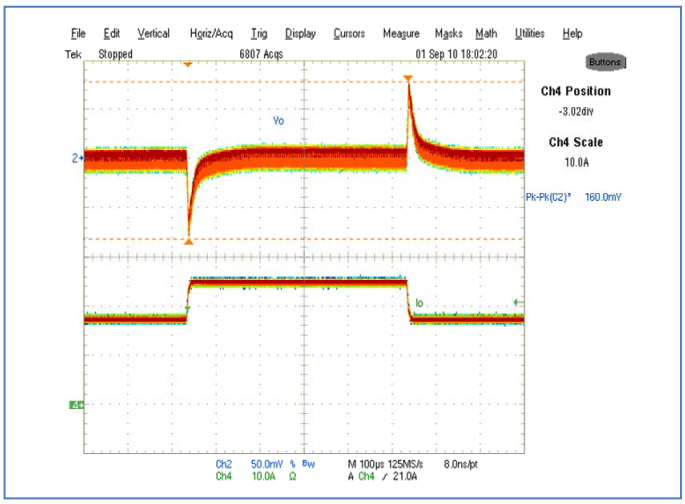
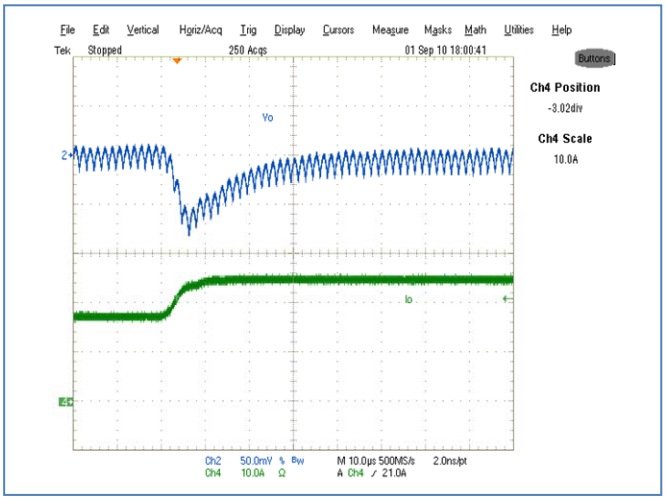


Figure 26: Transient Response, 3.5A to 14A step (2.5A/us)
Ch_2:V_{out}

TYPICAL OPERATING WAVEFORMS

Vin=12.0V, Vcc=3.3V, Vo=1.8V, Io=3.5A - 14A, Room Temperature, no airflow





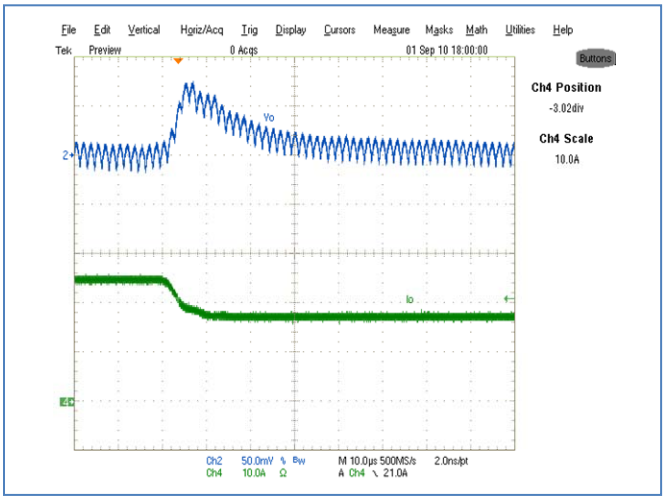


Figure 27: Transient Response, 24.5A to 25A step (2.5A/us)
Ch_2:V_{out}

TYPICAL OPERATING WAVEFORMS

Vin=12.0V, Vcc=3.3V, Vo=1.8V, Io=0A - 25A, Room Temperature

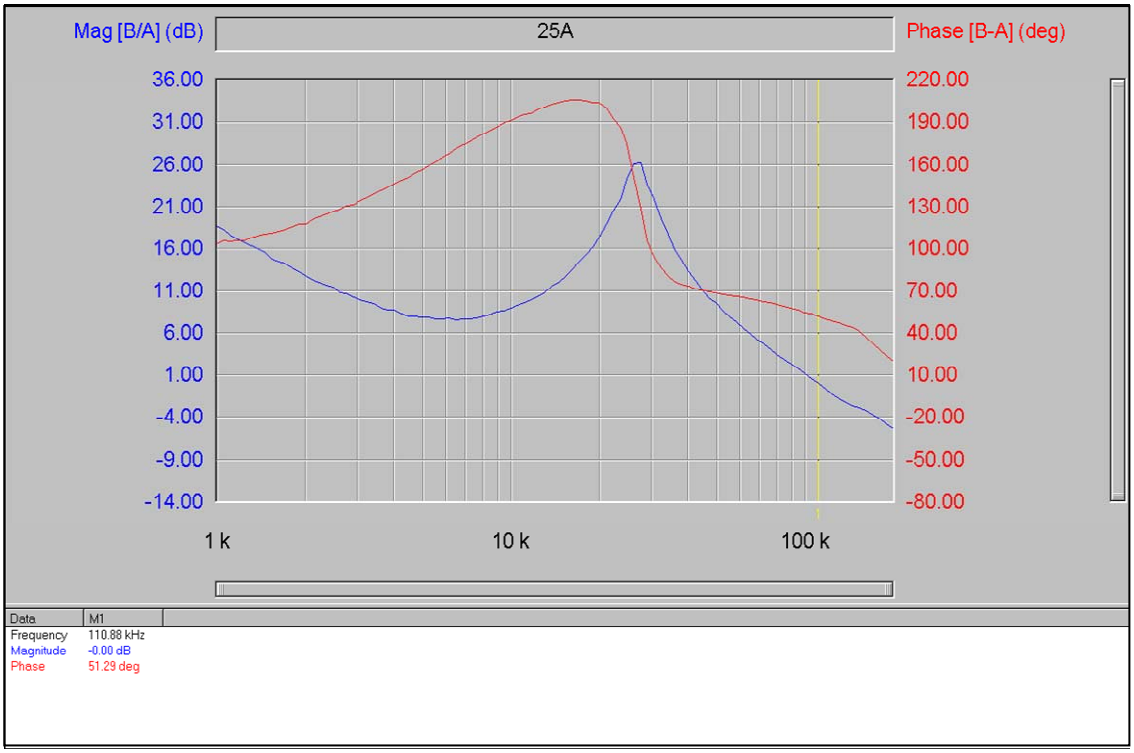


Figure 28: Bode Plot at 25A load shows a bandwidth of 110.88kHz and phase margin of 51.29 degrees

TYPICAL OPERATING WAVEFORMS

Vin=12.0V, Vcc=3.3V, Vo=1.8V, Io=0A - 25A, Room Temperature, No airflow

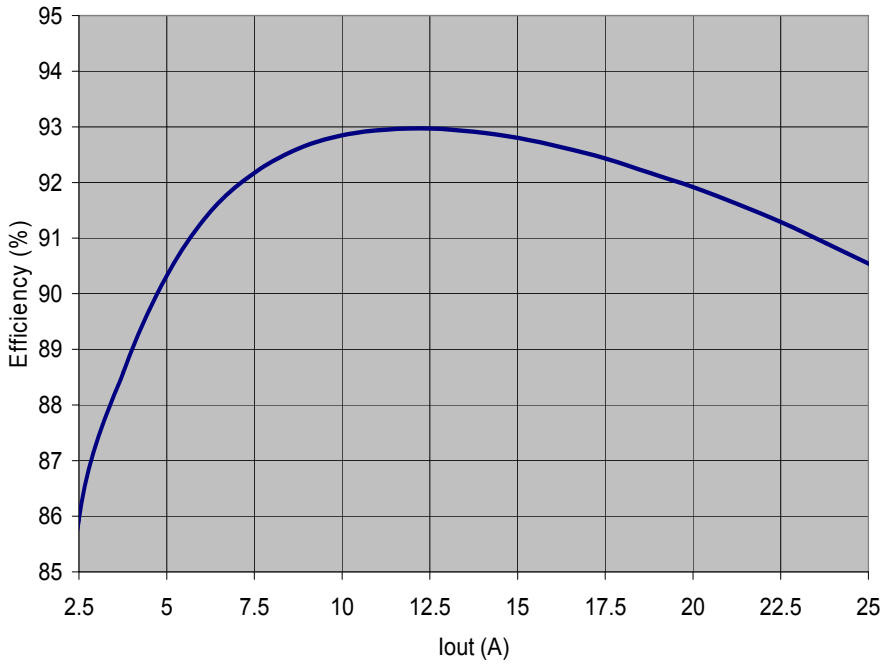


Figure 29: Efficiency versus load current

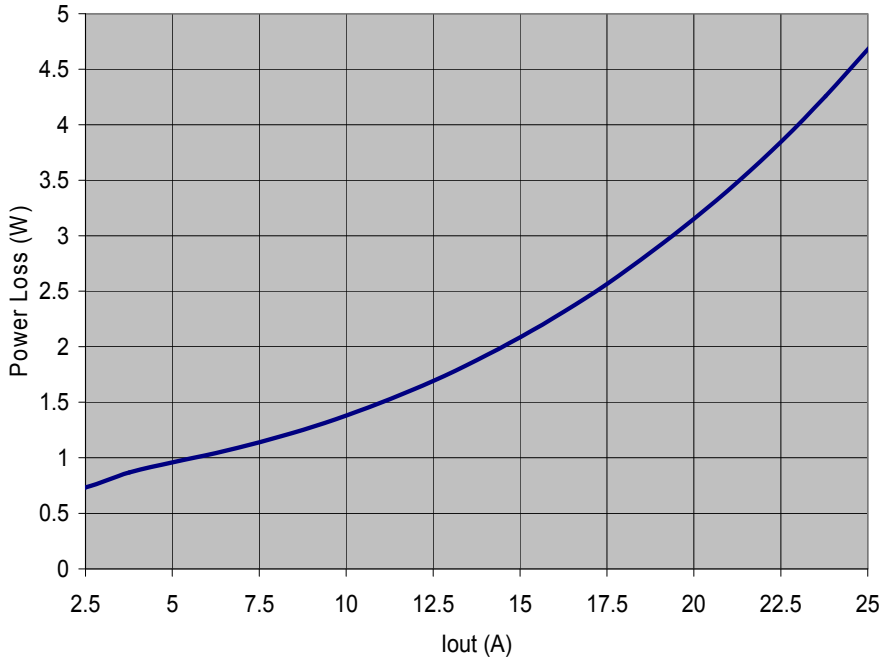


Figure 30: Power loss versus load current

THERMAL IMAGES

Vin=12.0V, Vcc=3.3V, Vo=1.8V, Io=0A-25A, Room Temperature, 200 LFM

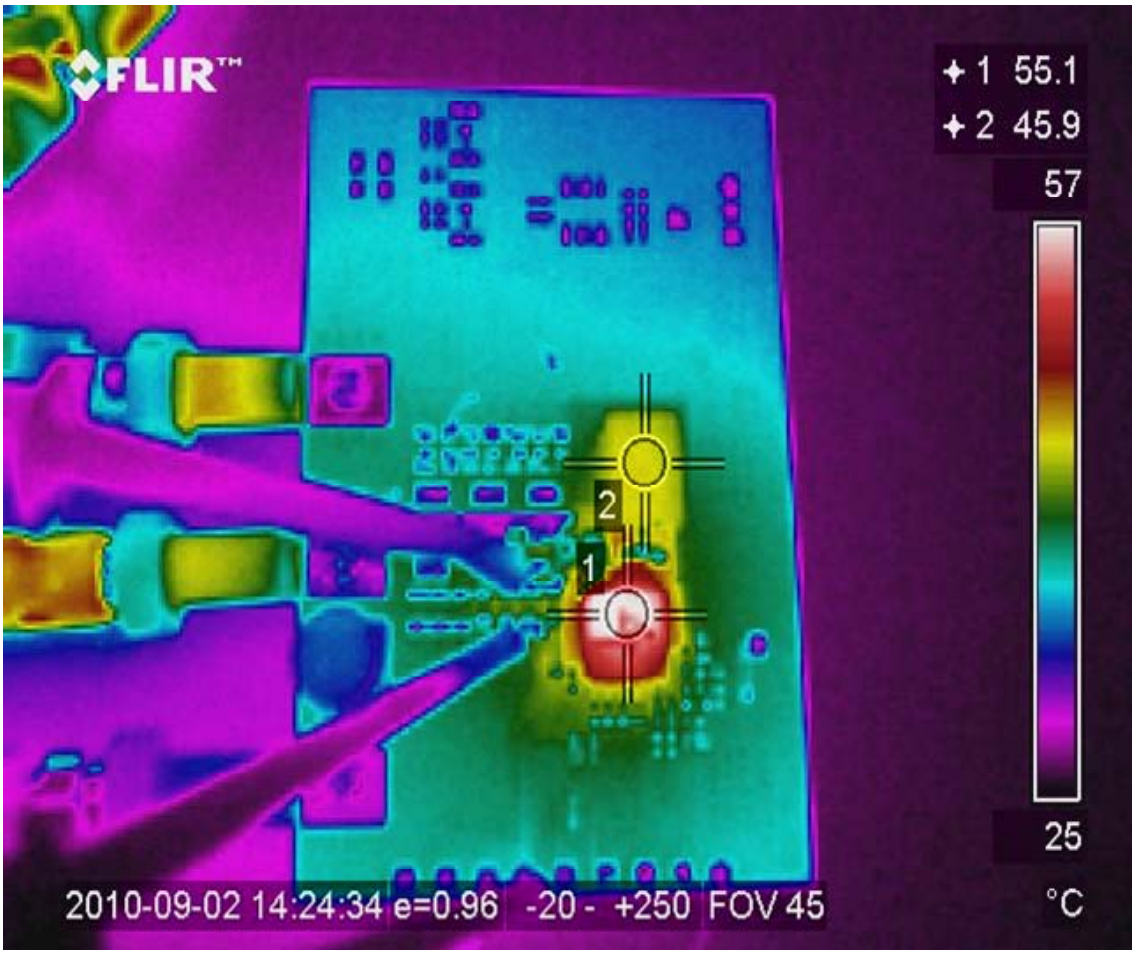


Figure 31: Thermal Image of the board at 25A load
Test point 1 is iP1827
Test point 2 is inductor

OTHER APPLICATION CIRCUITS

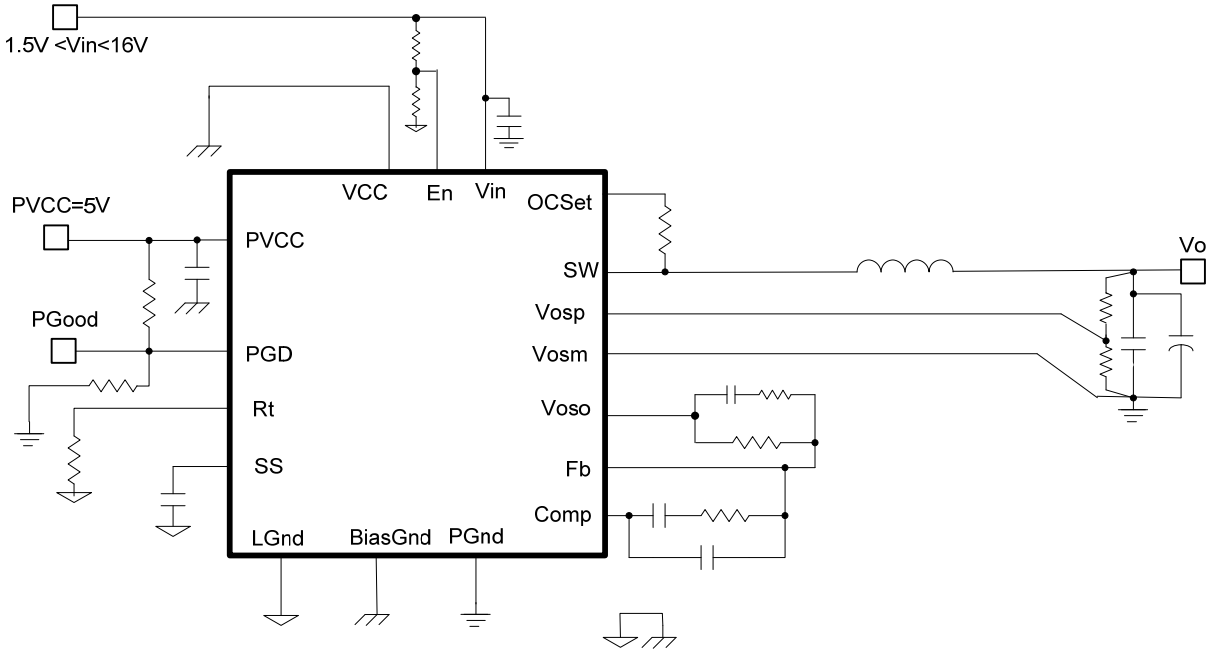


Figure 32: Application with external PVCC=5V

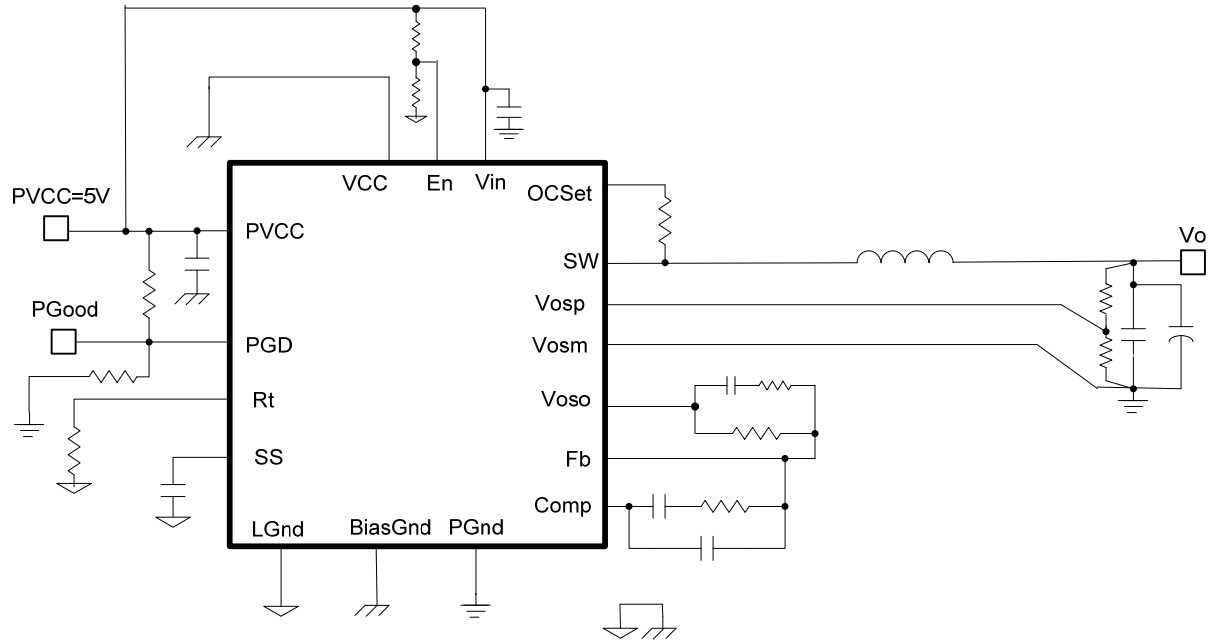


Figure 33: Single 5V application

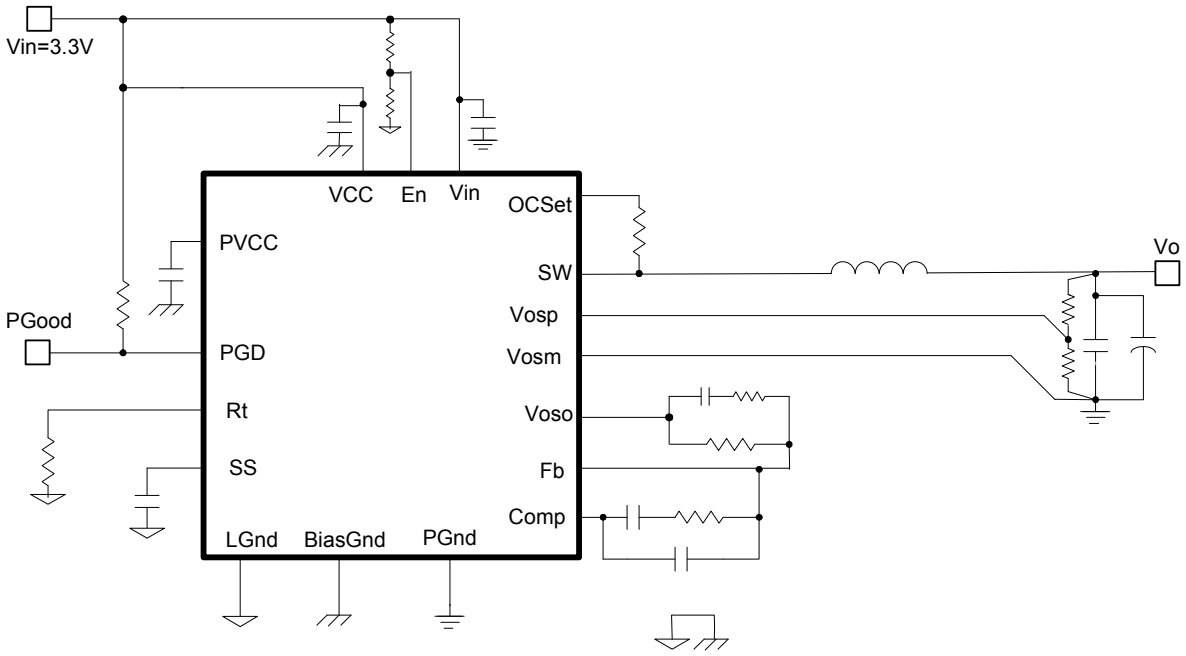


Figure 34: Single 3.3V Application

LAYOUT CONSIDERATIONS

The layout is very important when designing high frequency switching converters. Layout will affect noise pickup and can cause a good design to perform with less than expected results.

Make all the connections for the power components in the top layer with wide, copper filled areas or polygons. In general, it is desirable to make proper use of power planes and polygons for power distribution and heat dissipation.

The inductor, output capacitors and the iP1827 should be as close to each other as possible. This helps to reduce the EMI radiated by the power traces due to the high switching currents through them.

The input capacitors should be placed as close as possible to the PGnd pad. The connection of the Vin pad to the Vin power polygon should be low impedance, using several vias in parallel. The layout must ensure minimum length ground path and enough copper for input and output capacitors with a direct connection.

The iP1827 has a local power ground pad called Bias Gnd (pin 12) for bypassing Vcc or PVcc supplies. The analog or signal ground, LGnd, is used as a separate control circuit ground to which all signals are referenced. The analog ground polygon should be connected to BiasGnd through a single point connection using a 0 ohm resistor, at a location away from noise sources. The PGnd pad (Pin 3) should be connected to system power Ground.

In order to minimize coupling switching noise into other layers, the area of the switch node copper should be kept small. It is also advisable to keep the switch node copper localized to the top layer.

The critical bypass components such as capacitors for Vcc should be close to their respective pins. It is important to place the feedback components including feedback resistors and compensation components close to Fb and Comp pins.

A pair of sense traces running very close to each other and away from any noise sources should be used to implement true differential remote sensing of the voltage.

If remote sense is not used, the output voltage sense trace used for feedback should be tapped from a low impedance point such as directly from an output capacitor.

The iPOWiR package is a thermally enhanced package. Based on thermal performance it is recommended to use at least a 6-layers PCB. Figures 25A-f illustrate the implementation of the layout guidelines outlined above, on the IRDC1827 6 layer demoboard.

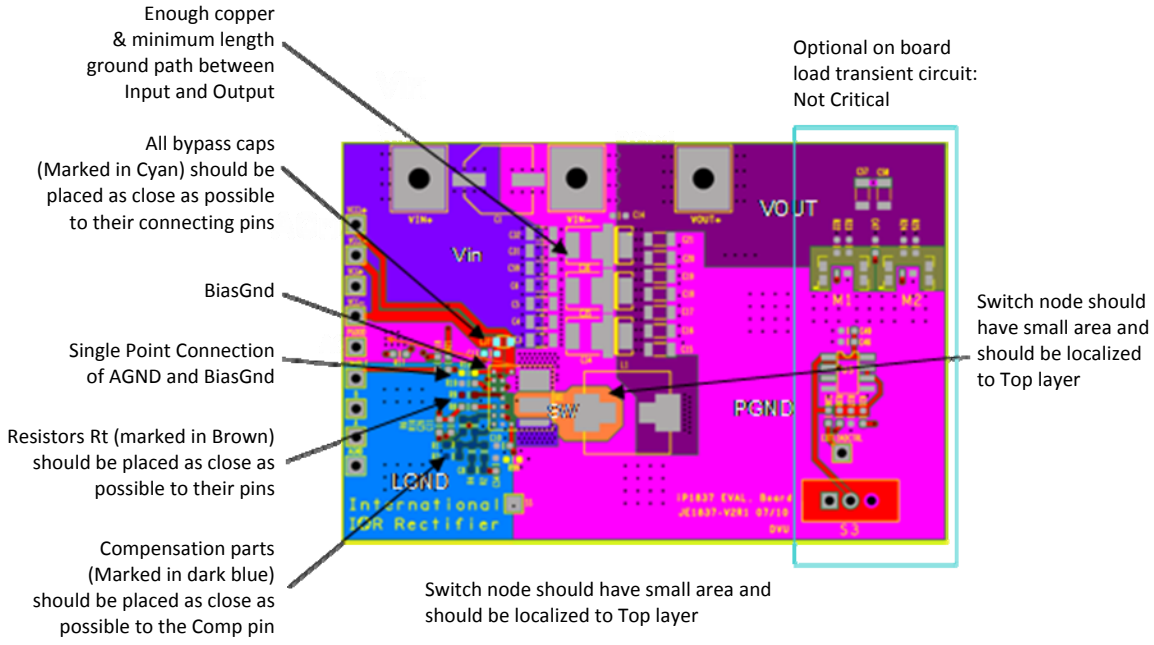


Figure 35a: IRDC1827 demoboard layout considerations – Top Layer

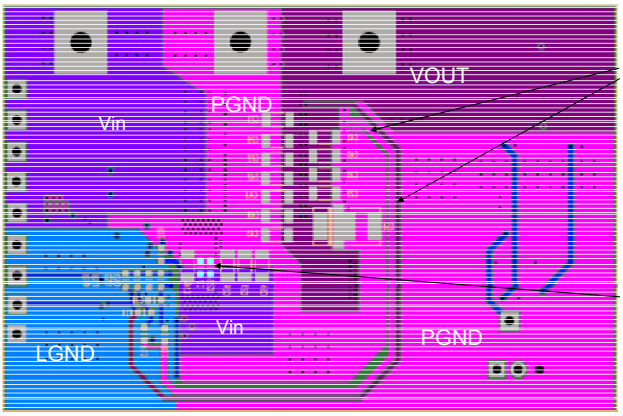


Figure 35b: IRDC1827 demoboard layout considerations – Bottom Layer

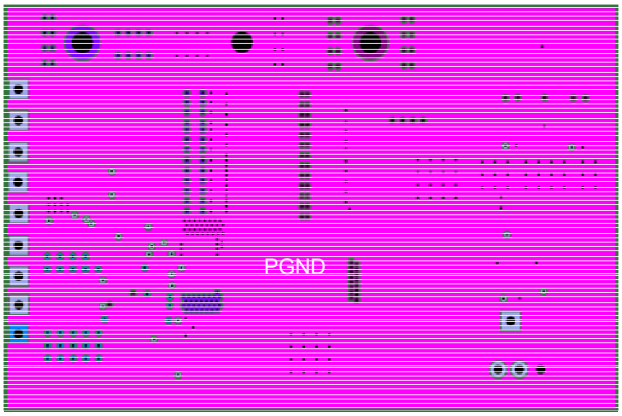


Figure 35c: IRDC1827 demoboard layout considerations – Mid Layer 1

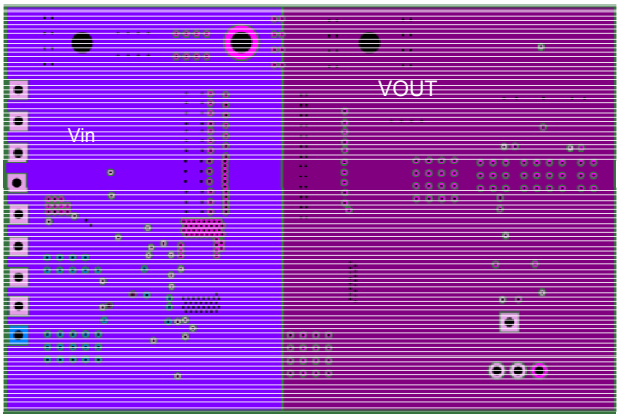


Figure 35d: IRDC1827 demoboard layout considerations – Mid Layer 2

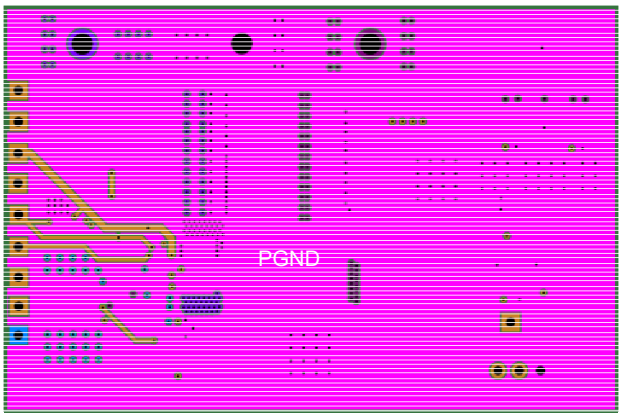


Figure 35e: IRDC1827 demoboard layout considerations – Mid Layer 3

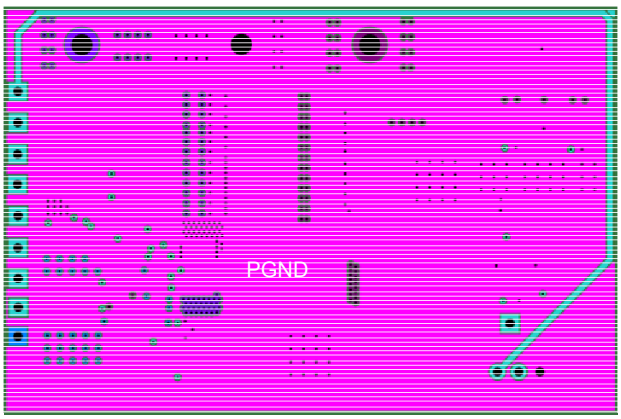


Figure 35f: IRDC1827 demoboard layout considerations – Mid Layer 4

METAL AND COMPONENT PLACEMENT

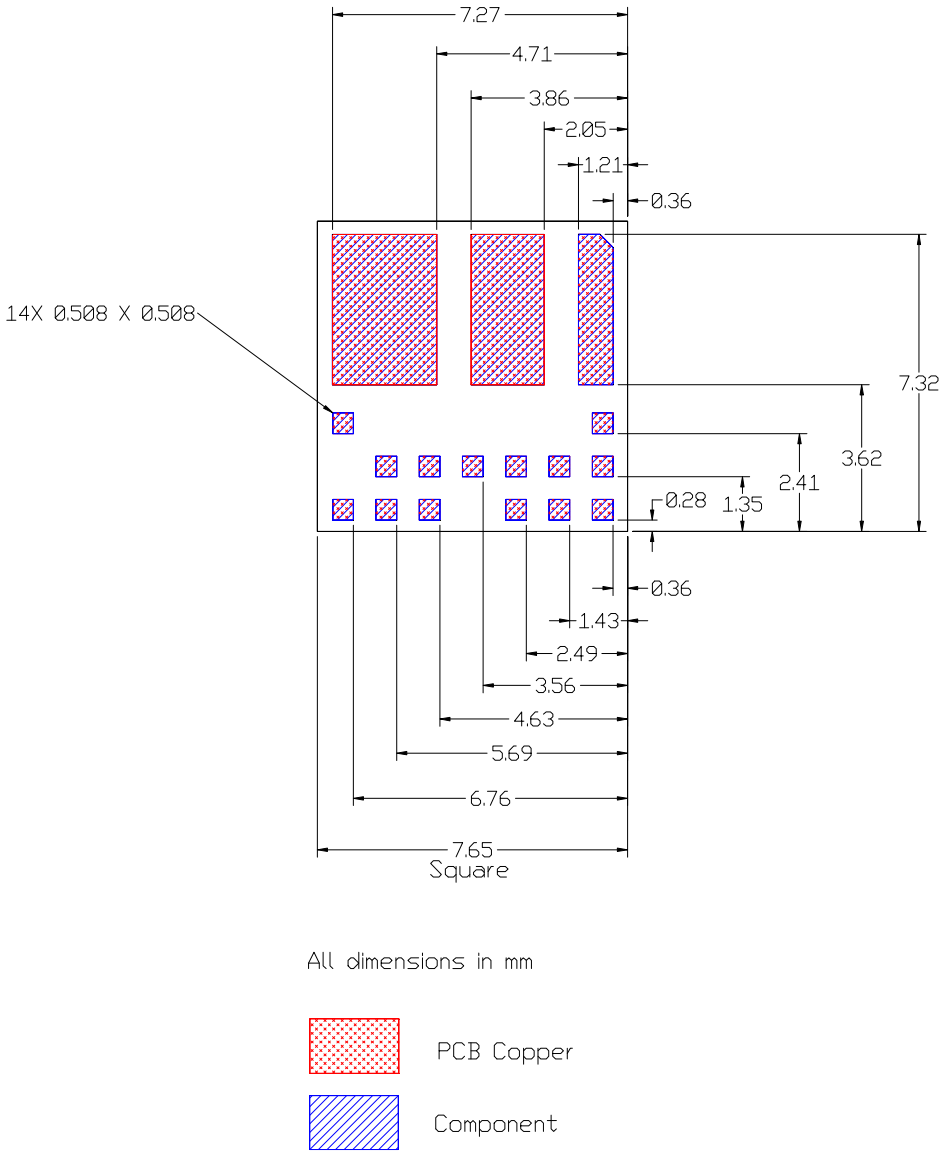


Figure 36: PCB Metal and Component Placement

* Contact International Rectifier to receive an electronic PCB Library file in your preferred format.

SOLDER RESIST

- It is recommended that the lead lands are Non Solder Mask Defined (NSMD). The solder resist should be pulled away from the metal lead lands by a minimum of 0.025mm to ensure NSMD pads.
- The three power land pads should be Solder Mask Defined (SMD), with a minimum overlap of the solder resist onto the copper of 0.05mm to accommodate solder resist mis-alignment.
- Ensure that the solder resist in-between the lead lands and the pad land is ≥ 0.15mm due to the high aspect ratio of the solder resist strip separating the lead lands from the power pad lands.

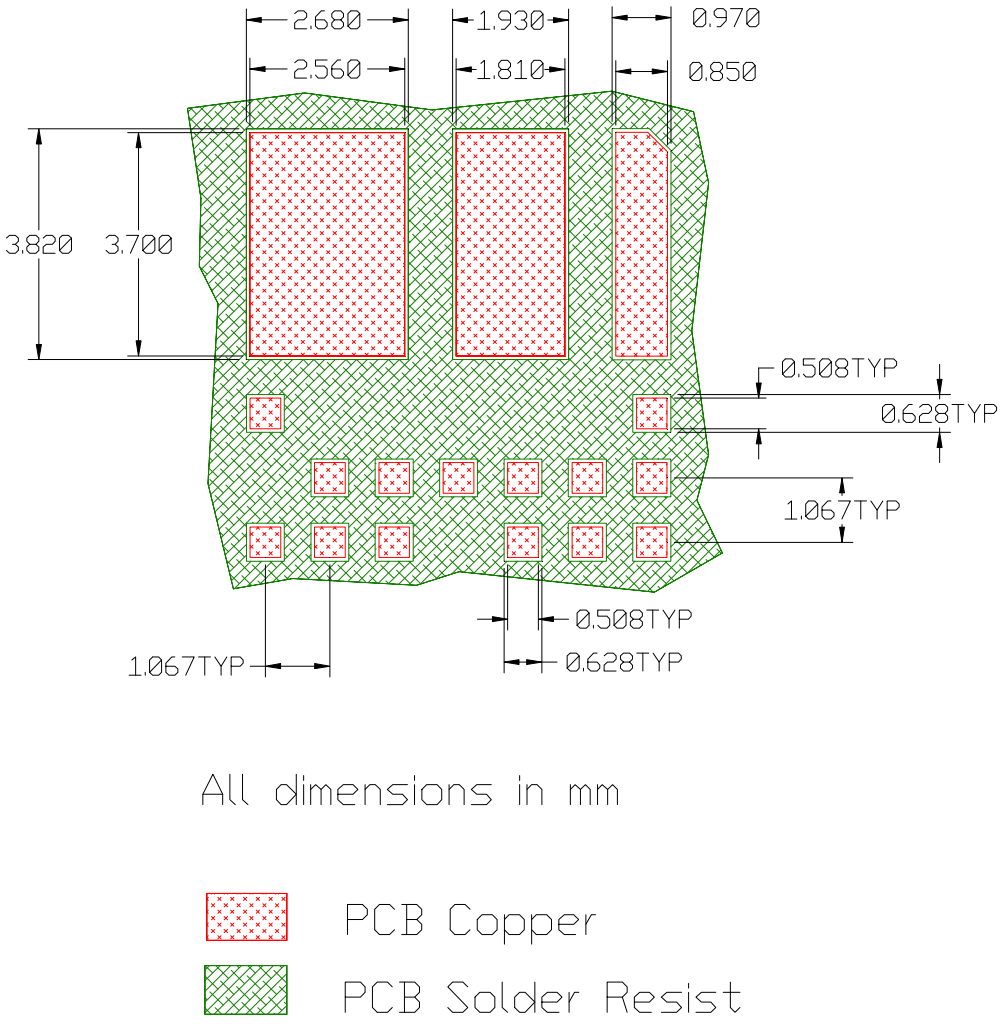


Figure 37: Solder resist

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STENCIL DESIGN

- The Stencil apertures for the lead lands should be approximately 80% of the area of the lead pads. Reducing the amount of solder deposited will minimize the occurrences of lead shorts. If too much solder is deposited on the three power land pads the part will float and the lead pads will be open.
- The maximum length and width of the power land pads stencil aperture should be equal to the solder resist opening minus an annular 0.2mm pull back to decrease the incidence of opens to the lead lands or use the recommended stencil design below.

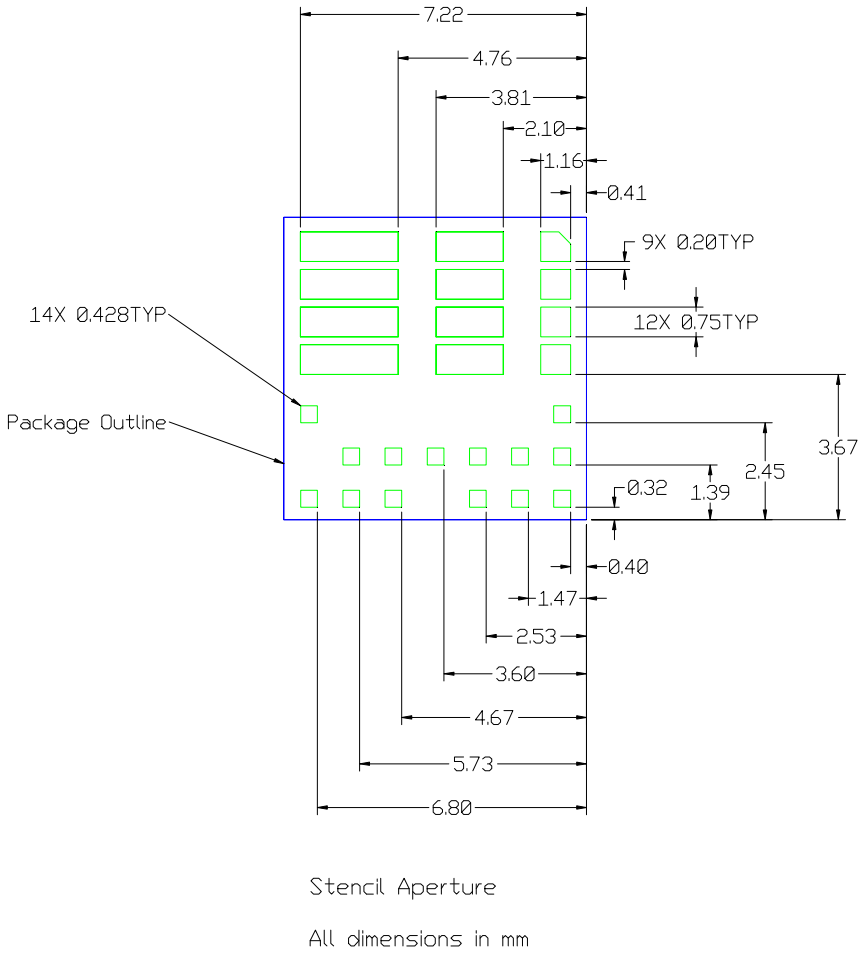

Figure 38: Stencil design

* Contact International Rectifier to receive an electronic PCB Library file in your preferred format.

MARKING INFORMATION

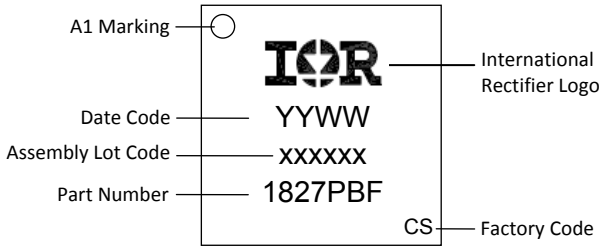

Figure 39: Marking Information

PACKAGE INFORMATION

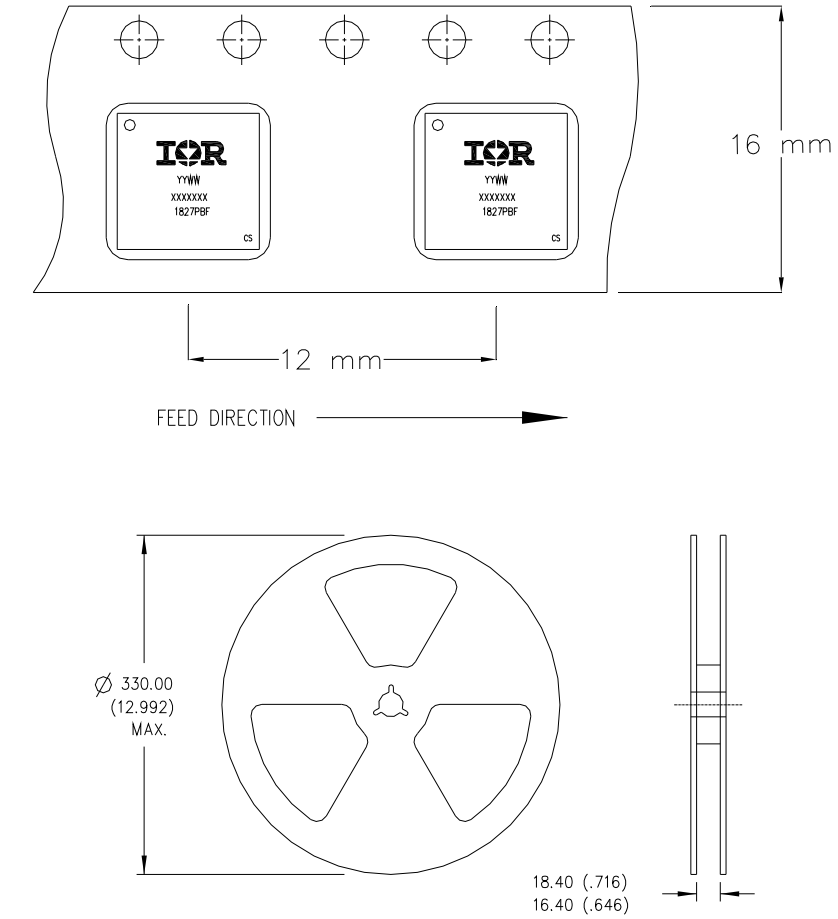

Figure 40: Tape and Reel Information

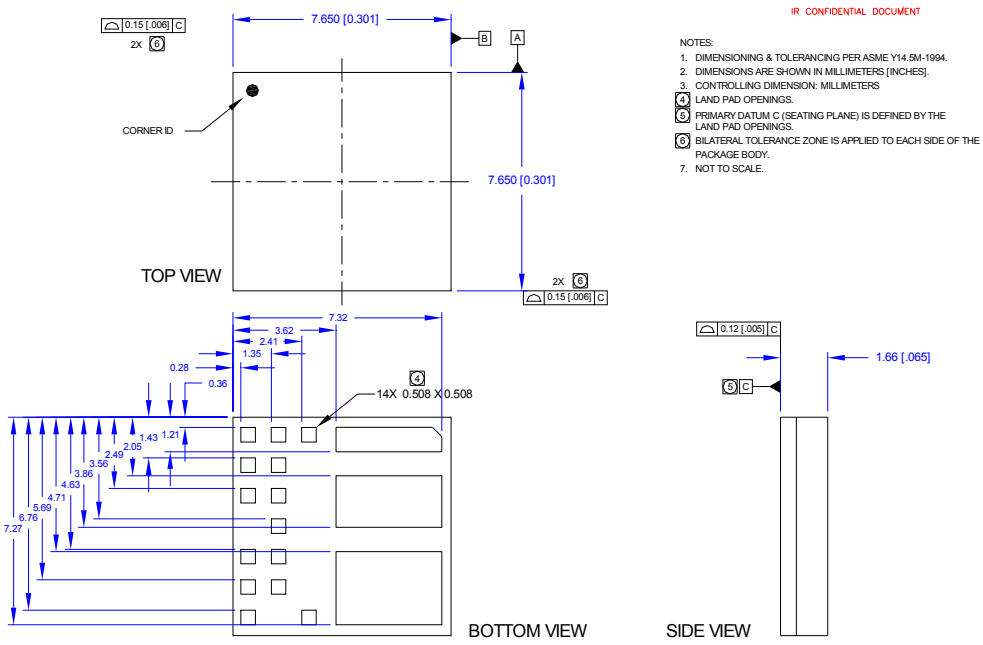

Figure 41: Mechanical Outline Drawing

Data and specifications subject to change without notice 12/10.
This product will be designed and qualified for the Consumer market.
Qualification Standards can be found on IR's Web site.

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