Dual LDO Regulator with Reset Function

General Description

The RT9006A/B is an efficient, precise dual-channel CMOS LDO regulator optimized for ultra-low-quiescent applications. Regulators output1 and output2 are capable of sourcing 300mA and 500mA of output current.

The RT9006' s performance is optimized for CD/DVD-ROM and CD/RW a supply applications.

The RT9006A/B regulators are stable with output capacitors as low as 1µF, including current limit, thermal shutdown protection, fast transient response, low dropout voltage, high output accuracy, current limiting protection, and high ripple rejection ratio. The RT9006A/B contains a reset circuit to detect VOUT2 voltage.

The RT9006A/B regulators are available in used SOP-8 (Exposed Pad) surface mount package.

Ordering Information

RT9006A/B □ □

- Package Type
  SP : SOP-8 (Exposed Pad-Option 2)
- Operating Temperature Range
  P : Pb Free with Commercial Standard
  G : Green (Halogen Free with Commercial Standard)
- Operating Frequency Version
  A : V_{OUT1} = 1.8V, V_{OUT2} = 3.3V
  B : V_{OUT1} = 1.5V, V_{OUT2} = 3.3V

Note :

Richtek Pb-free and Green products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.
- 100% matte tin (Sn) plating.

Features

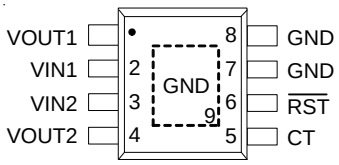
- **Low Quiescent Current (Typically 70µA)**
- **Wide Operating Voltage Ranges : 2.8V to 5.5V for RT9006A**
- **Wide Operating Voltage Ranges : 2.5V to 5.5V for RT9006B**
- **Ultra-Fast Transient Response**
- **Tight Load and Line Regulation**
- **Current Limiting Protection**
- **Thermal Shutdown Protection**
- **Only low-ESR Ceramic Capacitors Required for Stability**
- **RoHS Compliant and 100% Lead (Pb)-Free**

Applications

- CD/DVD-ROM, CD/RW
- Wireless LAN Card/Keyboard/Mouse
- Battery-Powered Equipment
- XDSL Router

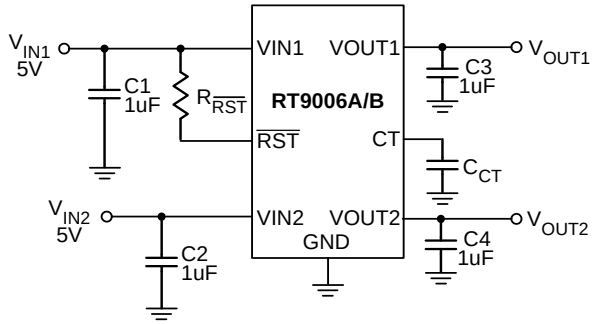
Pin Configurations

(TOP VIEW)



SOP-8 (Exposed Pad)

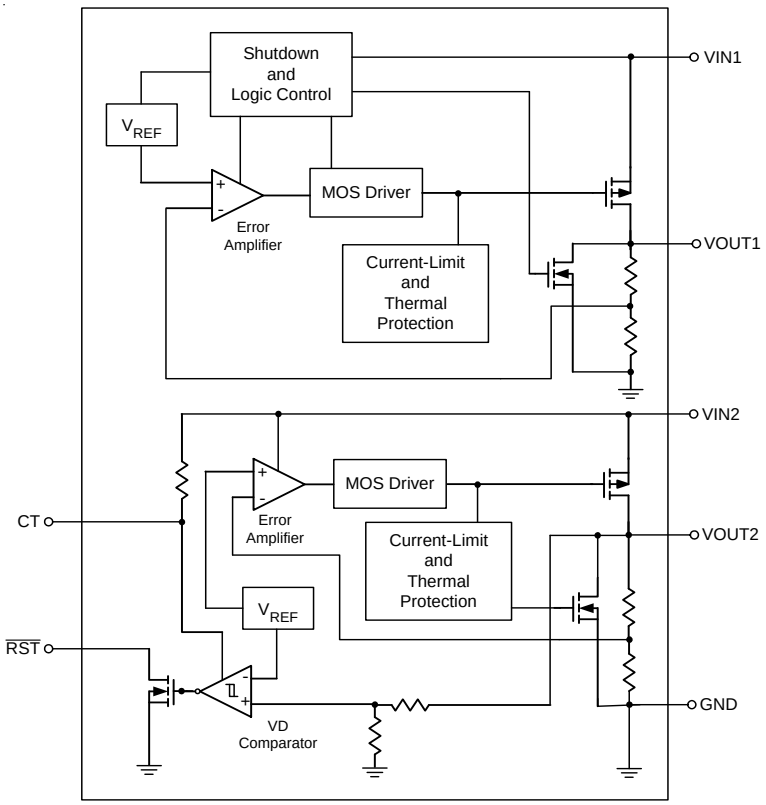
Typical Application Circuit



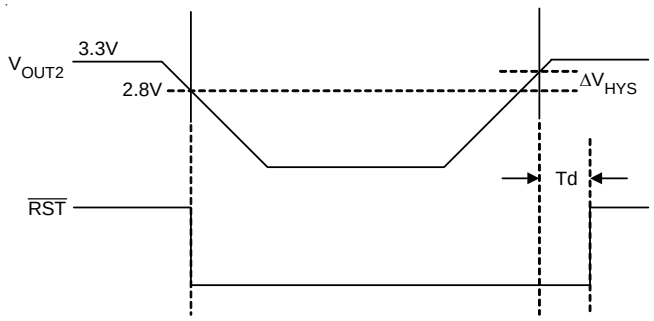
Functional Pin Description

Pin No.	Pin Name	Pin Function
1	VOUT1	Channel 1 Output Voltage
2	VIN1	Channel 1 Supply Voltage
3	VIN2	Channel 2 Supply Voltage
4	VOUT2	Channel 2 Output Voltage
5	CT	RESET Delay Capacitor
6	$\overline{RST}$	Detect VOUT2 Output Voltage
7, 8	GND	Common Ground
Exposed Pad (9)	GND	The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

Function Block Diagram



RESET Waveform



Absolute Maximum Ratings (Note 1)

- Input Voltage, V_{IN1}, V_{IN2} ---------- 6V
- Power Dissipation, P_D @ T_A = 25°C
  SOP-8 (Exposed Pad) ---------- 1.33W
- Package Thermal Resistance (Note 4)
  SOP-8 (Exposed Pad), θ_{JA} ---------- 75°C/W
  SOP-8 (Exposed Pad), θ_{JC} ---------- 28°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 2)
  HBM (Human Body Mode) ---------- 2kV
  MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 3)

- Input Voltage, V_{IN1}, V_{IN2} ---------- 2.8V to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{IN1} = V_{IN2} = 5V, C1 = C2 = 1µF, C3 = C4 = 1µF (Ceramic), T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Regulator 1						
Output Voltage Accuracy	V_{OUT1}	I_{OUT1} = 30mA (RT9006A)	1.773	1.8	1.827	V
		I_{OUT1} = 30mA (RT9006B)	1.478	1.5	1.523	
Output Voltage Temperature Coefficient		I_{OUT1} = 200mA (Note5)	--	--	80	ppm/°C
Load Regulation	ΔV_{LOAD1}	1mA < I_{OUT1} <100mA	--	5	30	mV
Line Regulation	V_{LINE1}	V_{IN1} = 2.8V to 5.5V, I_{OUT1} = 30mA (RT9006A)	--	0.1	0.2	%/V
		V_{IN1} = 2.5V to 5.5V, I_{OUT1} = 30mA (RT9006B)				
Power Supply Rejection Rate	PSRR1	f = 100Hz, I_{OUT1} = 100mA	--	–60	--	dB
Current Limit	I_{LIM1}	V_{IN1} = 5.0V, V_{OUT1} short to GND	400	--	600	mA
Quiescent Current	I_{Q1}	I_{OUT1} = 0A	--	30	--	mA
Thermal Shutdown Protection	T_{SD1}		--	170	--	°C
Thermal Shutdown Hysteresis	T_{SD1}		--	40	--	°C
Regulator 2						
Output Voltage Accuracy	V_{OUT2}	I_{OUT2} = 30mA	3.25	3.3	3.35	V
Output Voltage Temperature Coefficient		I_{OUT2} = 200mA (Note5)	--	--	80	ppm/°C

To be continued

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Load Regulation	ΔV_{LOAD2}	1mA < I_{OUT2} < 100mA	--	5	30	mV
Dropout Voltage	V_{DROP2_1}	I_{OUT2} = 30mA	--	50	90	mV
	V_{DROP2_2}	I_{OUT2} = 100mA	--	150	200	
Quiescent Current	I_{Q2}	I_{OUT2} = 0A	--	40	--	mA
Line Regulation	ΔV_{LINE2}	V_{IN2} = 4.3V to 5.5V, I_{OUT2} = 30mA	--	0.1	0.2	%/V
Power Supply Rejection Rate	PSRR2	f = 100Hz, I_{OUT2} = 100mA	--	–60	--	dB
Current Limit	I_{LIM2}	V_{IN2} = 5.0V, V_{OUT2} short to GND	500	--	700	mA
Thermal Shutdown Protection	T_{SD2}		--	170	--	°C
Thermal Shutdown Hysteresis	ΔT_{SD2}		--	40	--	°C
Detector						
Detect Falling Voltage	V_{DF}		2.744	2.8	2.856	V
Hysteresis	ΔV_{HYS}		--	--	140	mV
Sink Current	$I_{\overline{RST}}$	$V_{\overline{RST}}$ = 0.5V, V_{IN2} = 5.0V	7.0	12.0	--	mA
CT Source Current	I_{CT}		2.1	2.6	3.1	uA

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. The device is not guaranteed to function outside its operating conditions.

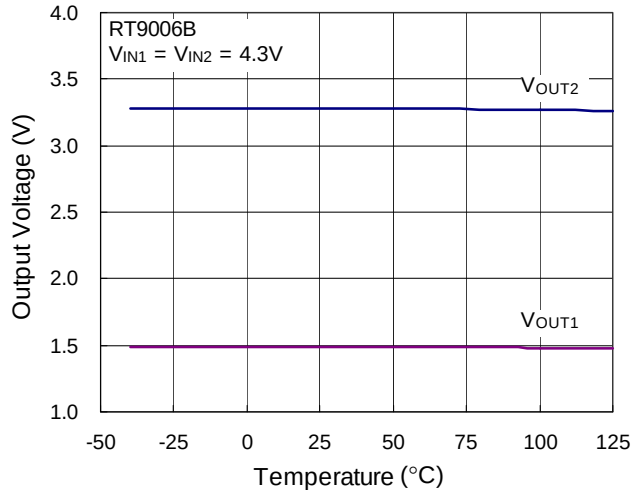
Note 4. θ_{JA} is measured in the natural convection at T_A = 25°C on a high effective thermal conductivity test board (4 Layers, 2S2P) of JEDEC 51-7 thermal measurement standard. The case point of θ_{JC} is on the expose pad for SOP-8 (Exposed Pad) package.

Note 5. Guaranteed by design.

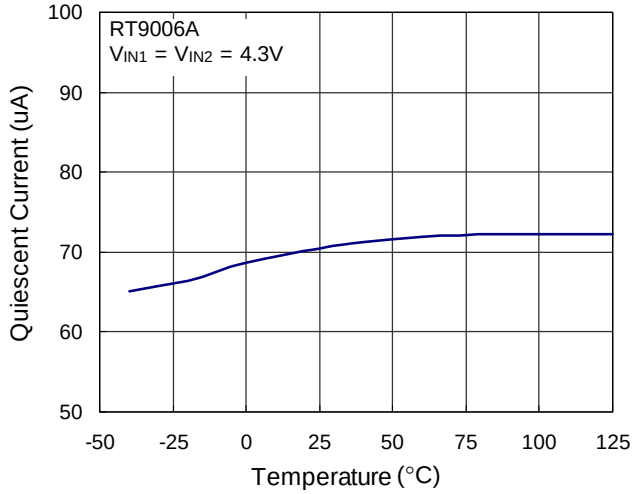
Typical Operating Characteristics

C1 = C2 = 1uF(X7R), C3 = C4 = 1uF(X7R), $R_{\overline{RST}}$ = 100kΩ, unless otherwise specified.

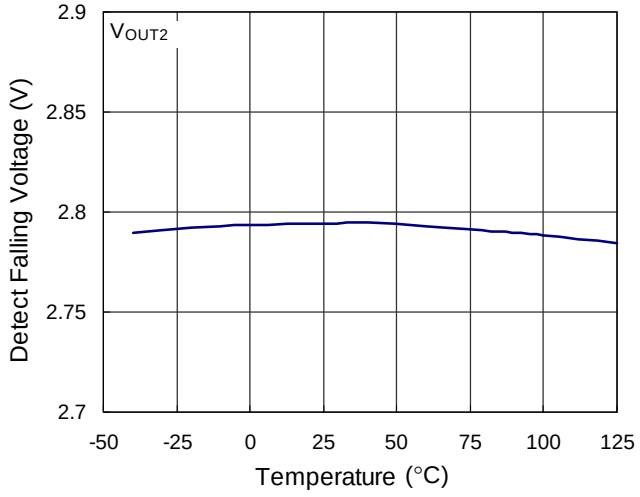
Output Voltage vs. Temperature



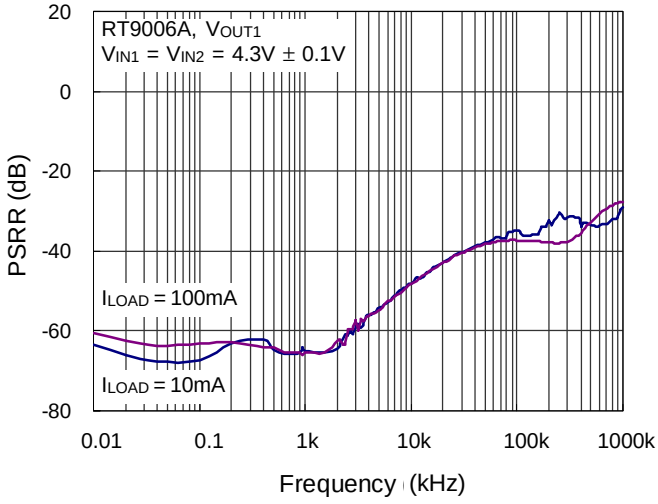
Quiescent Current vs. Temperature



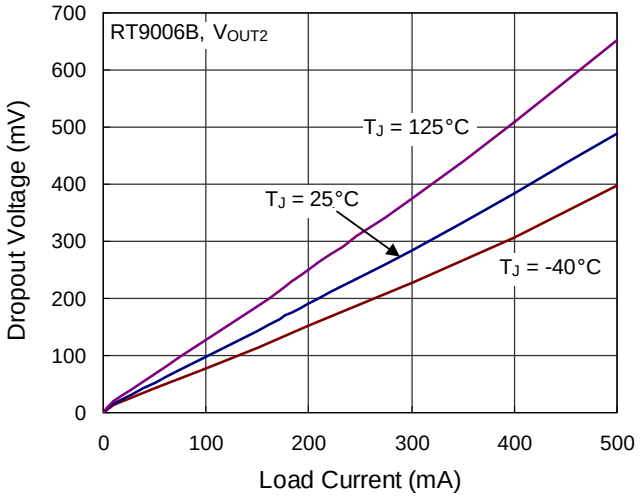
Detect Falling Voltage vs. Temperature



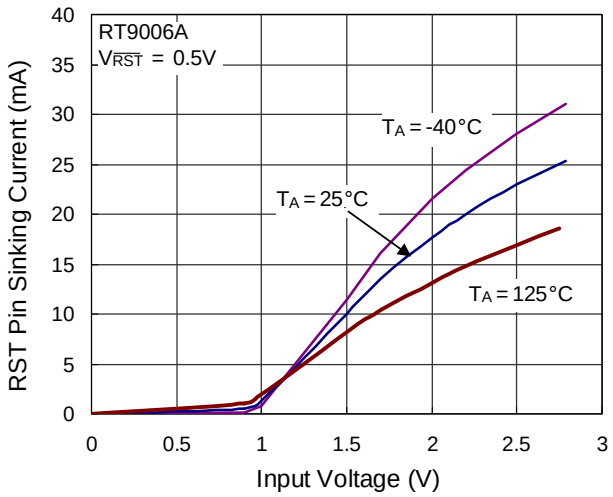
PSRR



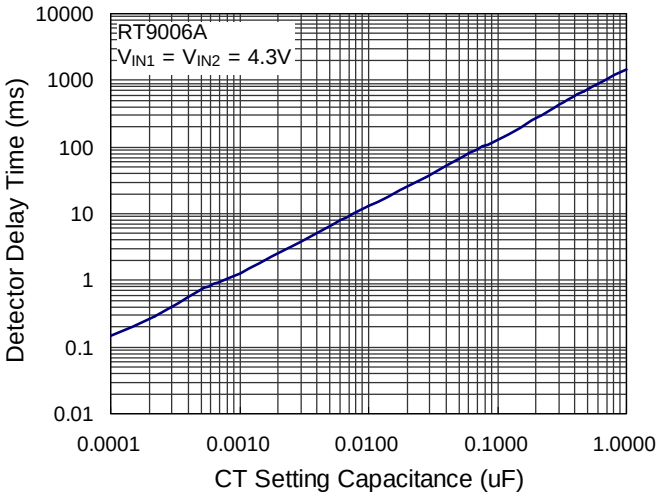
Dropout Voltage vs. Load Current



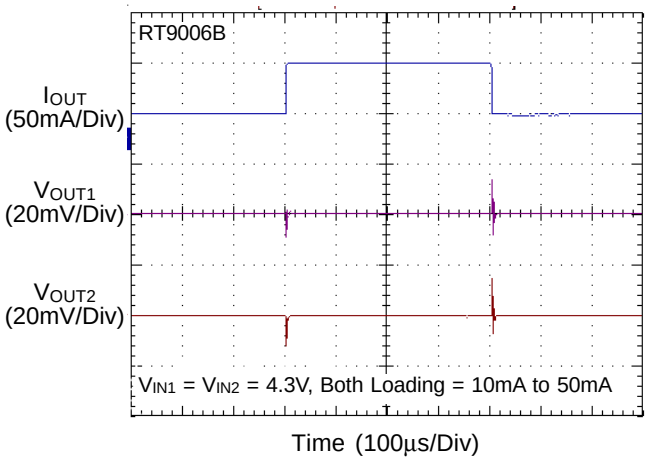
RST Pin Sinking Current vs. Input Voltage



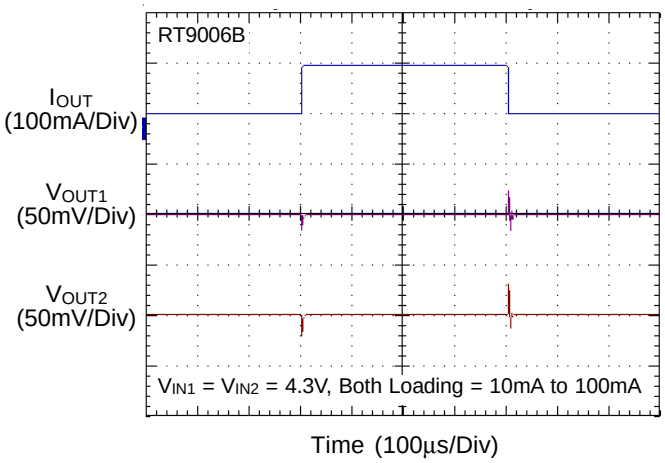
Detector Delay Time



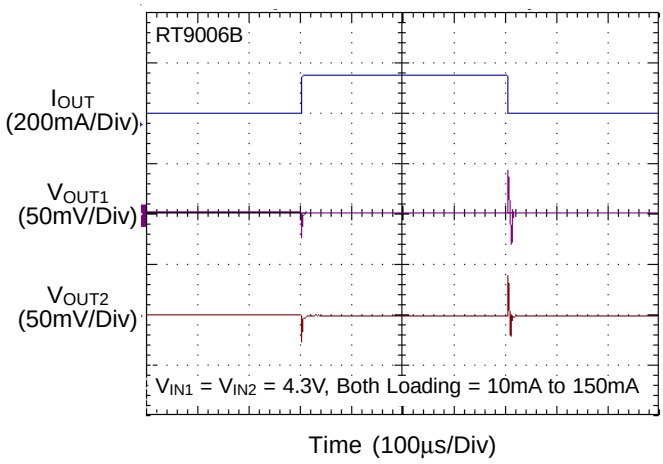
Load Transient Response



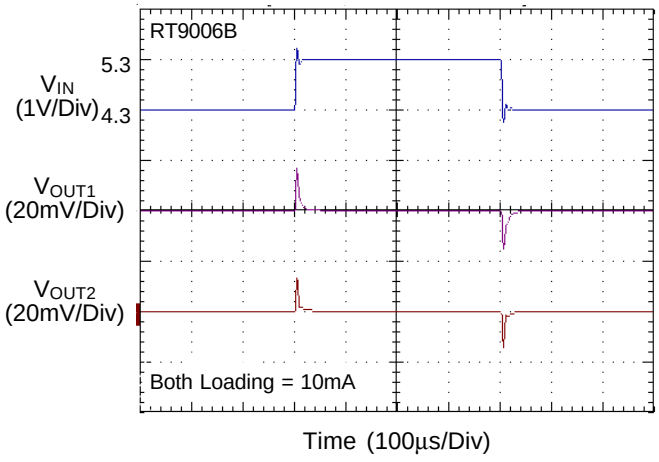
Load Transient Response



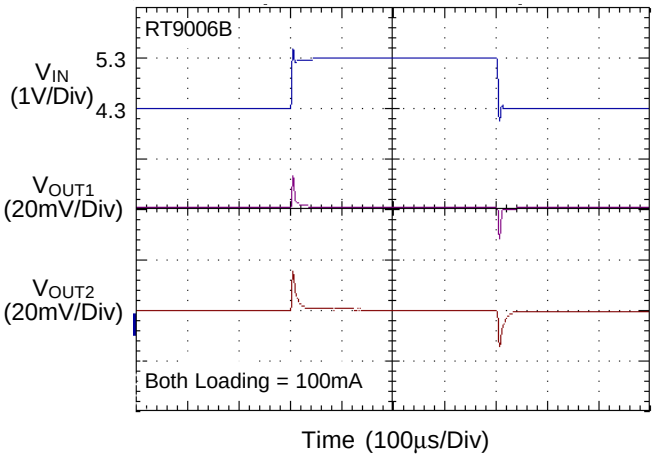
Load Transient Response



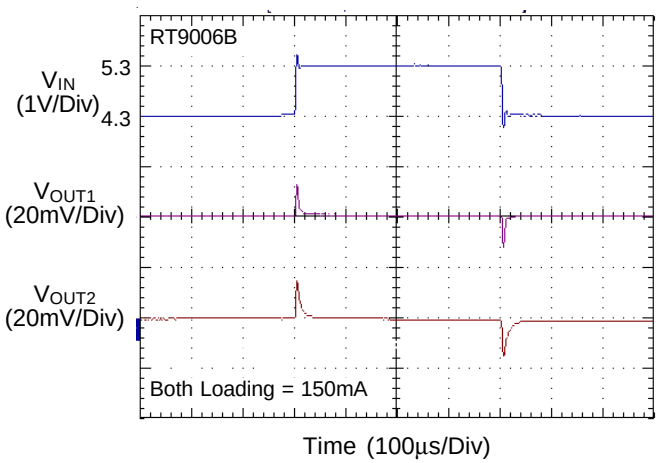
Line Transient Response



Line Transient Response



Line Transient Response



Application Information

Detector Delay Time

The delay time (T_d) of Reset signal from V_{OUT2} can be calculated from the formula :

$$T_d = C_{CT} \times \frac{0.8 \times V_{IN2}}{I_{CT}}$$

V_{IN2} is the input voltage of channel 2 and the I_{CT}(2.6uA.Typ.) is the CT pin sourcing current. C_{CT} is the capacitance of the external capacitor from CT pin to GND.

Current limit

The RT9006 contains two independent current limiters, which monitors and controls the pass transistor' s gate voltage, limiting the output current to a certain level. The typical current limit level of channel 1 and channel 2 is 450mA and 600mA respectively.

Thermal Consideration

For continued operation, do not exceed absolute maximum operation junction temperature 125°C. The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

Where

$T_{J(MAX)}$: The maximum operation junction temperature 125°C.

T_A : The operated ambient temperature.

θ_{JA} : The junction to ambient thermal resistance.

The junction to ambient thermal resistance for SOP-8 (Exposed Pad) package is 75°C/W on the standard JEDEC 51-7 (4 layers, 2S2P) thermal test board. The copper thickness is 2oz. The maximum power dissipation at T_A = 25°C can be calculated by following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / 75 °C/W = 1.33W {SOP-8 (Exposed Pad) packages}

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance θ_{JA}. For SOP-8 (Exposed Pad) packages, the Figure 1 of de-rating curves allows the designer to see the effect of rising ambient temperature on the maximum power allowed.

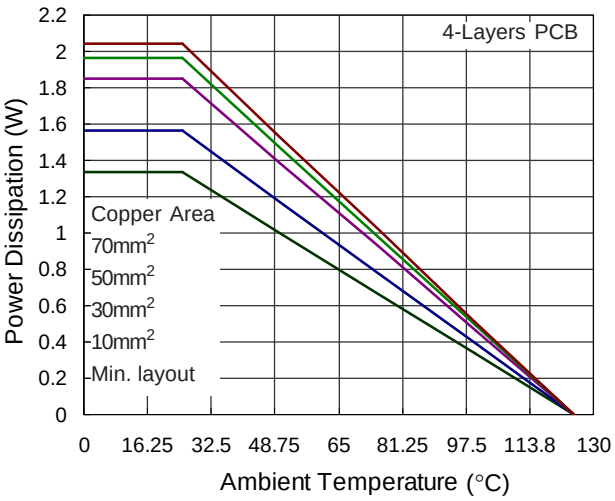
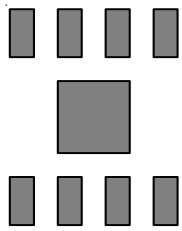


Figure 1. Derating Curves for SOP-8 (Exposed Pad) Package

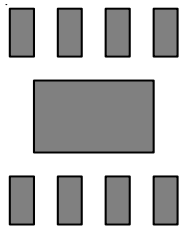
PCB Layout Considerations

The thermal resistance θ_{JA} of SOP-8 (Exposed Pad) is determined by the package design and the PCB design. However, the package design had been designed. If possible, it's useful to increase thermal performance by the PCB design. The thermal resistance θ_{JA} can be decreased by adding a copper under the exposed pad of SOP-8 (Exposed Pad) package.

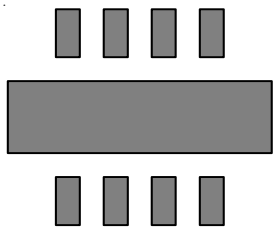
As shown in Figure 2, the amount of copper area to which the SOP-8 (Exposed Pad) is mounted affects thermal performance. When mounted to the standard SOP-8 (Exposed Pad) pad (Figure 2.a), θ_{JA} is 75°C/W. Adding copper area of pad under the SOP-8 (Exposed Pad) (Figure 2.b) reduces the θ_{JA} to 64°C/W. Even further, increasing the copper area of pad to 70mm^2 (Figure 2.e) reduces the θ_{JA} to 49°C/W.



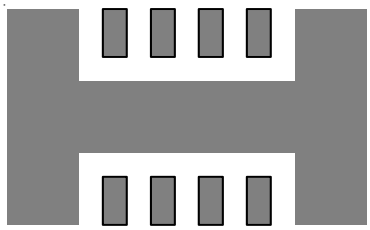
(a). Minimum Footprint, θ_{JA} = 75°C/W



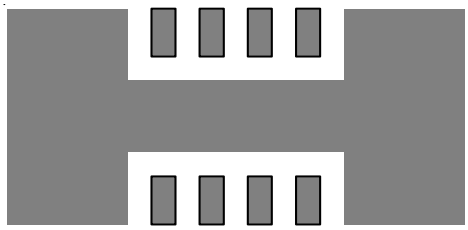
(b). Copper Area = 10mm^2, θ_{JA} = 64°C/W



(c). Copper Area = 30mm^2, θ_{JA} = 54°C/W



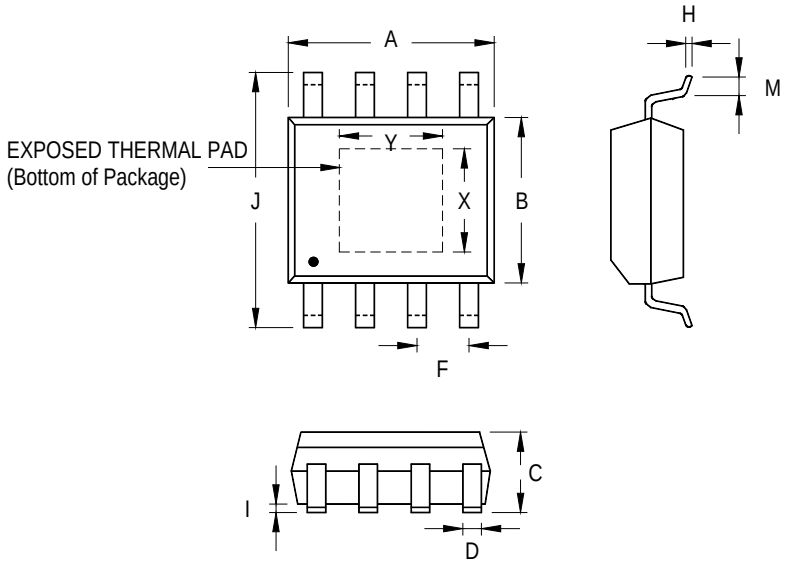
(d). Copper Area = 50mm^2, θ_{JA} = 51°C/W



(e). Copper Area = 70mm^2, θ_{JA} = 49°C/W

Figure 2. Thermal Resistance vs. Copper Area Layout Design

Outline Information



Symbol		Dimensions In Millimeters		Dimensions In Inches	
		Min	Max	Min	Max
A		4.801	5.004	0.189	0.197
B		3.810	4.000	0.150	0.157
C		1.346	1.753	0.053	0.069
D		0.330	0.510	0.013	0.020
F		1.194	1.346	0.047	0.053
H		0.170	0.254	0.007	0.010
I		0.000	0.152	0.000	0.006
J		5.791	6.200	0.228	0.244
M		0.406	1.270	0.016	0.050
Option 1	X	2.000	2.300	0.079	0.091
	Y	2.000	2.300	0.079	0.091
Option 2	X	2.100	2.500	0.083	0.098
	Y	3.000	3.500	0.118	0.138

8-Lead SOP (Exposed Pad) Plastic Package

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