2A, 2MHz, Synchronous Step-Down Converter

General Description

The RT8064 is a high efficiency synchronous, step-down DC/DC converter. Its input voltage range is from 2.7V to 5.5V and provides an adjustable regulated output voltage from 0.8V to 5V while delivering up to 2A of output current.

The internal synchronous low on-resistance power switches increase efficiency and eliminate the need for an external Schottky diode. The default switching frequency is set at 2MHz, if the RT pin is left open. It can also be varied from 200kHz to 2MHz by adding an external resistor. Current mode operation with external compensation allows the transient response to be optimized over a wide range of loads and output capacitors.

The RT8064 operates in forced continuous PWM Mode, which minimizes ripple voltage and reduces the noise and RF interference.

Ordering Information

RT8064 □□

- Package Type
  - SP : SOP-8 (Exposed Pad-Option 2)
  - QW : WDFN-8L 3x3 (W-Type)
- Lead Plating System
  - Z : ECO (Ecological Element with Halogen Free and Pb free)

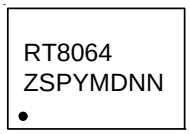
Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Marking Information

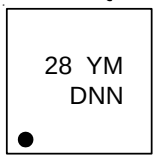
RT8064ZSP



RT8064ZSP : Product Number

YMDNN : Date Code

RT8064ZQW



28 : Product Code

YMDNN : Date Code

Features

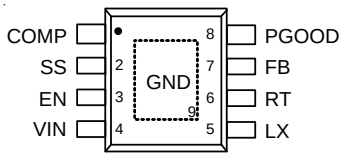
- **High Efficiency : Up to 95%**
- **Adjustable Frequency : 200kHz to 2MHz**
- **No Schottky Diode Required**
- **0.8V Reference Allows Low Output Voltage**
- **Forced Continuous Mode Operation**
- **Low Dropout Operation : 100% Duty Cycle**
- **Enable Function**
- **External Soft-Start**
- **Power Good Function**
- **RoHS Compliant and Halogen Free**

Applications

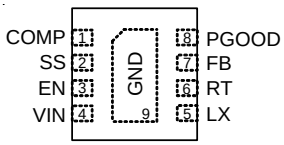
- LCD TV and Monitor
- Notebook Computers
- Distributed Power Systems
- IP Phones
- Digital Cameras

Pin Configurations

(TOP VIEW)



SOP-8 (Exposed Pad)



WDFN-8L 3x3

Typical Application Circuit

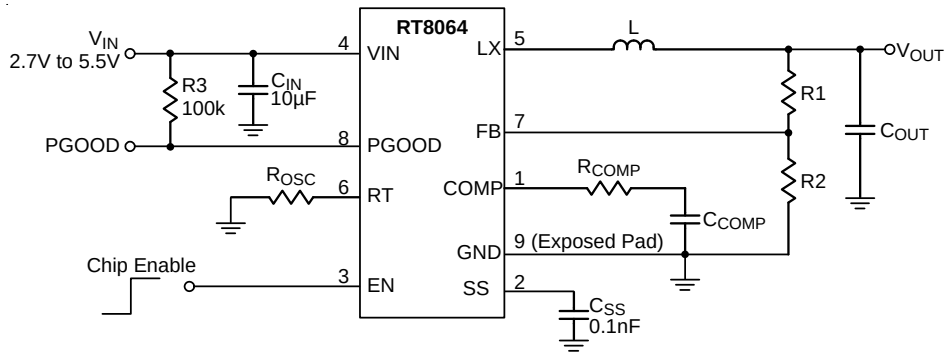


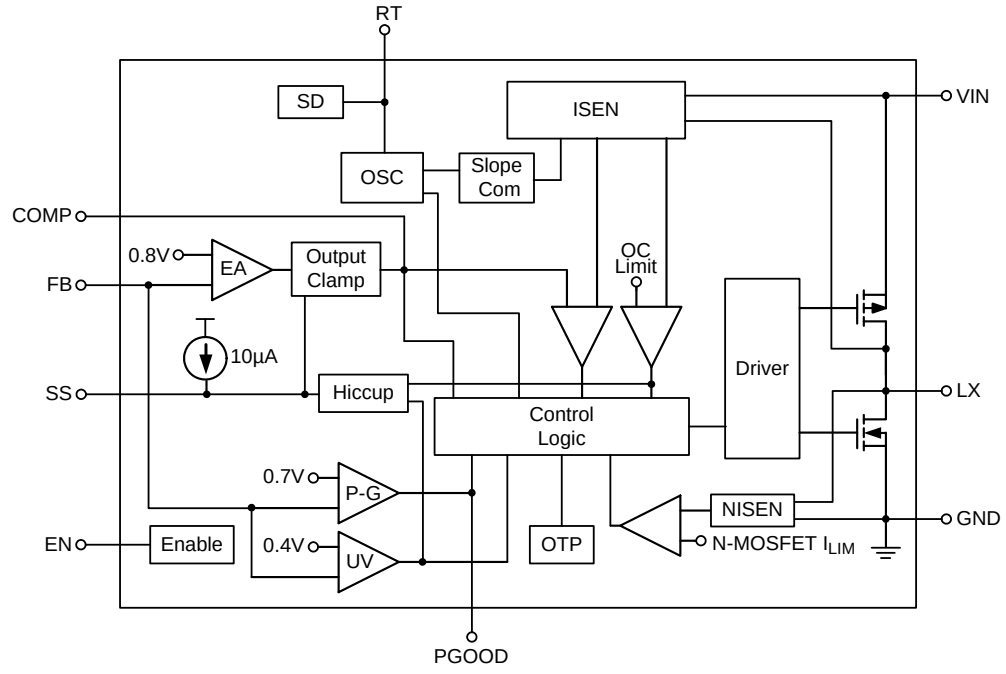
Table 1. Recommended Components Selection for f_{SW} = 1MHz

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	R_{COMP} (kΩ)	C_{COMP} (pF)	L (µH)	C_{OUT} (µF)
3.3	75	24	33	560	2	22
2.5	51	24	22	560	2	22
1.8	30	24	15	560	1.5	22
1.5	21	24	13	560	1.5	22
1.2	12	24	11	560	1.5	22
1	6	24	8.2	560	1.5	22

Functional Pin Description

Pin No.		Pin Name	Pin Function
SOP-8 (Exposed Pad)	WDFN-8L 3x3		
1	1	COMP	Error Amplifier Compensation Point. The current comparator threshold increases with this control voltage. Connect external compensation elements to this pin to stabilize the control loop.
2	2	SS	Soft-Start Control Input. Connect a capacitor from SS to GND to set the soft-start period. A 10nF capacitor sets the soft-start period to 800μs (typ.).
3	3	EN	Enable Control Input. Float or connect this pin to logic high for enable. Connect to GND for disable.
4	4	VIN	Power Input Supply. Decouple this pin to GND with a capacitor.
5	5	LX	Internal Power MOSFET Switches Output. Connect this pin to the inductor.
6	6	RT	Oscillator Resistor Input. Connect a resistor from this pin to GND sets the switching frequency. If this pin is floating, the frequency will be set at 2MHz internally.
7	7	FB	Feedback Pin. Receives the feedback voltage from a resistive divider connected across the output.
8	8	PGOOD	Power Good Indicator. This pin is an open drain logic output that is pulled to ground when the output voltage is not within ±12.5% of regulation point.
9 (Exposed Pad)	9 (Exposed Pad)	GND	Ground Pin. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

Function Block Diagram



Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, V_{IN} ---------- –0.3V to 6V
- LX Pin Switch Voltage ---------- –0.3V to (V_{IN} + 0.3V)
- Other I/O Pin Voltages ---------- –0.3V to (V_{IN} + 0.3V)
- LX Pin Switch Current ---------- 5A
- Power Dissipation, P_D @ T_A = 25°C
  - SOP-8 (Exposed Pad) ---------- 1.333W
  - WDFN-8L 3x3 ---------- 1.429W
- Package Thermal Resistance (Note 2)
  - SOP-8 (Exposed Pad), θ_{JA} ---------- 75°C/W
  - SOP-8 (Exposed Pad), θ_{JC} ---------- 15°C/W
  - WDFN-8L 3x3, θ_{JA} ---------- 70°C/W
  - WDFN-8L 3x3, θ_{JC} ---------- 8.2°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Mode) ---------- 2kV
  - MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, V_{IN} ---------- 2.7V to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{IN} = 3.3V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Feedback Reference Voltage	V_{REF}		0.784	0.8	0.816	V
DC Bias Current		Active , V_{FB} = 0.78V, Not Switching	--	460	--	μA
		Shutdown	--	--	10	
Output Voltage Line Regulation		V_{IN} = 2.7V to 5.5V	--	0.1	--	%/V
Output Voltage Load Regulation		0A < I_{LOAD} < 2A	--	0.25	--	%
Error Amplifier Trans-conductance	gm		--	400	--	μA/V
Current Sense Trans-resistance			--	0.3	--	Ω
Switching Frequency		R_{OSC} = 330kΩ	0.8	1	1.2	MHz
		Switching	0.2	--	2	
Enable Threshold Voltage	V_{IH}	EN Rising	1.6	--	--	V
	V_{IL}	EN Falling	--	--	0.4	
Switch On-Resistance, High	$R_{DS(ON)\_P}$	I_{LX} = 0.5A	--	180	250	mΩ
Switch On-Resistance, Low	$R_{DS(ON)\_N}$	I_{LX} = 0.5A	--	120	160	mΩ
Peak Current Limit	I_{LIM}		2.4	3.5	--	A
Under Voltage Lockout Threshold		V_{IN} Rising	--	2.4	--	V
		V_{IN} Falling	--	2.2	--	

To be continued

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
RT Shutdown Threshold	V_{RT}	V_{RT} Rising	--	V_{IN} – 0.7	V_{IN} – 0.4	V
Soft-Start Period	t_{SS}	C_{SS} = 10nF	--	800	--	μs
PGOOD Trip Threshold			--	87.5	--	%V_{OUT}

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

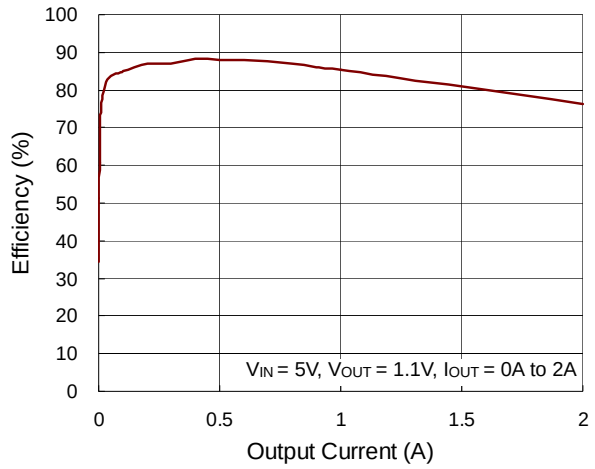
Note 2. θ_{JA} is measured in natural convection at T_A = 25°C on a high effective thermal conductivity four-layer test board of JEDEC 51-7 thermal measurement standard. The measurement case position of θ_{JC} is on the exposed pad of the packages.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

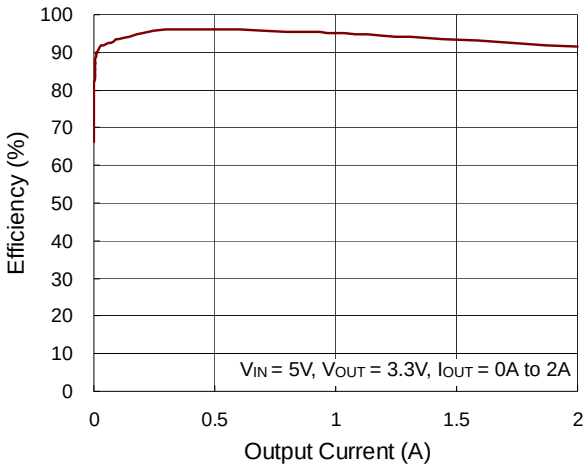
Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Operating Characteristics

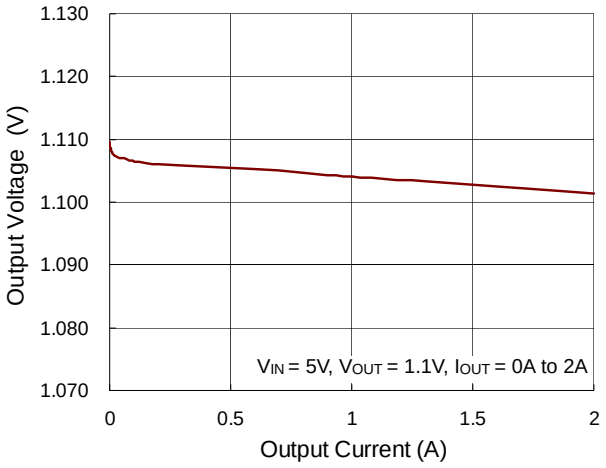
Efficiency vs. Output Current



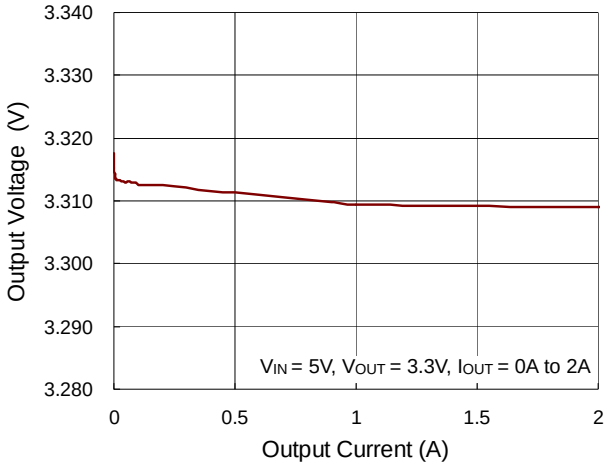
Efficiency vs. Output Current



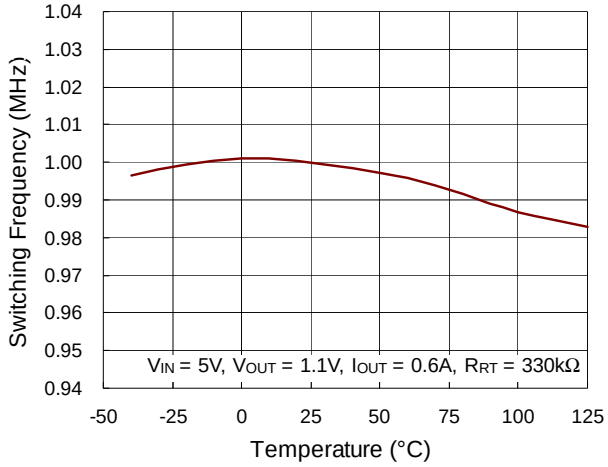
Output Voltage vs. Output Current



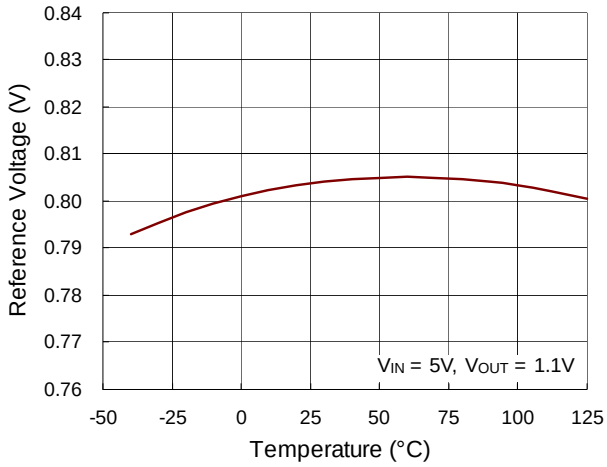
Output Voltage vs. Output Current



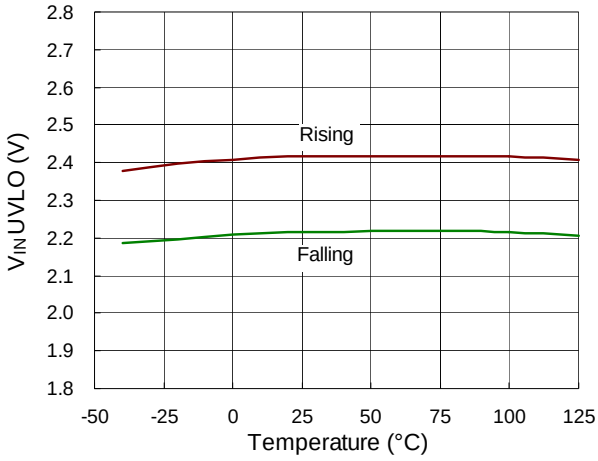
Switching Frequency vs. Temperature



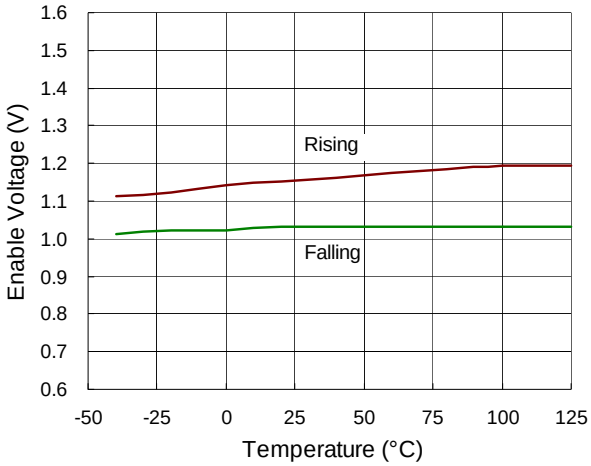
Reference Voltage vs. Temperature



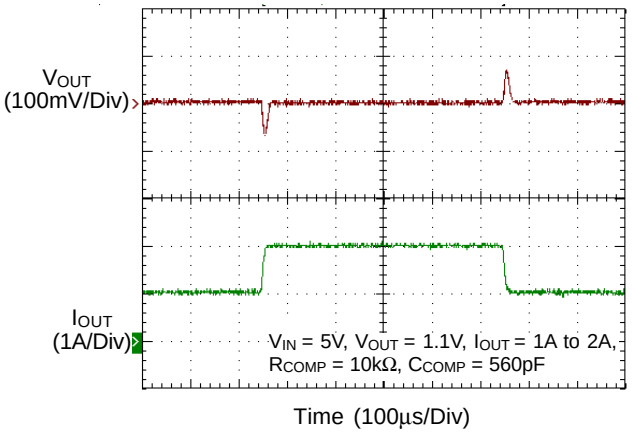
V_{IN} UVLO vs. Temperature



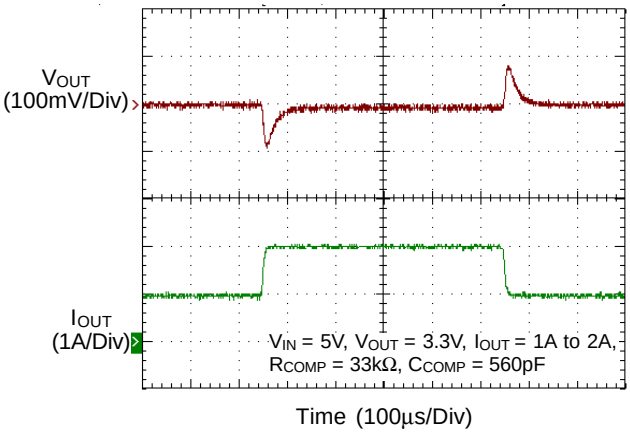
Enable Voltage vs. Temperature



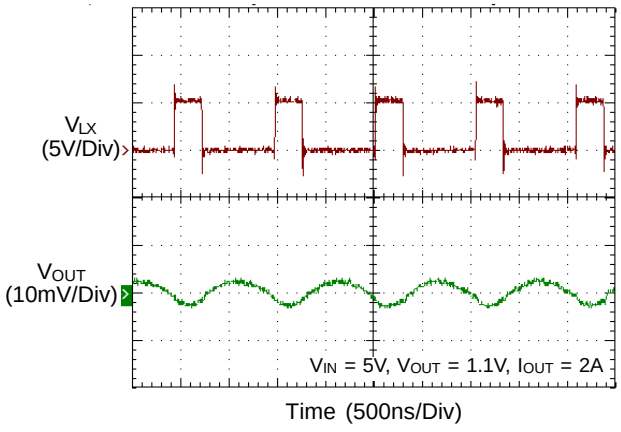
Load Transient Response



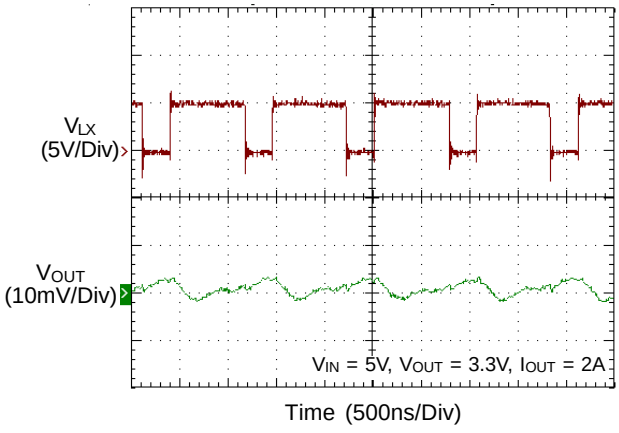
Load Transient Response



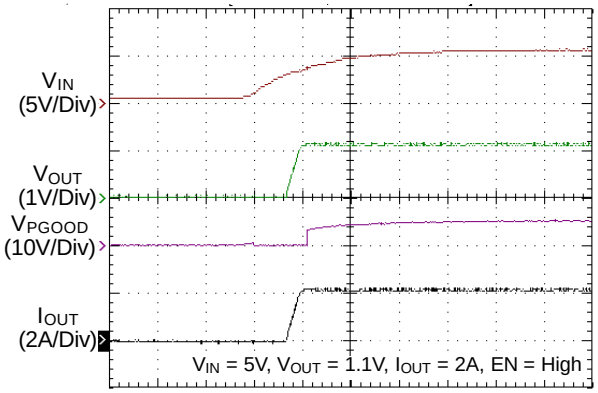
Switching



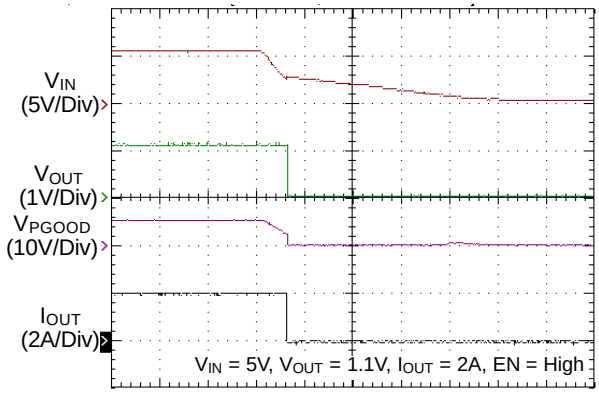
Switching



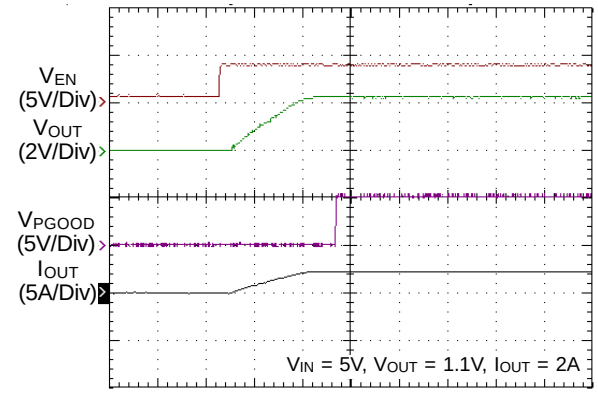
Power On from V_{IN}



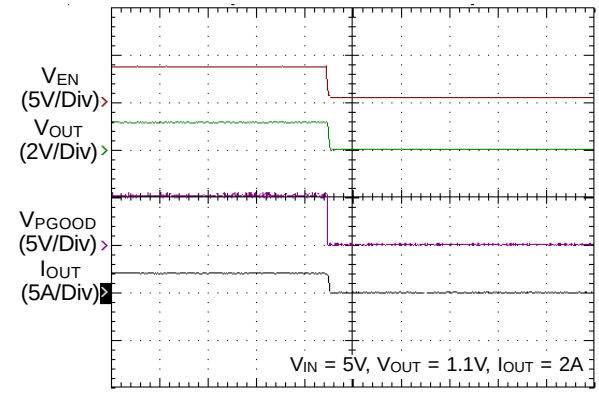
Power Off from V_{IN}



Power On from EN



Power Off from EN



Application Information

The basic IC application circuit is shown in Typical Application Circuit. External component selection is determined by the maximum load current and begins with the selection of the inductor value and operating frequency followed by C_{IN} and C_{OUT}.

Main Control Loop

During normal operation, the internal upper power switch (P-MOSFET) is turned on at the beginning of each clock cycle. Current in the inductor increases until the peak inductor current reaches the value defined by the output voltage (V_{COMP}) of the error amplifier. The error amplifier adjusts its output voltage by comparing the feedback signal from a resistive voltage divider on the FB pin with an internal 0.8V reference. When the load current increases, it causes a reduction in the feedback voltage relative to the reference. The error amplifier increases its output voltage until the average inductor current matches the new load current. When the upper power MOSFET shuts off, the lower synchronous power switch (N-MOSFET) turns on until the beginning of the next clock cycle.

Output Voltage Setting

The output voltage is set by an external resistive voltage divider according to the following equation :

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right)$$

where V_{REF} equals to 0.8V typical.

The resistive voltage divider allows the FB pin to sense a fraction of the output voltage as shown in Figure 1.

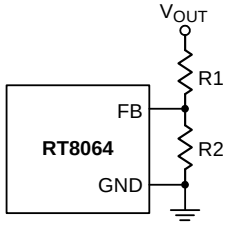


Figure 1. Setting the Output Voltage

Soft-Start

The IC contains an external soft-start clamp that gradually raises the output voltage. The soft-start timing is programmed by the external capacitor between SS pin and GND. The chip provides an internal 10μA charge current for the external capacitor. If 10nF capacitor is used to set the soft-start, the period will be 800μs (typ.).

Power Good Output

The power good output is an open-drain output and requires a pull up resistor. When the output voltage is 12.5% above or 12.5% below its set voltage, PGOOD will be pulled low. It is held low until the output voltage returns to within the allowed tolerances once more. During soft-start, PGOOD is actively held low and is only allowed to transition high when soft-start is over and the output voltage reaches 87.5% of its set voltage.

Operating Frequency

Selection of the operating frequency is a tradeoff between efficiency and component size. Higher frequency operation allows the use of smaller inductor and capacitor values. Lower frequency operation improves efficiency by reducing internal gate charge and switching losses but requires larger inductance and/or capacitance to maintain low output ripple voltage.

The operating frequency of the IC is determined by an external resistor, R_{OSC}, that is connected between the RT pin and ground. The value of the resistor sets the ramp current that is used to charge and discharge an internal timing capacitor within the oscillator. The practical switching frequency ranges from 200kHz to 2MHz. However, when the RT pin is floating, the internal frequency is set at 2MHz. Determine the RT resistor value by examining the curve below.

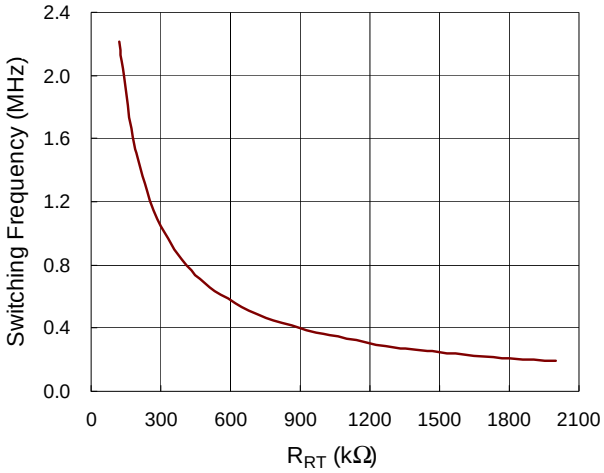


Figure 2. Switching Frequency vs. RT Resistor

Inductor Selection

For a given input and output voltage, the inductor value and operating frequency determine the ripple current. The ripple current, ΔI_L, increases with higher V_{IN} and decreases with higher inductance.

$$\Delta I_L = \left(\frac{V_{OUT}}{f \times L}\right) \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Having a lower ripple current reduces not only the ESR losses in the output capacitors but also the output voltage ripple. Highest efficiency operation is achieved by reducing ripple current at low frequency, but attaining this goal requires a large inductor.

For the ripple current selection, the value of $\Delta I_L = 0.4\ (I_{MAX})$ is a reasonable starting point. The largest ripple current occurs at the highest V_{IN}. To guarantee that the ripple current stays below a specified maximum value, the inductor value needs to be chosen according to the following equation :

$$L = \left[\frac{V_{OUT}}{f \times \Delta I_{L(MAX)}}\right] \times \left[1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right]$$

Using Ceramic Input and Output Capacitors

Higher values, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at the input and output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN} large enough to damage the part.

Slope Compensation and Peak Inductor Current

Slope compensation provides stability in constant frequency architectures by preventing sub-harmonic oscillations at duty cycles greater than 50%. It is accomplished internally by adding a compensating ramp to the inductor current signal. Normally, the peak inductor current is reduced when slope compensation is added. For the IC, however, separated inductor current signal is used to monitor over current condition, so the maximum output current stays relatively constant regardless of the duty cycle.

Hiccup Mode Under Voltage Protection

A Hiccup Mode Under Voltage Protection (UVP) function is provided for the IC. When the FB voltage drops below half of the feedback reference voltage, V_{FB}, the UVP function is triggered to auto soft-start the power stage until this event is cleared. The Hiccup Mode UVP reduces the input current in short circuit conditions, but will not be triggered during soft-start process.

Under Voltage Lockout Threshold

The RT8064 includes an input under voltage lockout protection (UVLO) function. If the input voltage exceeds the UVLO rising threshold voltage, the converter will reset and prepare the PWM for operation. However, if the input voltage falls below the UVLO falling threshold voltage during normal operation, the device will stop switching. The UVLO rising and falling threshold voltage has a hysteresis to prevent noise caused reset.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications of the RT8064, the maximum junction temperature is 125°C and T_A is the ambient temperature. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For SOP-8 (Exposed Pad) packages, the thermal resistance, θ_{JA}, is 75°C/W on a standard JEDEC 51-7 four-layer thermal test board. For WDFN-8L 3x3 packages, the thermal resistance, θ_{JA}, is 70°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power

dissipation at T_A =25°C can be calculated by the following formulas :

$P_{D(MAX)}$ = (125°C – 25°C) / (75°C/W) = 1.333W for SOP-8 (Exposed Pad) package

$P_{D(MAX)}$ = (125°C – 25°C) / (70°C/W) = 1.429W for WDFN-8L 3x3 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. For the RT8064 package, the derating curves in Figure 3 allow the designer to see the effect of rising ambient temperature on the maximum power dissipation.

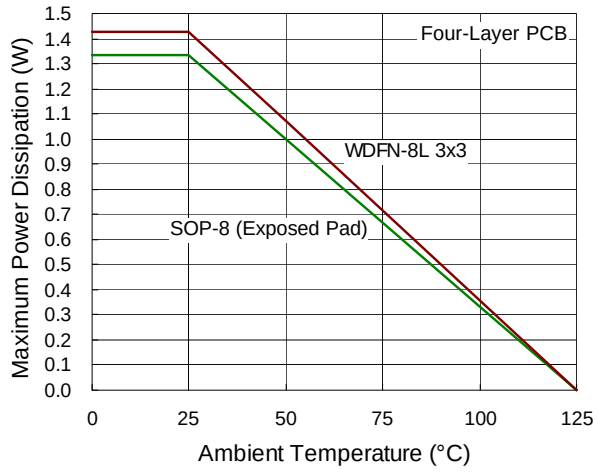


Figure 3. Derating Curves for the RT8064 Package

Layout Considerations

Follow the PCB layout guidelines for optimal performance of the IC.

- Connect the terminal of the input capacitor (s), C_{IN}, as close to the VIN pin as possible. This capacitor provides the AC current into the internal power MOSFETs.
- LX node experiences high frequency voltage swings so should be kept within a small area.
- Keep all sensitive small signal nodes away from the LX node to prevent stray capacitive noise pick up.
- Connect the FB pin directly to the feedback resistors. The resistive voltage divider must be connected between V_{OUT} and GND.

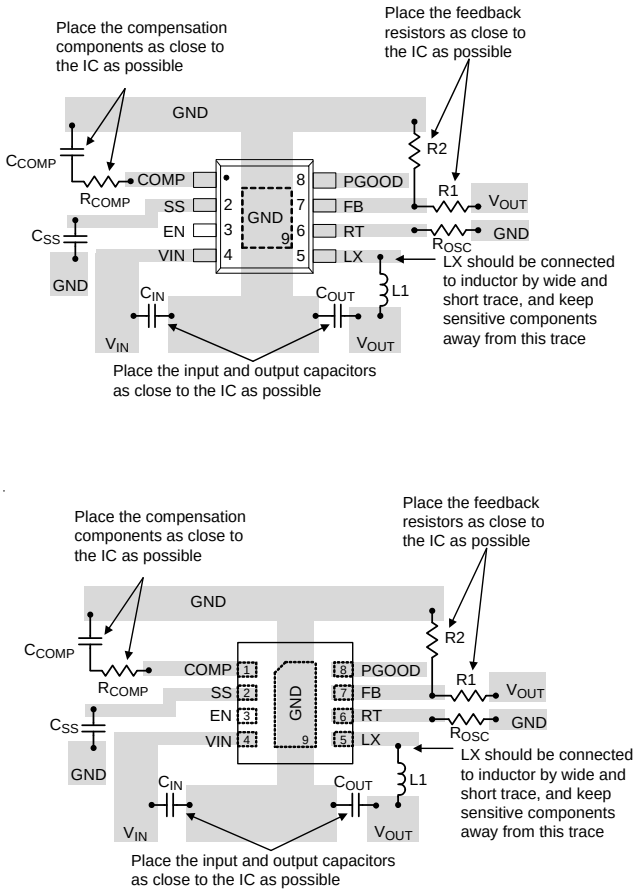
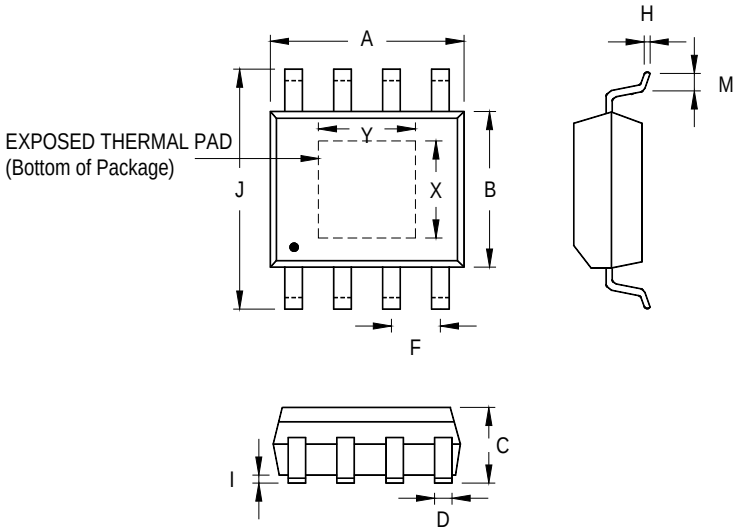


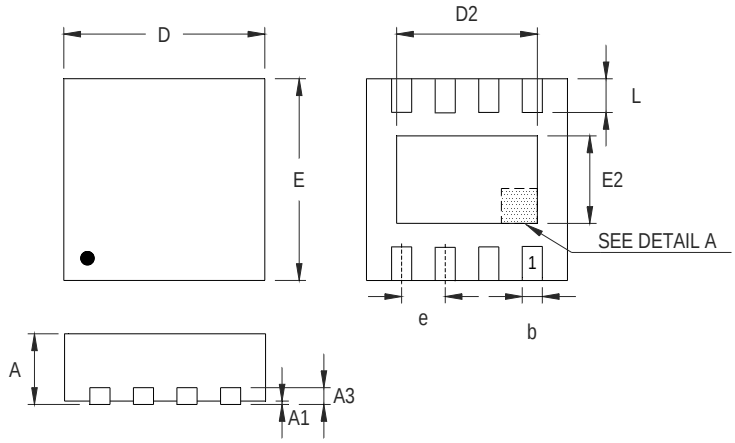
Figure 4. PCB Layout Guide

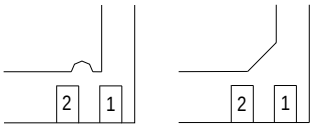
Outline Dimension



Symbol		Dimensions In Millimeters		Dimensions In Inches	
		Min	Max	Min	Max
A		4.801	5.004	0.189	0.197
B		3.810	4.000	0.150	0.157
C		1.346	1.753	0.053	0.069
D		0.330	0.510	0.013	0.020
F		1.194	1.346	0.047	0.053
H		0.170	0.254	0.007	0.010
I		0.000	0.152	0.000	0.006
J		5.791	6.200	0.228	0.244
M		0.406	1.270	0.016	0.050
Option 1	X	2.000	2.300	0.079	0.091
	Y	2.000	2.300	0.079	0.091
Option 2	X	2.100	2.500	0.083	0.098
	Y	3.000	3.500	0.118	0.138

8-Lead SOP (Exposed Pad) Plastic Package





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.200	0.300	0.008	0.012
D	2.950	3.050	0.116	0.120
D2	2.100	2.350	0.083	0.093
E	2.950	3.050	0.116	0.120
E2	1.350	1.600	0.053	0.063
e	0.650		0.026	
L	0.425	0.525	0.017	0.021

W-Type 8L DFN 3x3 Package

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