Dual 1A/1.5A-1.2MHz Synchronous Step-Down Converters

General Description

The RT8012A is a dual PWM, current mode, stepdown converter. Its input voltage range is from 2.6V to 5.5V and has a constant 1.2MHz switching frequency, allowing the use of tiny, low cost capacitors and inductors 2mm or less in height. Each output voltage is adjustable from 0.8V to 5V. Internal power switches with low on-resistance of the dual step-down regulators increase efficiency and eliminate the need for external Schottky diodes. The RT8012A can run at 100% duty cycle for low dropout operation that extends battery life in portable systems. With independent Enable and Power-Good pins, it is easy to control the power up sequence of the two converters, which is important in some applications.

Ordering Information

RT8012A □□

Package Type
QW : WQFN-16L 4x4 (W-Type)

Operating Temperature Range
P : Pb Free with Commercial Standard
G : Green (Halogen Free with Commercial Standard)

Note :

RichTek Pb-free and Green products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.
- 100% matte tin (Sn) plating.

Marking Information

For marking information, contact our sales representative directly or through a RichTek distributor located in your area, otherwise visit our website for detail.

Features

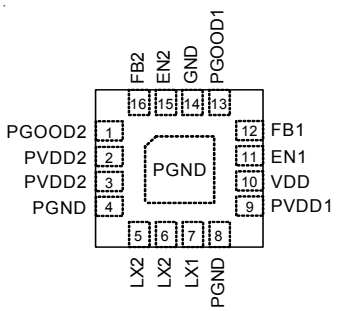
- **High Efficiency : Up to 95%**
- **1.2MHZ Constant Switching Frequency**
- **1A and 1.5A Load Current on Each Channel Respectively**
- **Low $R_{DS(ON)}$ Internal Switches**
- **No Schottky Diode Required**
- **0.8V Reference Allows Low Output Voltage**
- **Low Dropout Operation : 100% Duty Cycle**
- **Internally Compensated**
- **< 2μA Shutdown Current**
- **Power Good Output Voltage Monitor**
- **Internal Soft-Start**
- **Easy Power Sequence Control**
- **Over temperature Protection**
- **Short Circuit Protection**
- **Thermally Enhanced 16-Lead WQFN Package**
- **RoHS Compliant and 100% Lead (Pb)-Free**

Applications

- Portable Instruments
- Microprocessors and DSP Core Supplies
- Cellular Phones
- Wireless and DSL Modems
- PC Cards
- Digital Cameras

Pin Configurations

(TOP VIEW)



WQFN-16L 4x4

Typical Application Circuit

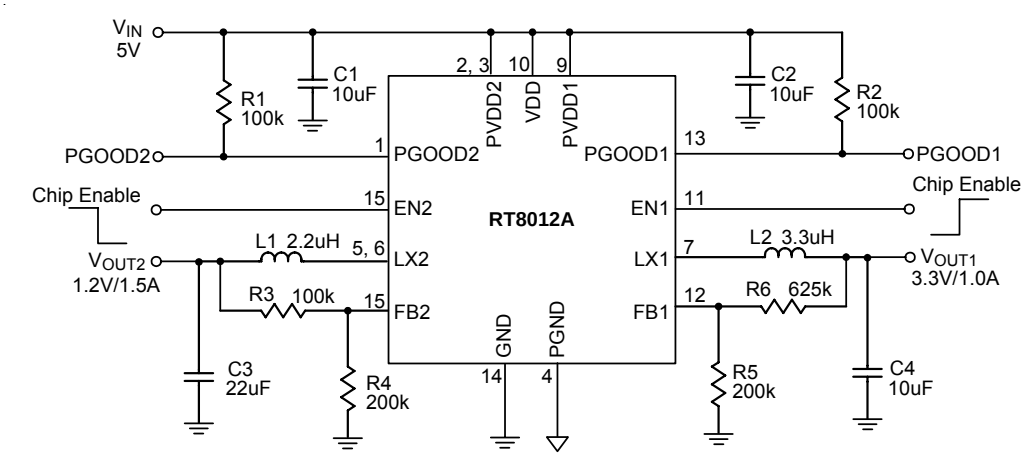


Figure 1. Dual Output 3.3V and 1.2V Step Down Regulators

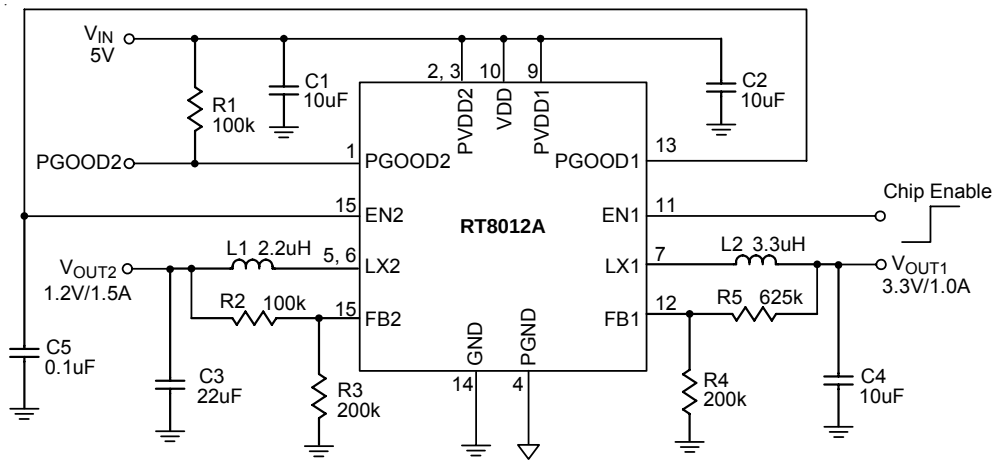
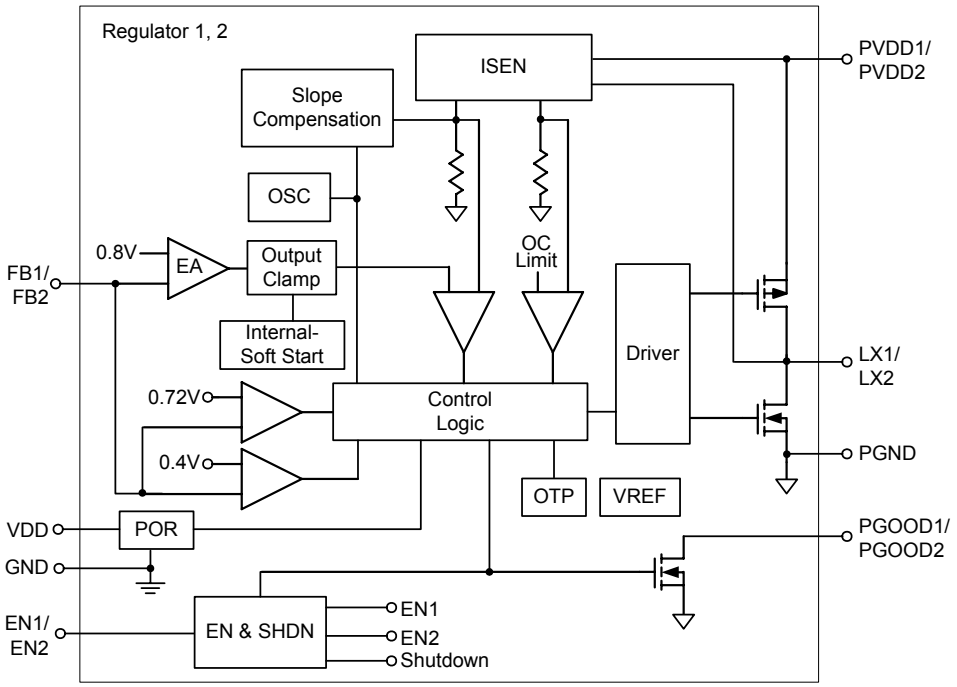


Figure 2. Dual Output 3.3V and 1.2V Step Down Regulators (Power up sequence is 3.3V first and then 1.2V).

Functional Pin Description

Pin Number	Pin Name	Pin Function
1	PGOOD2	Power Good Indicator of Regulator 2. Open-drain logic output that is opened when the output voltage exceeds 90% of the regulation point.
2,3	PVDD2	Power Input Supply of Regulator 2. Decouple this pin to PGND with a capacitor.
4,8, Exposed Pad	PGND	Power Ground. Exposed pad should be soldered to PCB board and connected to GND.
5,6	LX2	Internal Power MOSFET Switches Output of Regulator 2. Connect this pin to the inductor.
7	LX1	Internal Power MOSFET Switches Output of Regulator 1. Connect this pin to the inductor.
9	PVDD1	Power Input Supply of Regulator 1. Decouple this pin to PGND with a capacitor.
10	VDD	Signal Input Supply. Decouple this pin to GND with a capacitor. Normally V_{DD} is equal to PVDD1 and PVDD2. Keep the voltage difference between V_{DD}, PVDD1 and PVDD2 less than 0.5V.
11	EN1	Regulator 1 Chip Enable. A logic high level at this pin enables Regulator 1, while a logic low level causes Regulator 1 to shut down.
12	FB1	Feedback Pin of Regulator 1. Receives the feedback voltage from a resistive divider connected across the output.
13	PGOOD1	Power Good Indicator of Regulator 1. Open-drain logic output that is opened when the output voltage exceeds 90% of the regulation point.
14	GND	Signal Ground. Return the feedback resistive dividers to this ground, which in turn connects to PGND at one point.
15	EN2	Regulator 2 Chip Enable. A logical high level at this pin enables regulator 2, while a logic low level causes Regulator 2 to shut down. A 1μA pull up current from V_{DD} will be injected to EN2 pin when Regulator 1 is ready (V_{FB1} exceeds 90% of regulation point). Tie this pin to PGOOD1 and add a capacitor between this pin and GND will introduce a delay time before enabling Regulator 2. The delay time can be adjusted by different capacitance.
16	FB2	Feedback Pin of Regulator 2. Receives the feedback voltage from a resistive divider connected across the output.

Function Block Diagram



Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, VDD, PVDD1, PVDD2 ---------- –0.3V to 6V
- LX1, LX2 Pin Voltage ---------- –0.3V to (V_{DD} + 0.3V)
- Other I/O Pin Voltages ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  WQFN-16L 4x4 ---------- 1.852W
- Package Thermal Resistance (Note 4)
  WQFN-16L 4x4, θ_{JA} ---------- 54°C/W
  WQFN-16L 4x4, θ_{JC} ---------- 7°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 2)
  HBM (Human Body Mode) ---------- 2kV
  MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 3)

- Supply Input Voltage, VDD, PVDD1, PVDD2 ---------- 2.6V to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(PVDD1 = PVDD2 = V_{DD} = 3.6V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Input Voltage Range	V_{DD}		2.6	--	5.5	V
Feedback Reference Voltage	V_{REF}		0.784	0.8	0.816	V
DC Bias Current (PVDD1, PVDD2, VDD total)		Active, not Switching, V_{FB1}, V_{FB1} = 0.75V	500	830	1100	μA
		EN1, EN2 = 0	--	--	2	μA
Under Voltage Lockout Threshold		V_{DD} Rising	2.3	2.43	2.55	V
		V_{DD} Hysteresis	--	150	--	mV
FB Threshold for PGOOD Transition			0.68	0.72	0.76	V
PGOOD Pull-Down Resistance			--	--	100	Ω
Switching Frequency		Switching Frequency	1.0	1.2	1.4	MHz
EN1 Input High			1.4	--	--	V
EN1 Input Low			--	--	0.4	V
EN2 Threshold		EN2 Rising	0.85	1	1.15	V
		EN2 Hysteresis	--	200	--	mV
EN2 Delay		C5 = 0.1uF	70	100	130	ms
EN2 Pull-up current (Note 5)			--	1	--	μA

To be continued

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Regulator 1						
Switch On Resistance, High	R_{FET_H}	I_{SW} = 0.2A	--	300	450	mΩ
Switch On Resistance, Low	R_{FET_L}	I_{SW} = 0.2A	--	260	390	mΩ
Peak Current Limit	I_{LIM}		1.2	1.6	2.2	A
Output Voltage Line Regulation		V_{IN} = 2.6V to 5.5V	--	--	1	%V
Output Voltage Load Regulation		Measured by sever loop, EA output from 0.773V to 1.376V	--	--	1	%
Regulator 2						
Switch On Resistance, High	R_{FET_H}	I_{SW} = 0.5A	--	180	300	mΩ
Switch On Resistance, Low	R_{FET_L}	I_{SW} = 0.5A	--	90	150	mΩ
Peak Current Limit	I_{LIM}		1.7	2.2	3	A
Output Voltage Line Regulation		V_{IN} = 2.6V to 5.5V	--	--	1	%V
Output Voltage Load Regulation		Measured by sever loop, EA output from 0.336V to 0.948V	--	--	1	%

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution recommended.

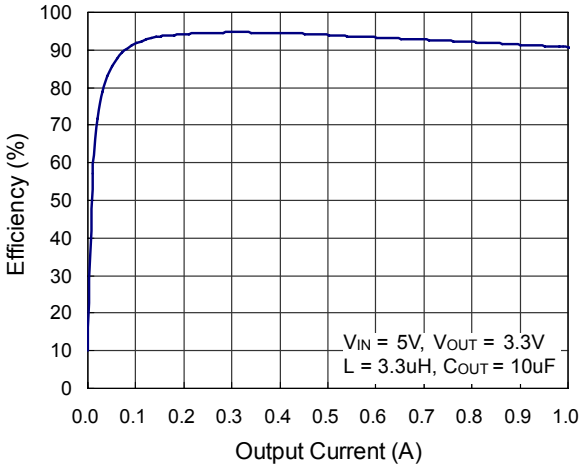
Note 3. The device is not guaranteed to function outside its operating conditions.

Note 4. θ_{JA} is measured in the natural convection at T_A = 25°C on a high effective four layers thermal conductivity test board of JEDEC 51-7 thermal measurement standard. The case point of θ_{JC} is on the expose pad for the QFN package.

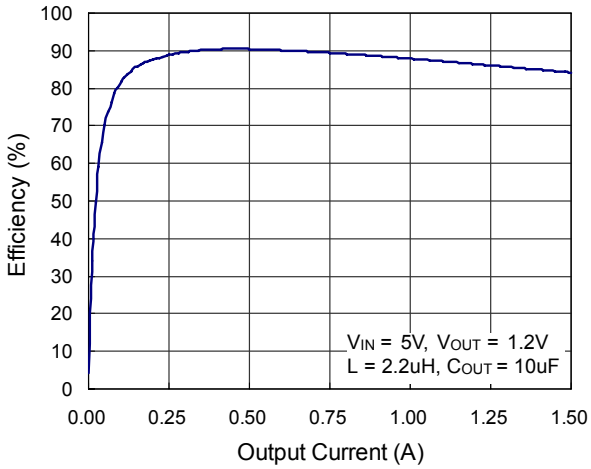
Note 5. EN2 pull-up current only is activated when Regulator-1 is ready (V_{FB1} > 0.72V). No pull-up current (<0.1μA) appear when V_{FB1} < 0.72V.

Typical Operating Characteristics

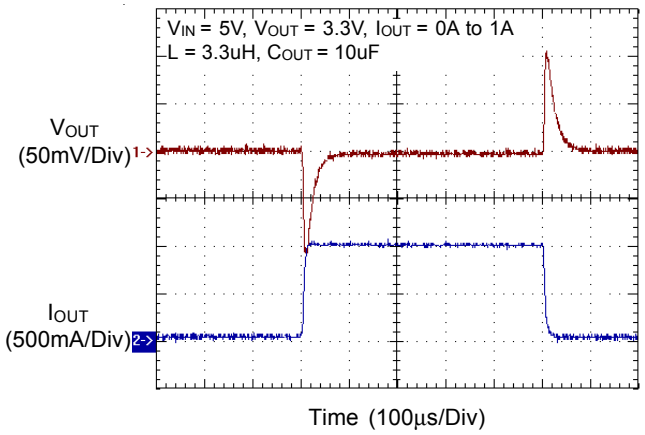
Regulator 1 Efficiency vs. Output Current



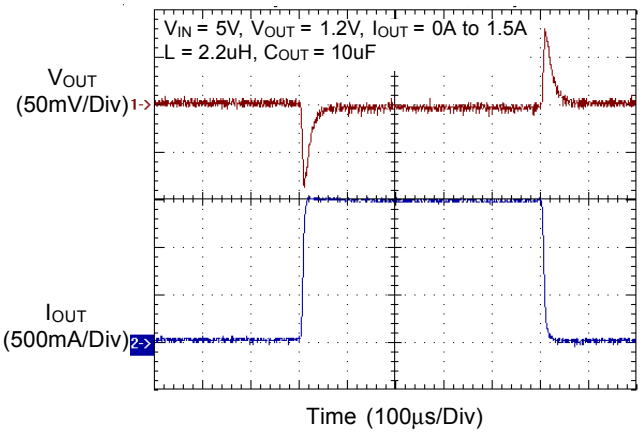
Regulator 2 Efficiency vs. Output Current



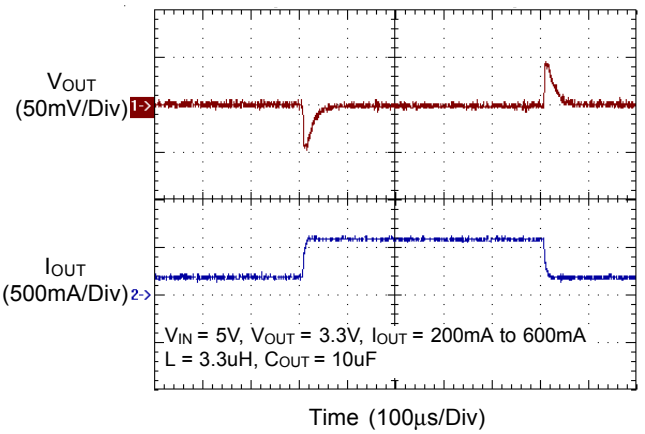
Regulator 1 Load Transient Response



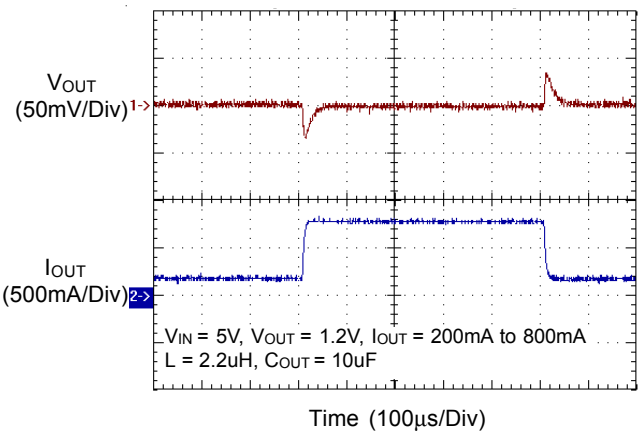
Regulator 2 Load Transient Response



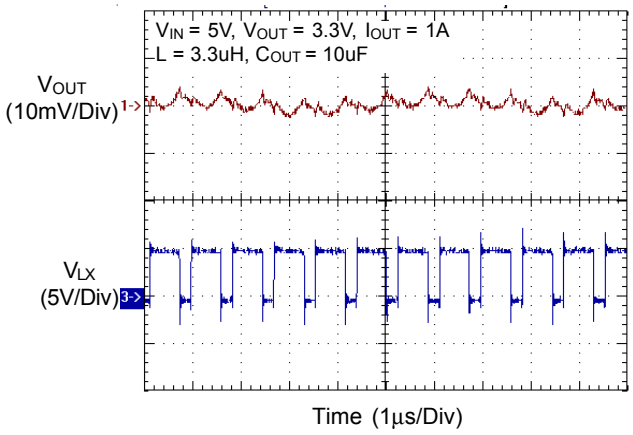
Regulator 1 Load Transient Response



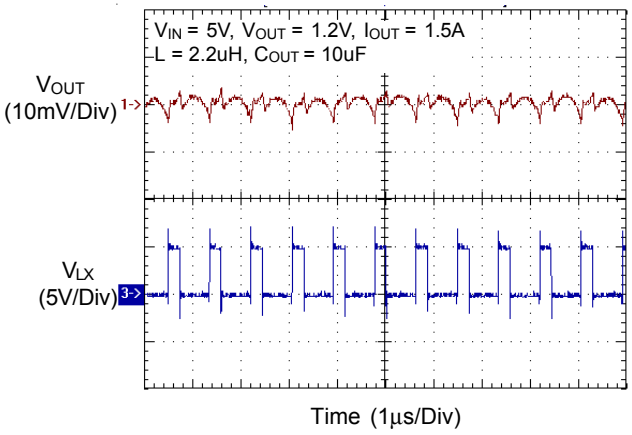
Regulator 2 Load Transient Response



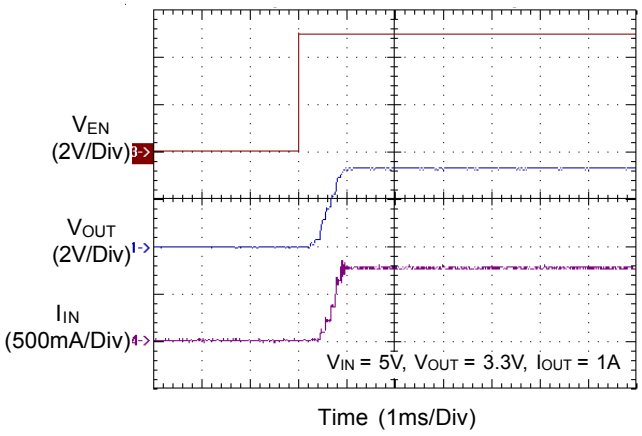
Regulator 1 Ripple



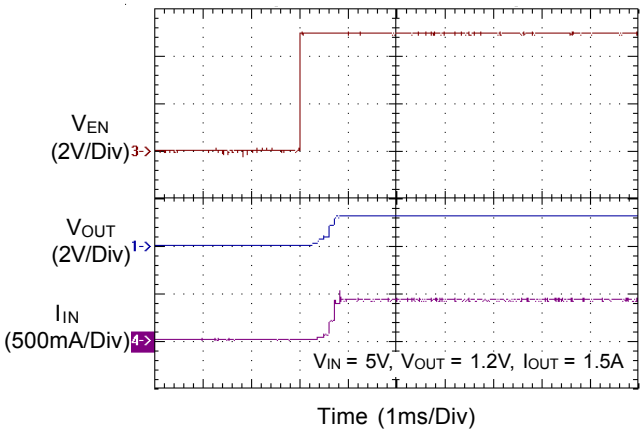
Regulator 2 Ripple



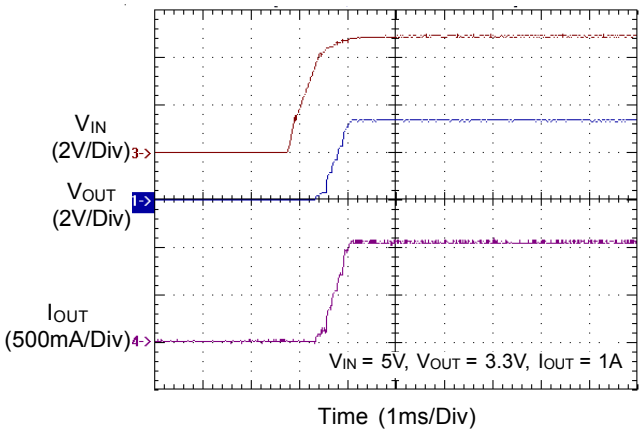
Regulator 1 Power On from EN



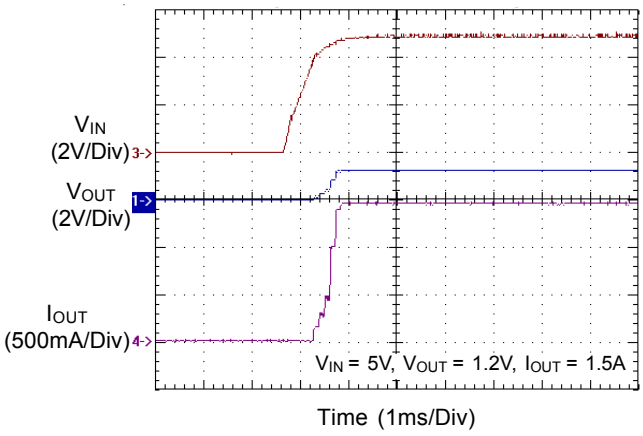
Regulator 2 Power On from EN



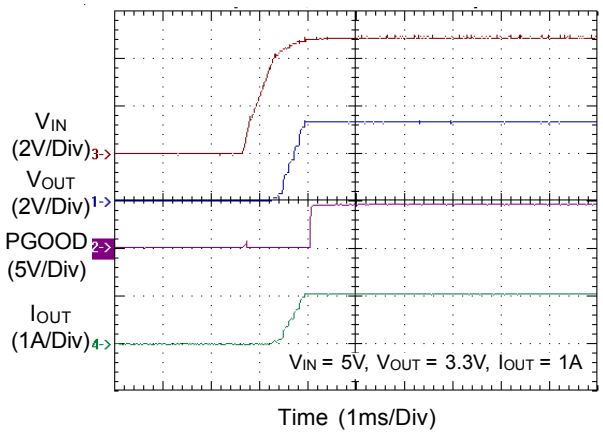
Regulator 1 Power On from V_{IN}



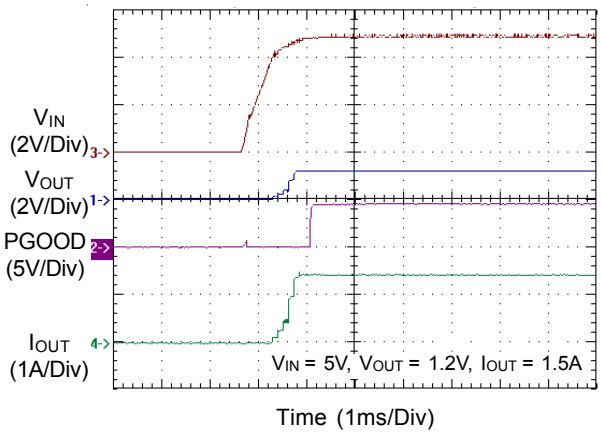
Regulator 2 Power On from V_{IN}



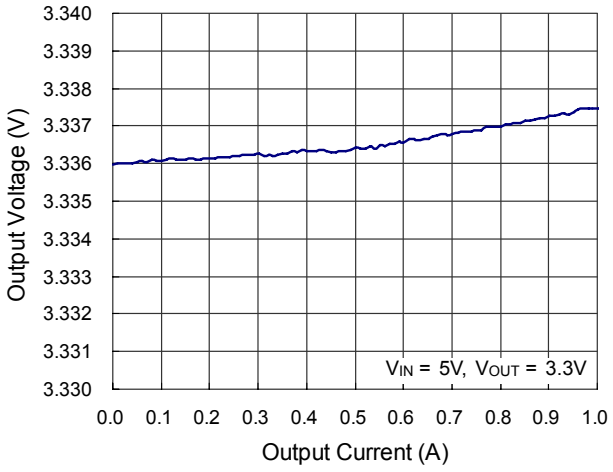
Regulator 1 Power Good Delay



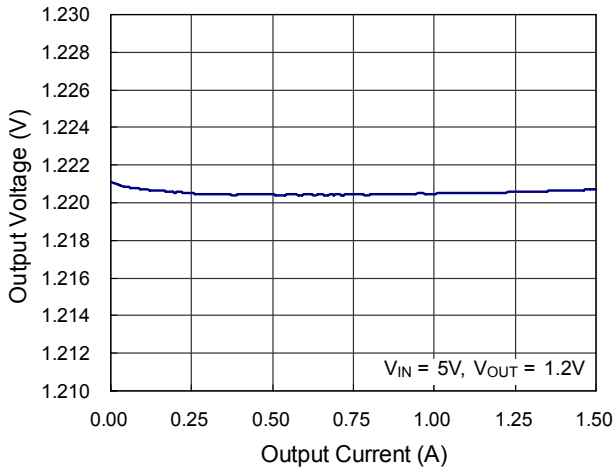
Regulator 2 Power Good Delay



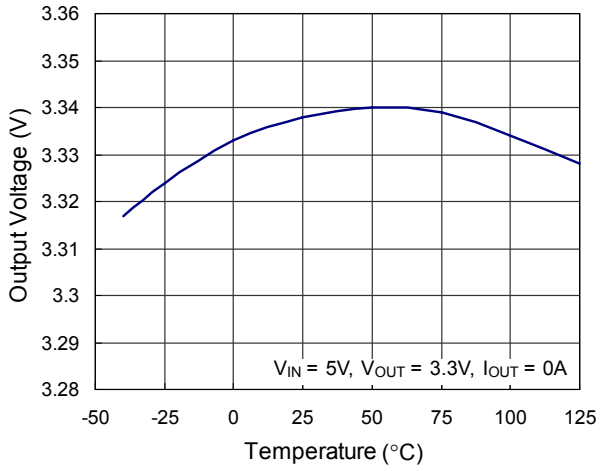
Regulator 1 Load Regulation



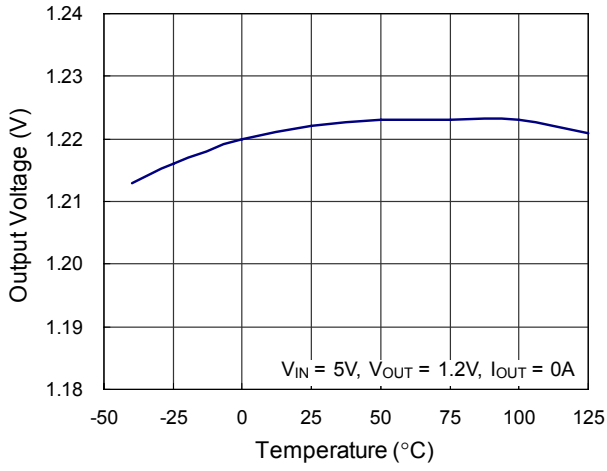
Regulator 2 Load Regulation



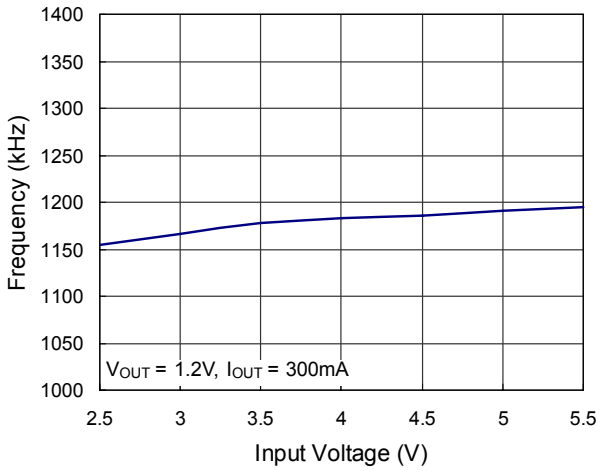
Regulator 1 Output Voltage vs. Temperature



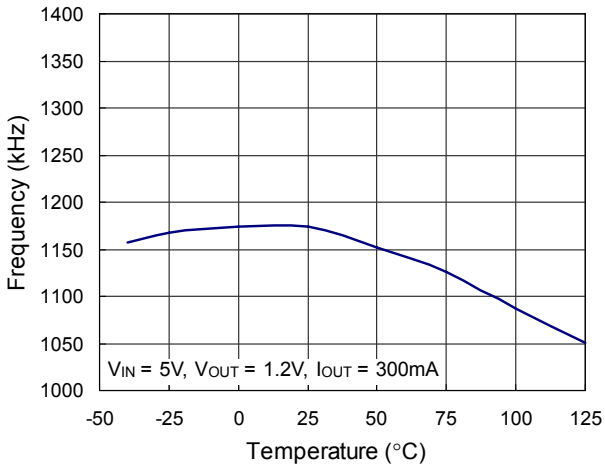
Regulator 2 Output Voltage vs. Temperature



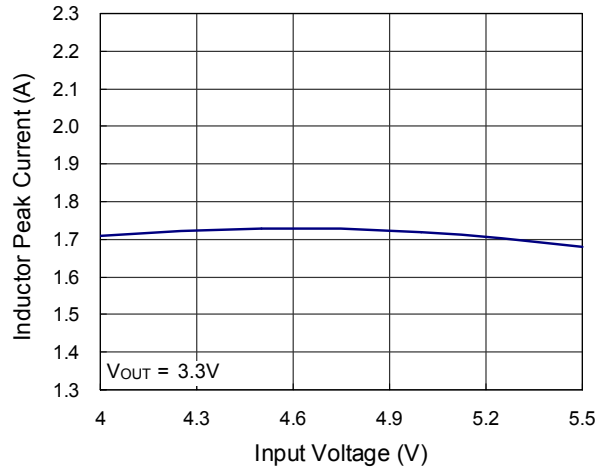
Switching Frequency vs. Input Voltage



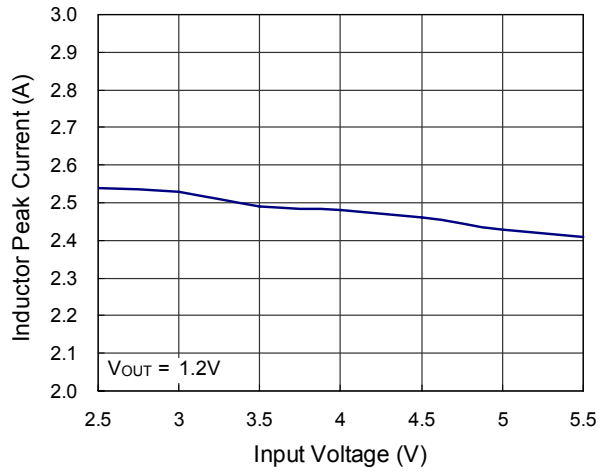
Switching Frequency vs. Temperature



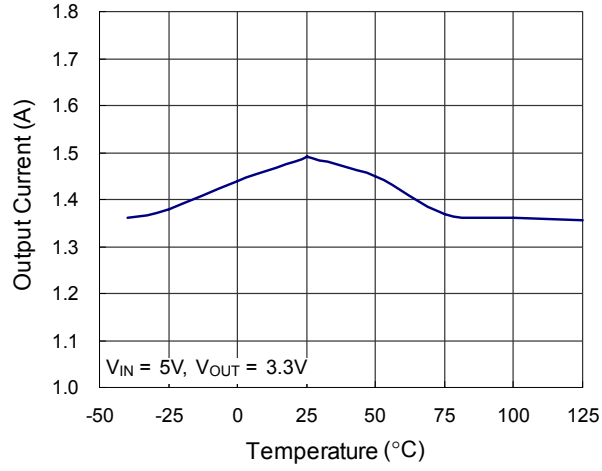
Regulator 1 Inductor Peak Current vs. Input Voltage



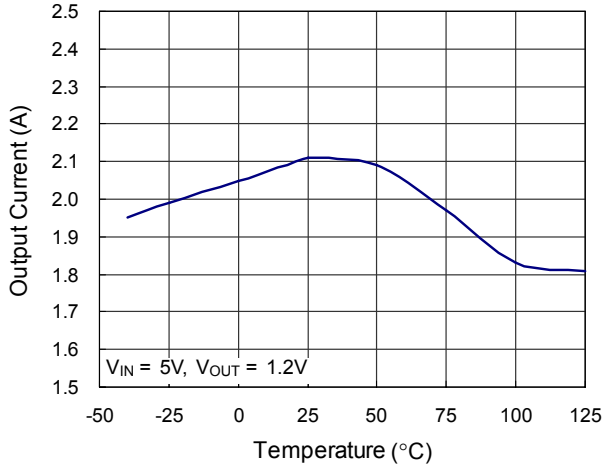
Regulator 2 Inductor Peak Current vs. Input Voltage



Regulator 1 Current Limit vs. Temperature



Regulator 2 Current Limit vs. Temperature



Applications Information

The basic RT8012A application circuit is shown in Typical Application Circuit. External component selection is determined by the maximum load current and begins with the selection of the inductor value and operating frequency followed by C_{IN} and C_{OUT}.

Inductor Selection

For a given input and output voltage, the inductor value and operating frequency determine the ripple current. The ripple current ΔI_L increases with higher V_{IN} and decreases with higher inductance.

$$\Delta I_L = \left[\frac{V_{OUT}}{f \times L}\right] \times \left[1 - \frac{V_{OUT}}{V_{IN}}\right]$$

Having a lower ripple current reduces the ESR losses in the output capacitors and the output voltage ripple. Highest efficiency operation is achieved at low frequency with small ripple current. This, however, requires a large inductor.

A reasonable starting point for selecting the ripple current is $\Delta I_L = 0.4(I_{MAX})$. The largest ripple current occurs at the highest V_{IN}. To guarantee that the ripple current stays below a specified maximum, the inductor value should be chosen according to the following equation :

$$L = \left[\frac{V_{OUT}}{f \times \Delta I_{L(MAX)}}\right] \times \left[1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right]$$

Inductor Core Selection

Once the value for L is known, the type of inductor must be selected. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite or mollypermalloy cores. Actual core loss is independent of core size for a fixed inductor value but it is very dependent on the inductance selected. As the inductance increases, core losses decrease. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core losses and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates "hard", which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

Different core materials and shapes will change the size/ current and price/current relationship of an inductor.

Toroid or shielded pot cores in ferrite or permalloy materials are small and don't radiate energy. However, they are usually more expensive than the similar powered iron inductors. The choice of which style inductor to use mainly depends on the price vs size requirements and any radiated field/EMI requirements.

C_{IN} and C_{OUT} Selection

The input capacitance, C_{IN}, is needed to filter the trapezoidal current at the source of the top MOSFET. To prevent large ripple voltage, a low ESR input capacitor sized for the maximum RMS current should be used. RMS current is given by :

$$I_{RMS} = I_{OUT(MAX)} \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life which makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design.

The selection of C_{OUT} is determined by the effective series resistance (ESR) that is required to minimize voltage ripple and load step transients, as well as the amount of bulk capacitance that is necessary to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response as described in a later section. The output ripple, ΔV_{OUT}, is determined by :

$$\Delta V_{OUT} \leq \Delta I_L \left[ESR + \frac{1}{8fC_{OUT}}\right]$$

The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Dry tantalum, special polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Special polymer capacitors offer very low ESR but have lower capacitance density than other types. Tantalum capacitors have the highest capacitance density but it is important to only use types that have been surge tested for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR but can be used in cost-sensitive applications provided that consideration is given to ripple current ratings and long term reliability. Ceramic capacitors have excellent low ESR characteristics but can have a high voltage coefficient and audible piezoelectric effects. The high Q of ceramic capacitors with trace inductance can also lead to significant ringing.

Selecting Ceramic Input and Output Capacitors

Higher values, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at the input and output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, V_{IN}. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN} large enough to damage the part.

Output Voltage Programming

The resistive divider allows the FB pin to sense a fraction of the output voltage as shown in Figure 3.

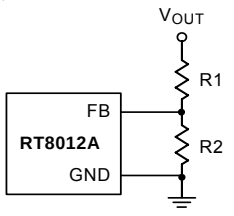


Figure 3. Setting the Output Voltage

For adjustable voltage mode, the output voltage is set by an external resistive divider according to the following equation :

$$V_{OUT} = V_{REF}(1+\frac{R1}{R2})$$

where V_{REF} is the internal reference voltage (0.8V typ.)

Efficiency Considerations

The efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Efficiency can be expressed as :

Efficiency = 100% – (L1+ L2+ L3+ ...)

where L1, L2, etc. are the individual losses as a percentage of input power. Although all dissipative elements in the circuit produce losses, two main sources usually account for most of the losses : VIN quiescent current and I^2R losses.

The VIN quiescent current loss dominates the efficiency loss at very low load currents whereas the I^2R loss dominates the efficiency loss at medium to high load currents. In a typical efficiency plot, the efficiency curve at very low load currents can be misleading since the actual power lost is of no consequence.

1. The VIN quiescent current appears due to two factors including the DC bias current as given in the electrical characteristics and the internal main switch and synchronous switch gate charge currents. The gate charge current results from switching the gate capacitance of the internal power MOSFET switches. Each time the gate is switched from high to low to high again, a packet of charge ΔQ moves from V_{IN} to ground.

The resulting $\Delta Q/\Delta t$ is the current out of V_{IN} that is typically larger than the DC bias current. In continuous mode,

$I_{GATECHG} = f(Q_T+Q_B)$

where Q_T and Q_B are the gate charges of the internal top and bottom switches. Both the DC bias and gate charge losses are proportional to V_{IN} and thus their effects will be more pronounced at higher supply voltages.

2. I^2R losses are calculated from the resistances of the internal switches, R_{SW} and external inductor R_L.In continuous mode, the average output current flowing

through inductor L is "chopped" between the main switch and the synchronous switch. Thus, the series resistance looking into the LX pin is a function of both top and bottom MOSFET $R_{DS(ON)}$ and the duty cycle (DC) as follows :

$R_{SW} = R_{DS(ON)TOP} \times DC + R_{DS(ON)BOT} \times (1-DC)$

The $R_{DS(ON)}$ for both the top and bottom MOSFETs can be obtained from the Typical Performance Characteristics curves. Thus, to obtain I^2R losses, simply add R_{SW} to R_L and multiply the result by the square of the average output current.

Other losses including C_{IN} and C_{OUT} ESR dissipative losses and inductor core losses generally account for less than 2% of the total loss.

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to ΔI_{LOAD} (ESR), where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value. During this recovery time, V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem.

Thermal Considerations

For continuous operation, do not exceed the maximum operation junction temperature 125°C. The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature differential between junction to ambient. The maximum power dissipation can be calculated by following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

Where $T_{J(MAX)}$ is the maximum operation junction temperature 125°C, T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance.

For recommended operating conditions specification of RT8012A, where $T_{J(MAX)}$ is the maximum junction temperature of the die (125°C) and T_A is the maximum ambient temperature. The junction to ambient thermal resistance θ_{JA} is layout dependent. For WQFN-16L 4x4 packages, the thermal resistance θ_{JA} is 54°C/W on the standard JEDEC 51-7 four-layers thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / 54°C/W = 1.852W for WQFN-16L 4x4 packages

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance θ_{JA}. For RT8012A packages, the Figure 4 of derating curves allows the designer to see the effect of rising ambient temperature on the maximum power allowed.

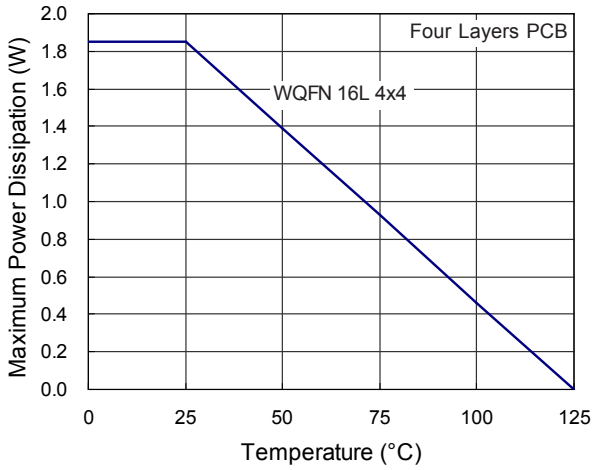


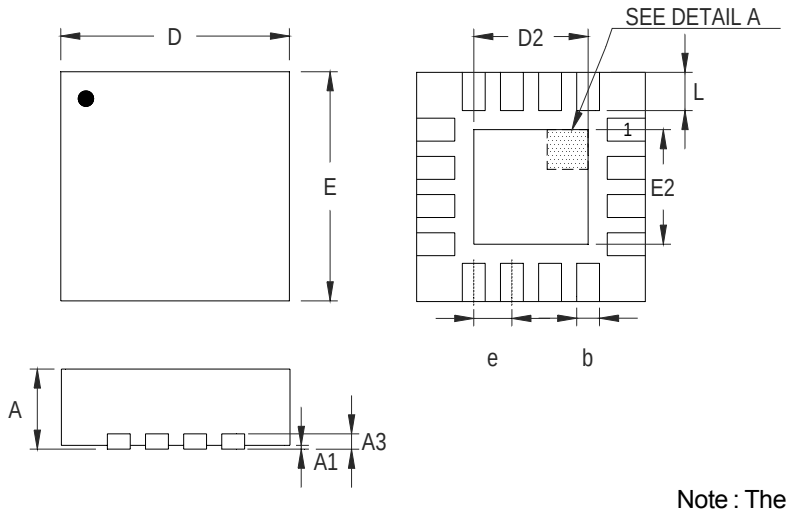
Figure 4. Derating Curves for RT8012A Packages

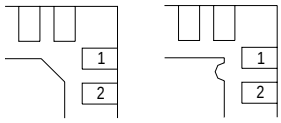
Layout Considerations

Follow the PCB layout guidelines for optimal performance of RT8012A.

- Keep the traces of the main current paths as short and wide as possible.
- Put the input capacitor as close as possible to the device pins (VIN and GND).
- LX node is with high frequency voltage swing and should be kept small area. Keep analog components away from LX node to prevent stray capacitive noise pick-up.
- Connect feedback network behind the output capacitors. Keep the loop area small. Place the feedback components near the RT8012A.
- Connect all analog grounds to a command node and then connect the command node to the power ground behind the output capacitors.

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.250	0.380	0.010	0.015
D	3.950	4.050	0.156	0.159
D2	2.000	2.450	0.079	0.096
E	3.950	4.050	0.156	0.159
E2	2.000	2.450	0.079	0.096
e	0.650		0.026	
L	0.500	0.600	0.020	0.024

W-Type 16L QFN 4x4 Package

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