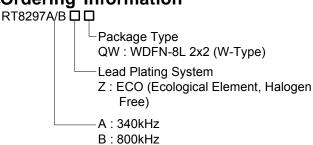


1.5A, 17V, 340/800kHz Synchronous Step-Down Converter

General Description

The RT8297A/B is a high efficiency, monolithic synchronous step-down DC/DC converter that can operate at 340 kHz/800 kHz, while delivering up to 1.5 A output current from a 4V to 17V input supply. The RT8297A/B's current mode architecture allows the transient response to be optimized. Cycle-by-cycle current limit provides protection against shorted outputs and soft-start eliminates input current surge during start-up. Fault conditions also include output under voltage protection, output over voltage protection, and thermal shutdown. The low current (<5µA) shutdown mode provides output disconnect, enabling easy power management in battery-powered systems. The RT8297A/B is available in a WDFN-8L 2x2 package.

Ordering Information

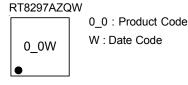


Note:

Richtek Green products are:

- ▶ RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- ▶ Suitable for use in SnPb or Pb-free soldering processes.

Marking Information



RT8297BZQW



7_1 : Product Code W : Date Code

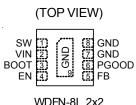
Features

- 4V to 17V Input Voltage Range
- 1.5A Output Current
- Internal N-MOSFETs
- Current Mode Control
- Fixed Frequency Operation: 340kHz/800kHz
- Output Adjustable from 0.8V to 12V
- Up to 95% Efficiency
- Internal Compensation
- Stable with Low ESR Ceramic Output Capacitors
- Cycle-by-Cycle Over Current Protection
- Input Under Voltage Lockout
- Output Under Voltage Protection
- Output Over Voltage Protection
- Power Good Indicator
- Thermal Shutdown Protection
- RoHS Compliant and Halogen Free

Applications

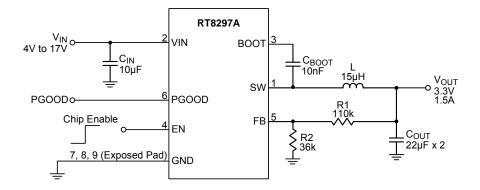
- Industrial and Commercial Low Power Systems
- Computer Peripherals
- LCD Monitors and TVs
- Green Electronics/Appliances
- Point of Load Regulation for High-Performance DSPs, FPGAs, and ASICs

Pin Configurations





Typical Application Circuit



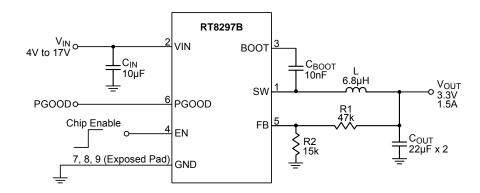


Table 1. Recommended Component Selection RT8297A

V _{OUT} (V)	L (μH)	R1 (kΩ)	R2 (kΩ)	C _{OUT} (μF)
1.2	4.7	110	220	22 x 2
2.5	10	110	51	22 x 2
3.3	15	110	36	22 x 2
5	22	120	22	22 x 2

RT8297B

V _{OUT} (V)	L (μH)	R1 (kΩ)	R2 (kΩ)	C _{OUT} (μF)
1.2	3.6	47	91	22 x 2
2.5	4.7	47	22	22 x 2
3.3	6.8	47	15	22 x 2
5	10	62	12	22 x 2

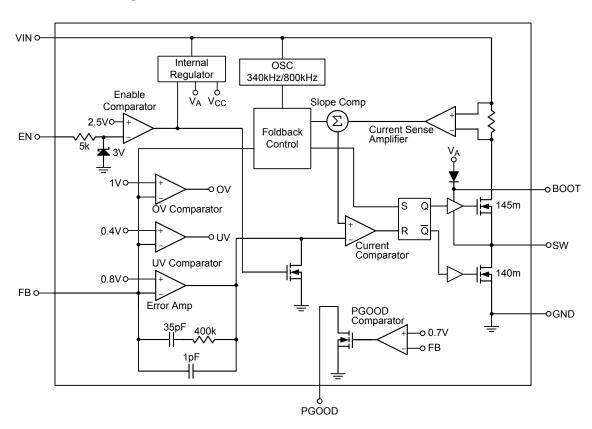
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Functional Pin Description

Pin No.	Pin Name	Pin Function		
1	SW	Switch Node. Connect to external L-C filter.		
2	VIN	Input Supply Voltage. Must bypass with a suitably large ceramic capacitor.		
3	воот	Bootstrap for High Side Gate Driver. Connect $0.01\mu F$ or greater ceramic capacitor from BOOT to SW pin.		
4	EN	Chip Enable. A logic-high enables the converter; a logic-low forces the RT8297A/B into shutdown mode, reducing the supply current to less than $5\mu A$. Attach this pin to VIN with a $100k\Omega$ pull up resistor for automatic startup.		
5	FB	Feedback Input Pin. For an adjustable output, connect an external resistive voltage divider to this pin.		
6	PGOOD	Power Good Indicator. The output of this pin is low if the output voltage is 12.5% less than the nominal voltage. Otherwise, it is an open drain.		
7, 8, 9 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.		

Function Block Diagram





Absolute Maximum Ratings (Note 1)

• Supply Voltage, V _{IN}	0.3V to 19V
• SW	$-0.3V$ to $(V_{IN} + 0.3V)$
• BOOT	- (SW - 0.3V) to $(SW + 0.3V)$
• All Other Pins	0.3V to 6V
 Power Dissipation, P_D @ T_A = 25°C 	
WDFN-8L 2x2	- 0.833W
Package Thermal Resistance (Note 2)	
WDFN-8L 2x2, θ_{JA}	- 120°C/W
WDFN-8L 2x2, θ_{JC}	
Lead Temperature (Soldering, 10 sec.)	- 260°C
Junction Temperature	
Storage Temperature Range	65°C to 150°C
ESD Susceptibility (Note 3)	
HBM (Human Body Mode)	2kV
MM (Machine Mode)	- 200V

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, V_{IN}------ 4V to 17V
- Junction Temperature Range ----- --- -40°C to 125°C
- Ambient Temperature Range ----- --- -40°C to 85°C

Electrical Characteristics

(V_{IN} = 12V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Тур	Max	Unit	
Shutdown Supply Current	I _{SHDN}	V _{EN} = 0V	-	1	5	μΑ	
Supply Current	I _{OUT}	V _{EN} = 3V, V _{FB} = 0.9V		0.6	1	mA	
Feedback Voltage	V _{FB}	$4V \le V_{IN} \le 17V$	0.788	0.8	0.812	V	
Feedback Current	I _{FB}	V _{FB} = 0.8V		10		nA	
High Side Switch On Resistance	R _{DS(ON)1}			145		mΩ	
Low Side Switch On Resistance	R _{DS(ON)2}			140	1	mΩ	
Upper Switch Current Limit		Min. Duty Cycle, V _{BOOT} –V _{SW} = 4.8V Maximum Loading = 1.5A	-	2.5	ı	Α	
Lower Switch Current Limit		From Drain to Source		1		Α	
Oscillation Fraguency	fosc1	For RT8297A	300	340	380	kHz	
Oscillation Frequency		For RT8297B	700	800	900		
Short-Circuit Oscillation	fosc2	V _{FB} = 0V, For RT8297A		95		kHz	
Frequency		V _{FB} = 0V, For RT8297B		170			
Maximum Duty Cyala	D _{MAX}	V _{FB} = 0.7V, For RT8297A		93		%	
Maximum Duty Cycle		V _{FB} = 0.7V, For RT8297B		84		%	

To be continued

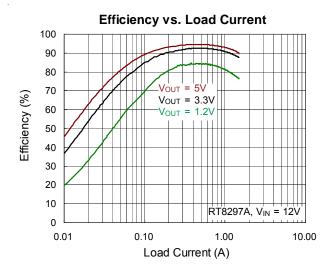


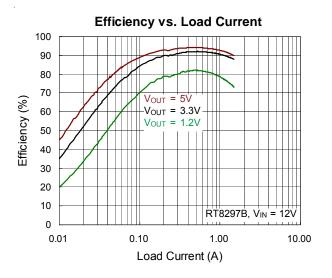
Parameter		Symbol	Test Conditions	Min	Тур	Max	Unit
Minimum On Time		t _{ON}			100		ns
Input Under Voltage Lockout Threshold		V _{UVLO}			3.5		V
Input Under Volta Threshold Hyster		ΔV _{UVLO}			320		mV
EN Threshold	Logic-High	V _{IH}		2.5			V
Voltage	Logic-Low	VIL				0.4	V
EN Pull Low Cur	EN Pull Low Current		V _{EN} = 2V, V _{FB} = 1V		1		μΑ
Soft-Start Period		t _{SS}			1		ms
Thermal Shutdown		T _{SD}			150		°C
Thermal Shutdov Hysteresis	vn	ΔT _{SD}			15		°C
Power Good Threshold Rising					0.7		V
Power Good Threshold Hysteresis					130		mV
Power Good Pull Down Resistance					12		Ω
Output OVP Trip	Threshold				125		%V _{REF}
Output OVP Prop	o Delay				10		μS

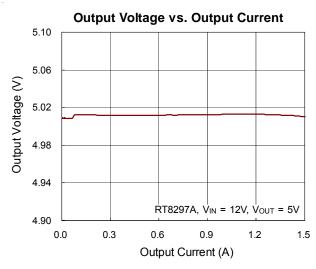
- **Note 1.** Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.
- Note 2. θ_{JA} is measured in natural convection at T_A = 25°C on a high effective thermal conductivity four-layer test board of JEDEC 51-7 thermal measurement standard. The measurement case position of θ_{JC} is on the exposed pad of the package.
- Note 3. Devices are ESD sensitive. Handling precaution is recommended.
- Note 4. The device is not guaranteed to function outside its operating conditions.

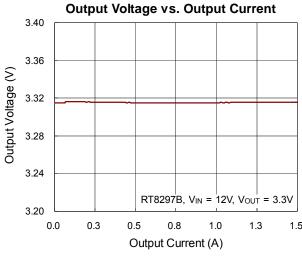


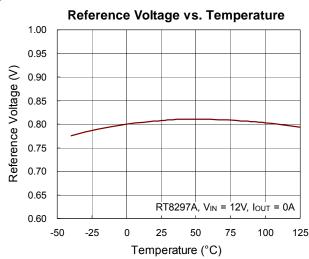
Typical Operating Characteristics

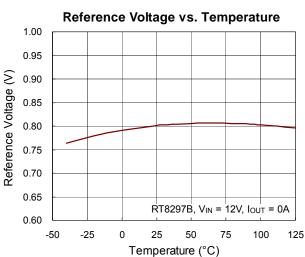


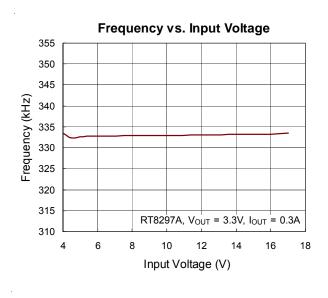


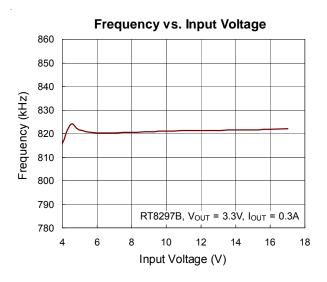


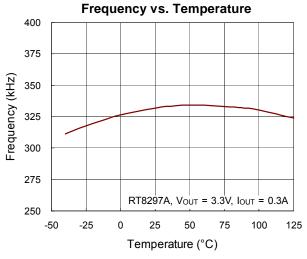


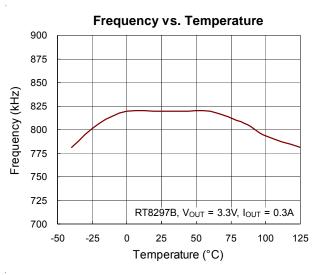


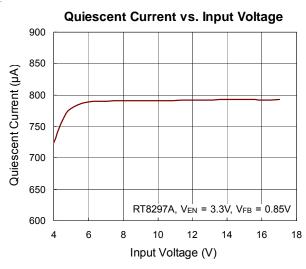


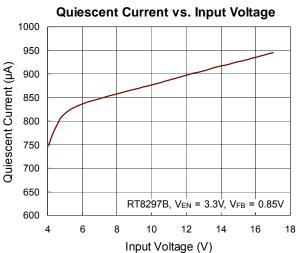






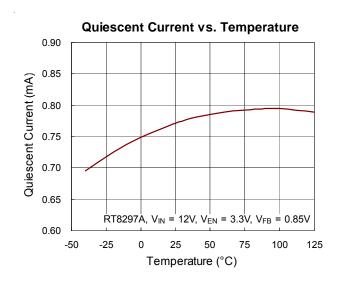


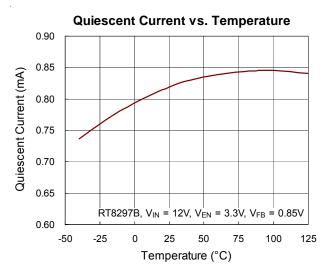


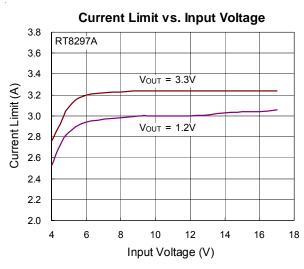


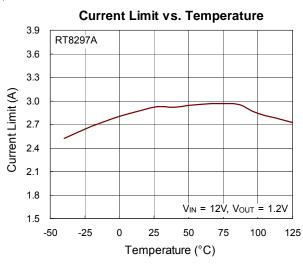
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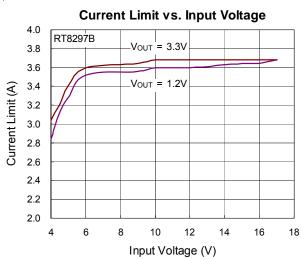


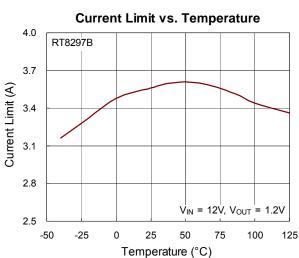


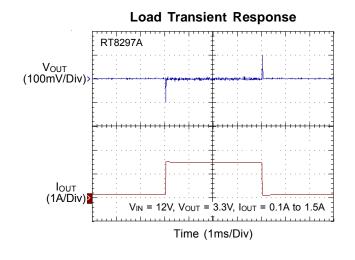


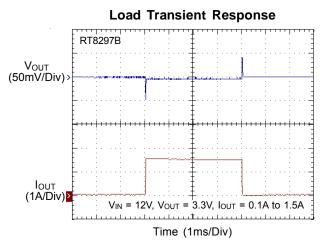


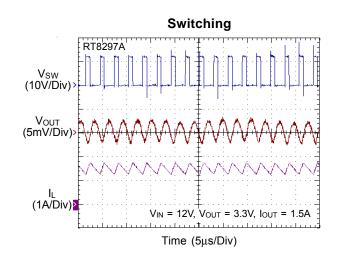


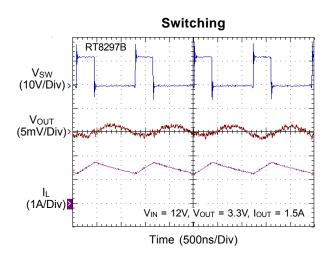


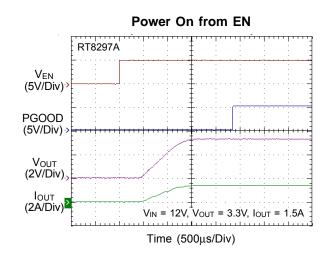


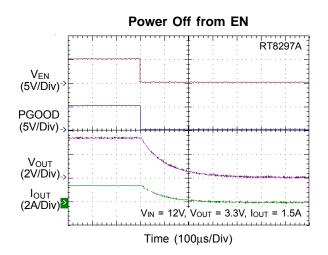


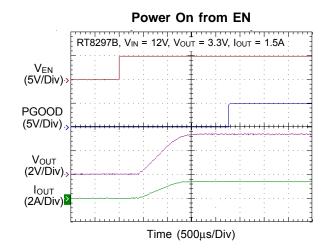


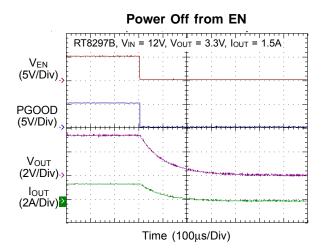














Application Information

The RT8297A/B is a synchronous high voltage buck converter that can support the input voltage range from 4V to 17V and the output current can be up to 1.5A.

Output Voltage Setting

The resistive divider allows the FB pin to sense the output voltage as shown in Figure 1.

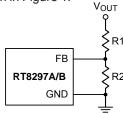


Figure 1. Output Voltage Setting

The output voltage is set by an external resistive divider according to the following equation:

$$V_{OUT} = V_{FB} \left(1 + \frac{R1}{R2} \right)$$

Where V_{FB} is the feedback reference voltage (0.8V typ.).

External Bootstrap Diode

Connect a 10nF low ESR ceramic capacitor between the BOOT pin and SW pin. This capacitor provides the gate driver voltage for the high side MOSFET. It is recommended to add an external bootstrap diode between an external 5V and the BOOT pin for efficiency improvement when input voltage is lower than 5.5V or duty ratio is higher than 65%. The bootstrap diode can be a low cost one such as 1N4148 or BAT54. The external 5V can be a 5V fixed input from system or a 5V output of the RT8297A/B. Note that the external boot voltage must be lower than 5.5V

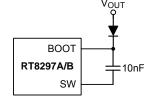


Figure 2. External Bootstrap Diode

Over Voltage Protection (OVP)

The RT8297A/B provides Over Voltage Protection function when output voltage over 125%. The internal MOS will be turned off. The control will return to normal operation if over voltage condition is removed.

Under Voltage Protection (UVP)

Latch-Off Mode

For the RT8297A/B, it provides Hiccup Mode Under Voltage Protection (UVP). When the FB voltage drops below 50% of the feedback reference voltage, V_{FB}, the UVP function will be triggered and the RT8297A/B will shut down for a period of time and then recover automatically. The Hiccup Mode UVP can reduce input current in short-circuit conditions.

Inductor Selection

The inductor value and operating frequency determine the ripple current according to a specific input and output voltage. The ripple current ΔI_L increases with higher V_{IN} and decreases with higher inductance.

$$\Delta I_{L} = \left[\frac{V_{OUT}}{f \times L} \right] \left[1 - \frac{V_{OUT}}{V_{IN}} \right]$$

Having a lower ripple current reduces not only the ESR losses in the output capacitors but also the output voltage ripple. High frequency with small ripple current can achieve highest efficiency operation. However, it requires a large inductor to achieve this goal. For the ripple current selection, the value of $\Delta I_L = 0.2 (I_{MAX})$ will be a reasonable starting point. The largest ripple current occurs at the highest V_{IN} . To guarantee that the ripple current stays below the specified maximum, the inductor value should be chosen according to the following equation :

$$L = \left[\frac{V_{OUT}}{f \times \Delta I_{L(MAX)}} \right] \left[1 - \frac{V_{OUT}}{V_{IN(MAX)}} \right]$$

Table 2. Suggested Inductors for Typical Application Circuit

Component Supplier	Series	Dimensions (mm)
TDK	VLF10045	10 x 9.7 x 4.5
TDK	SLF12565	12.5 x 12.5 x 6.5
TAIYO YUDEN	NR8040	8 x 8 x 4



CIN and COUT Selection

The input capacitance, C_{IN} , is needed to filter the trapezoidal current at the source of the high side MOSFET. To prevent large ripple current, a low ESR input capacitor sized for the maximum RMS current should be used. The RMS current is given by :

$$I_{RMS} = I_{OUT(MAX)} \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}}} - 1$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} =$ I_{OUT}/2. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design. For the input capacitor, a 10µF low ESR ceramic capacitor is recommended. For the recommended capacitor, please refer to table 3 for more detail. The selection of C_{OUT} is determined by the required ESR to minimize voltage ripple. Moreover, the amount of bulk capacitance is also a key for Cout selection to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response as described in a later section. The output ripple, ΔV_{OUT} , is determined by:

$$\Delta V_{OUT} \le \Delta I_{L} \left[ESR + \frac{1}{8fC_{OUT}} \right]$$

The output ripple will be highest at the maximum input voltage since ΔI_{\perp} increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirement. Dry tantalum, special polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Special polymer capacitors offer very low ESR value. However, it provides lower capacitance density than other types. Although Tantalum capacitors have the highest capacitance density, it is important to only use types that pass the surge test for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR. However, it can be used in cost-sensitive applications for ripple current rating and long term reliability considerations. Ceramic capacitors have excellent low ESR characteristics but can have a high voltage coefficient and audible piezoelectric effects. The high Q of ceramic

capacitors with trace inductance can also lead to significant ringing.

Higher values, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at input and output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, VIN. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at VIN large enough to damage the part.

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to ΔI_{LOAD} (ESR) also begins to charge or discharge C_{OUT} generating a feedback error signal for the regulator to return V_{OUT} to its steady-state value. During this recovery time, V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications of the RT8297A/B, the maximum junction temperature is 125° C and T_{A} is the ambient temperature. The junction to ambient thermal resistance, θ_{JA} , is layout dependent. For

WDFN-8L 2x2 packages, the thermal resistance, θ_{JA} , is 120°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

 $P_{D(MAX)} = (125^{\circ}C - 25^{\circ}C) / (120^{\circ}C/W) = 0.833W$ for WDFN-8L 2x2 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA} . For the RT8297A/B package, the derating curve in Figure 3 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

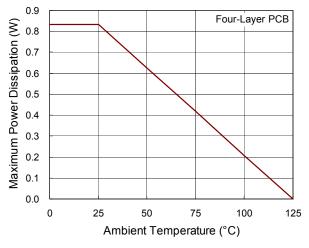


Figure 3. Derating Curve for the RT8297A/B Package

Layout Consideration

Follow the PCB layout guidelines for optimal performance of the RT8297A/B

- Keep the traces of the main current paths as short and wide as possible.
- Put the input capacitor as close as possible to the device pins (VIN and GND).
- LX node is with high frequency voltage swing and should be kept at small area. Keep sensitive components away from the LX node to prevent stray capacitive noise pickup.
- Place the feedback components to the FB pin as close as possible.
- The GND and Exposed Pad should be connected to a strong ground plane for heat sinking and noise protection.

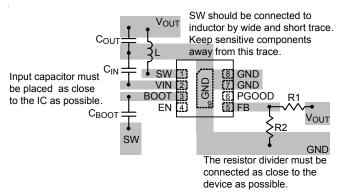
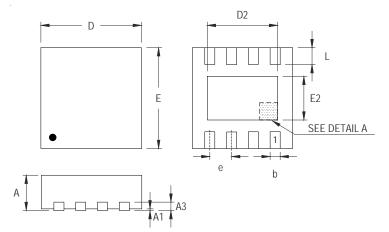


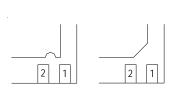
Figure 4. PCB Layout Guide

13



Outline Dimension





DETAIL APin #1 ID and Tie Bar Mark Options

Note: The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions	In Millimeters	Dimensions In Inches		
Symbol	Min	Max	Min	Max	
Α	0.700	0.800	0.028	0.031	
A1	0.000	0.050	0.000	0.002	
A3	0.175	0.250	0.007	0.010	
b	0.200	0.300	0.008	0.012	
D	1.950	2.050	0.077	0.081	
D2	1.000	1.250	0.039	0.049	
Е	1.950	2.050	0.077	0.081	
E2	0.400	0.650	0.016	0.026	
е	0.500		0.0)20	
L	0.300	0.400	0.012	0.016	

W-Type 8L DFN 2x2 Package

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