3A, 21V 500kHz Synchronous Step-Down Converter

General Description

The RT8287 is a synchronous step-down regulator with an internal power MOSFET. It achieves 3A of continuous output current over a wide input supply range with excellent load and line regulation. Current mode operation provides fast transient response and eases loop stabilization.

Fault condition protection includes cycle-by-cycle current limiting and thermal shutdown. An adjustable soft-start reduces the stress on the input source at startup.

The RT8287 requires a minimal number of readily available external components, providing a compact solution.

Ordering Information

RT8287 □□

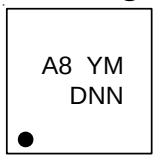
- Package Type
  QW : WDFN-14L 4x3 (W-Type)
- Lead Plating System
  Z : ECO (Ecological Element with Halogen Free and Pb free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Marking Information



A8 : Product Code

YMDNN : Date Code

Features

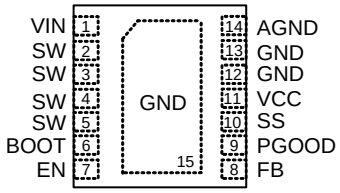
- **3A Output Current**
- **Adjustable Soft-Start**
- **120mΩ/40mΩ Internal Power MOSFET Switch**
- **Internal Compensation Minimizes External Parts Count**
- **Fixed 500kHz Frequency**
- **Thermal Shutdown Protection**
- **Cycle-by-Cycle Over Current Protection**
- **Wide 4.5V to 21V Operating Input Range**
- **Adjustable Output from 0.808V to 15V**
- **Small 14-Lead WDFN Package**
- **RoHS Compliant and Halogen Free**

Applications

- Distributive Power Systems
- Battery Charger
- DSL Modems
- Pre-Regulator for Linear Regulators

Pin Configurations

(TOP VIEW)



WDFN-14L 4x3

Typical Application Circuit

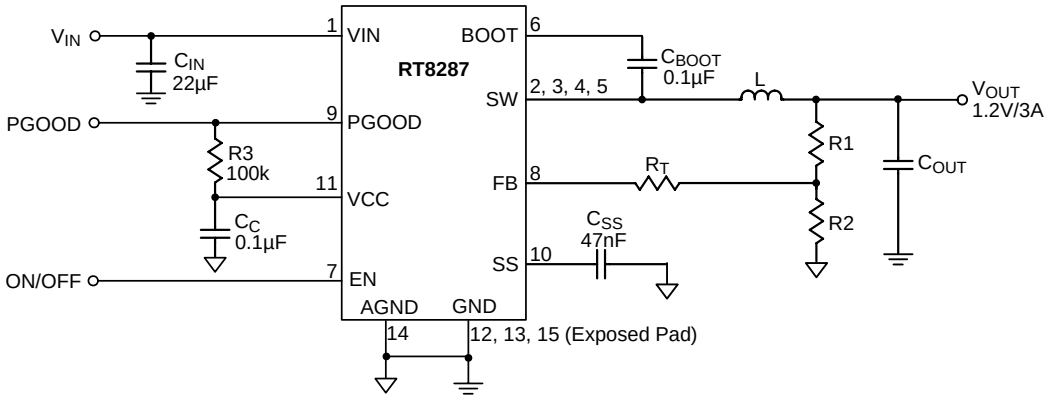


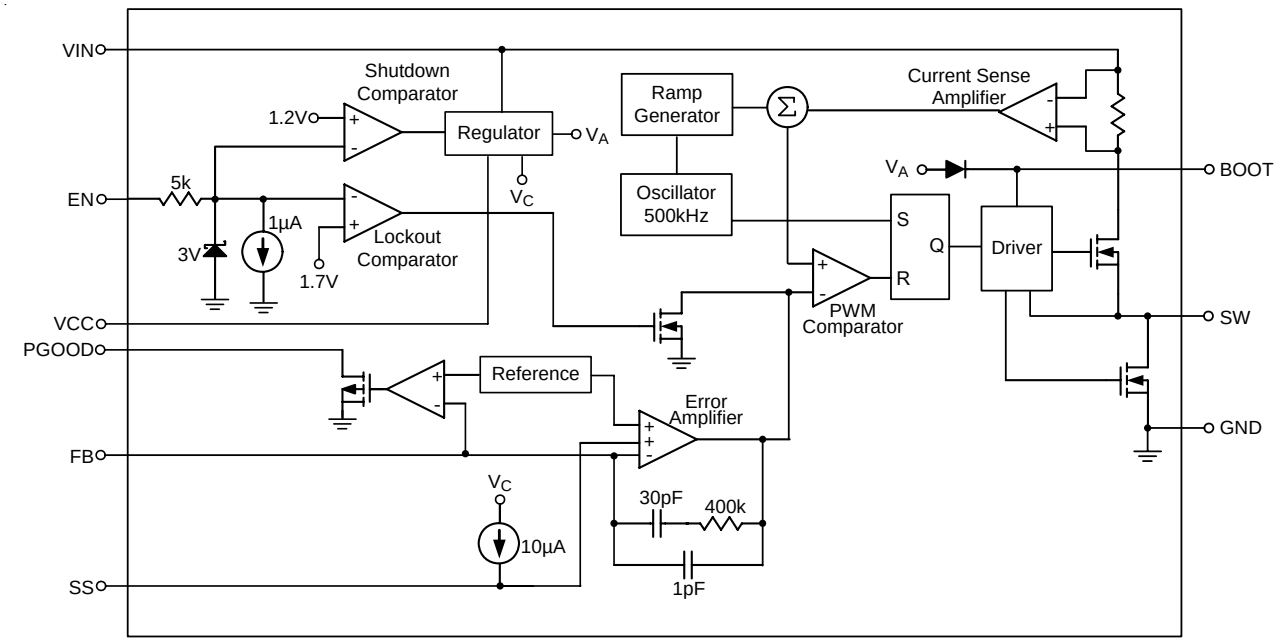
Table 1. Recommended Components Selection

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	R_T (kΩ)	L (µH)	C_{OUT} (µF)
5	75	14.46	0	4.7	22 x 2
3.3	75	24.32	0	3.6	22 x 2
2.5	75	35.82	0	3.6	22 x 2
1.8	5	4.07	30	2	22 x 2
1.5	5	5.84	39	2	22 x 2
1.2	5	10.31	47	2	22 x 2
1.05	5	16.69	47	1.5	22 x 2

Function Pin Description

Pin No.	Pin Name	Pin Function
1	VIN	Supply Input. VIN supplies the power to the IC, as well as the step-down converter switches. Drive VIN with a 4.5V to 21V power source. Bypass VIN to GND with a suitably large capacitor to eliminate noise on the input to the IC.
2, 3, 4, 5	SW	Switch Node. SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load. Note that a capacitor is required from SW to BOOT to power the high side switch.
6	BOOT	High Side Gate Drive Boost Input. BOOT supplies the drive for the high side N-MOSFET switch. Connect a 100nF or greater capacitor from SW to BOOT to power the high side switch.
7	EN	Chip Enable (Active High). For automatic start-up, connect the EN pin to VIN with a 100kΩ resistor.
8	FB	Feedback Input. FB senses the output voltage to regulate said voltage. Drive FB with a resistive voltage divider from the output voltage. The feedback threshold is 0.808V.
9	PGOOD	Power Good Output. The output of this pin is open-drain. Power good threshold is 90% low to high and 70% high to low of regulation value.
10	SS	Soft-Start Control Input. SS controls the soft-start period. Connect a capacitor from SS to GND to set the soft-start period.
11	VCC	Bias Supply. Decouple with 0.1µF to 0.22µF capacitor. The capacitance should be no more than 0.22µF.
12, 13 15 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
14	AGND	Analog Ground. Connect this pin to the system ground in PCB layout.

Function Block Diagram



Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, V_{IN} ---------- –0.3V to 26V
- Switch Voltage, SW ---------- –0.3V to (V_{IN} + 0.3V)
- Boot Voltage, BOOT ---------- (SW – 0.3V) to (SW + 6V)
- All Other Pins ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  WDFN-14L 4x3 ---------- 1.667W
- Package Thermal Resistance (Note 2)
  WDFN-14L 4x3, θ_{JA} ---------- 60°C/W
  WDFN-14L 4x3, θ_{JC} ---------- 7°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM ---------- 2kV
  MM ---------- 200V

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, V_{IN} ---------- 4.5V to 21V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{IN} = 12V, T_A = 25°C unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Shutdown Current		I_{SHDN}	V_{EN} = 0	--	0	1	μA
Quiescent Current		I_Q	V_{EN} = 2V, V_{FB} = 1V	--	0.7	--	mA
Upper Switch On Resistance		$R_{DS(ON)1}$		--	120	--	mΩ
Lower Switch On Resistance		$R_{DS(ON)2}$		--	40	--	mΩ
Switch Leakage		I_{LEAK}	V_{EN} = 0V, V_{SW} = 0V or 12V	--	0	10	μA
Current Limit		I_{LIMIT}	$V_{BOOT} - V_{SW}$ = 4.8V	5.4	6.5	--	A
Oscillator Frequency		f_{SW}	V_{FB} = 0.75V	425	500	575	kHz
Short Circuit Frequency			V_{FB} = 0V	--	150	--	kHz
Maximum Duty Cycle		D_{MAX}	V_{FB} = 0.8V	--	90	--	%
Minimum On Time		t_{ON}		--	100	--	ns
Feedback Voltage		V_{FB}	4.5V ≤ V_{IN} ≤ 21V	0.796	0.808	0.82	V
Feedback Current		I_{FB}		--	10	50	nA
EN Threshold Voltage	Logic-High	V_{IH}		2	--	5.5	V
	Logic-Low	V_{IL}		--	--	0.4	
Enable Current			V_{EN} = 2V	--	1	--	μA
			V_{EN} = 0V	--	0	--	

To be continued

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Good Rising Threshold			--	90	--	%
Power Good Falling Threshold			--	70	--	%
Power Good Delay			--	20	--	μs
Power Good Sink Current Capability		Sink 4mA	--	--	0.4	V
Power Good Leakage Current			--	10	--	nA
Under Voltage Lockout Threshold	V_{UVLO}	V_{IN} Rising	3.8	4	4.2	V
Under Voltage Lockout Threshold Hysteresis	ΔV_{UVLO}		--	400	--	mV
VCC Regulator			--	5	--	V
VCC Load Regulation		I_{CC} = 5mA	--	5	--	%
Soft-Start Period	t_{SS}	C_{SS} = 47nF	--	4.7	--	ms
Thermal Shutdown	T_{SD}		--	150	--	°C

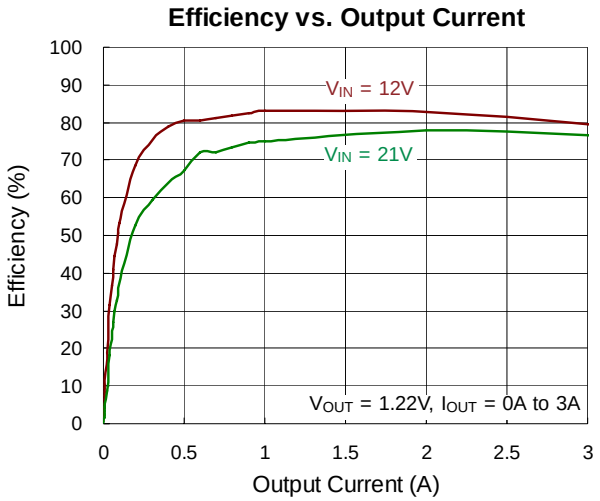
Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

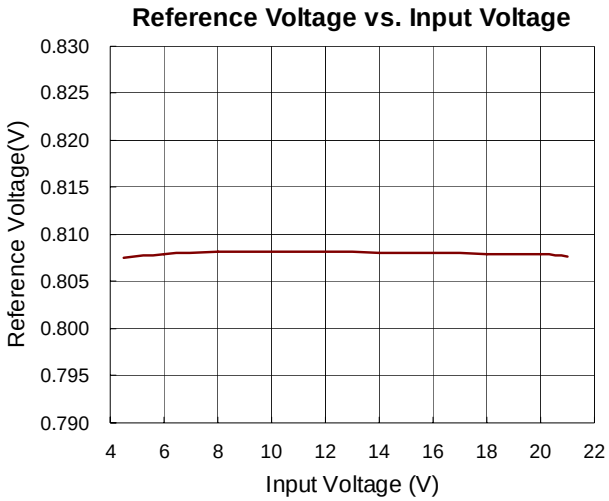
Note 2. θ_{JA} is measured in natural convection at T_A = 25°C on a high-effective thermal conductivity four-layer test board of JEDEC 51-7 thermal measurement standard. The measurement case position of θ_{JC} is on the exposed pad of the package.

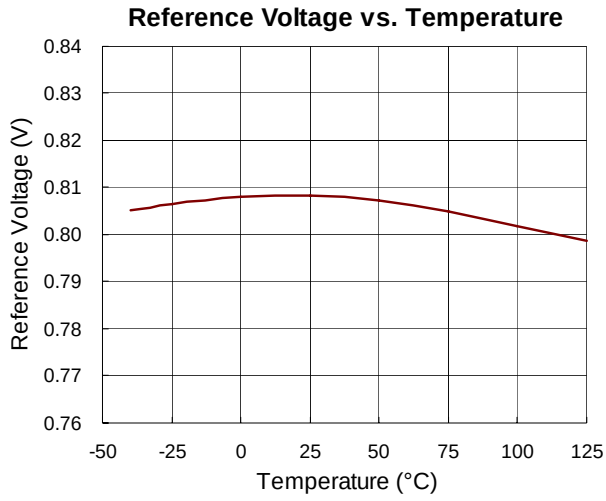
Note 3. Devices are ESD sensitive. Handling precaution is recommended.

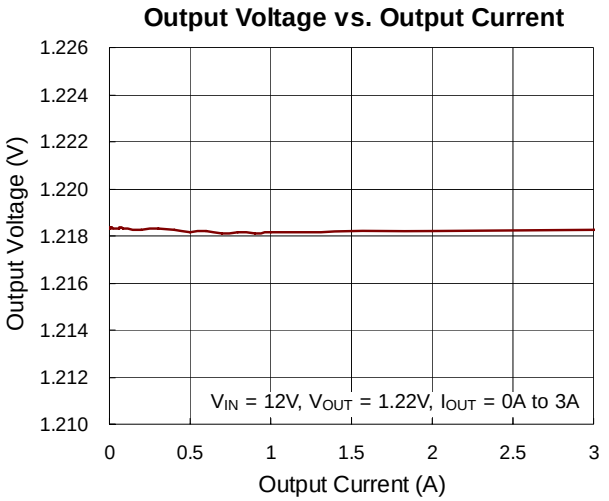
Note 4. The device is not guaranteed to function outside its operating conditions.

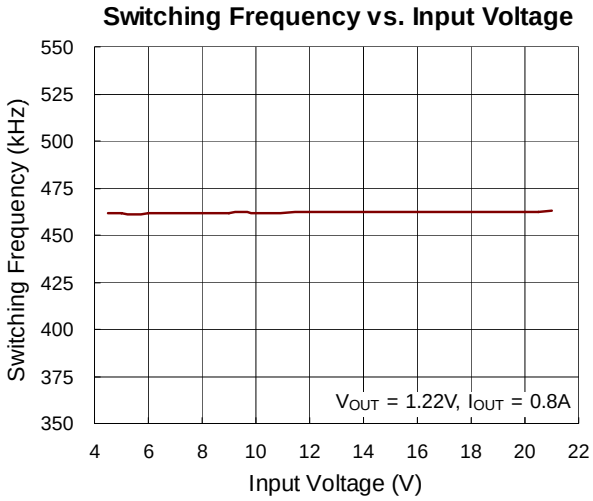
Typical Operating Characteristics

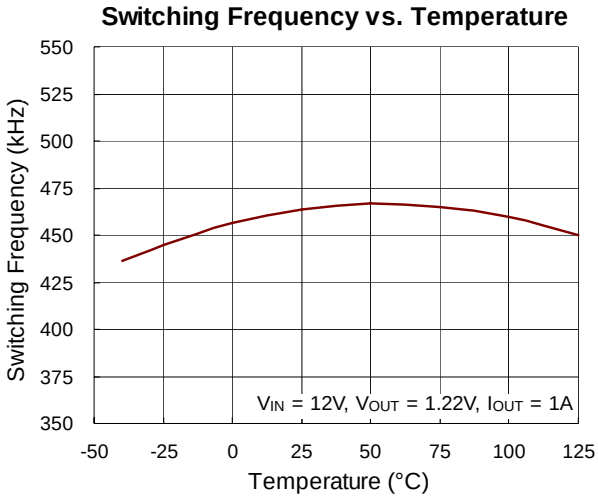




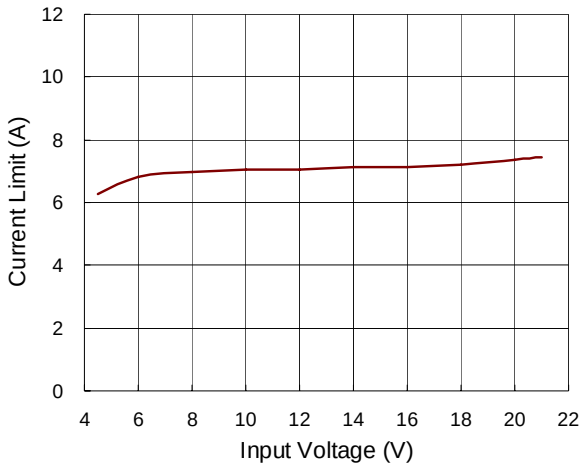




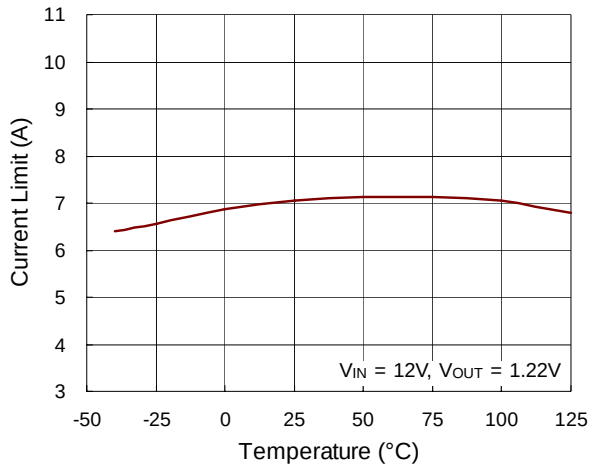




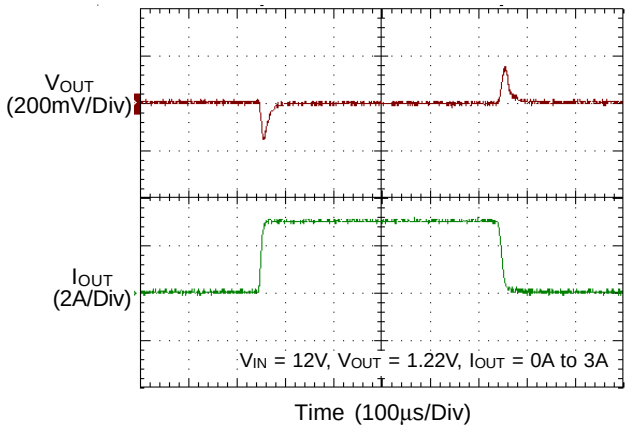
Current Limit vs. Input Voltage



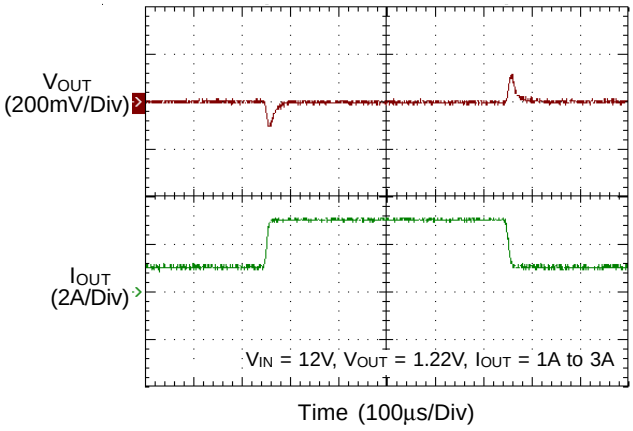
Current Limit vs. Temperature



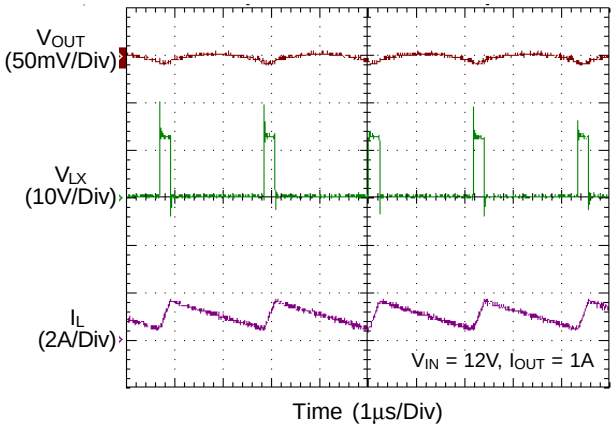
Load Transient Response



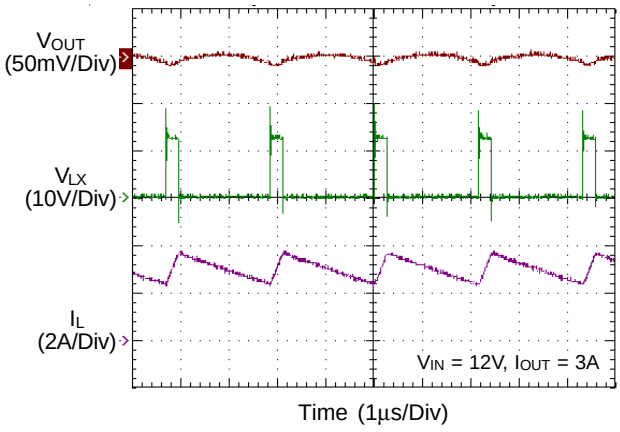
Load Transient Response



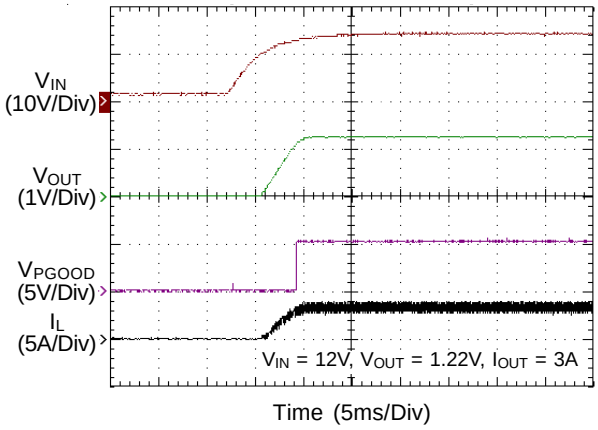
Output Voltage Ripple



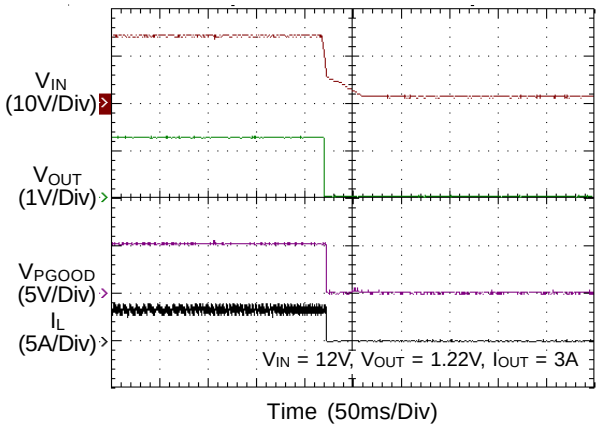
Output Voltage Ripple



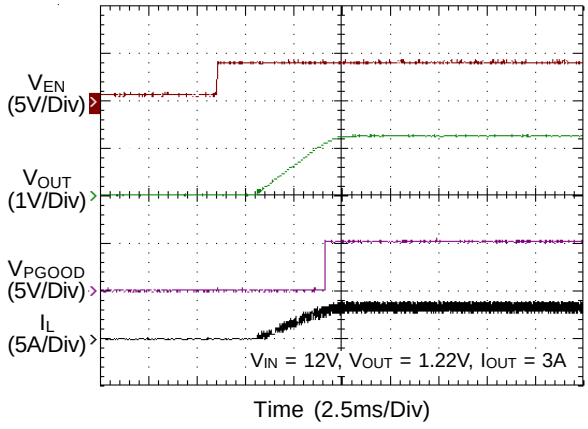
Power On from V_{IN}



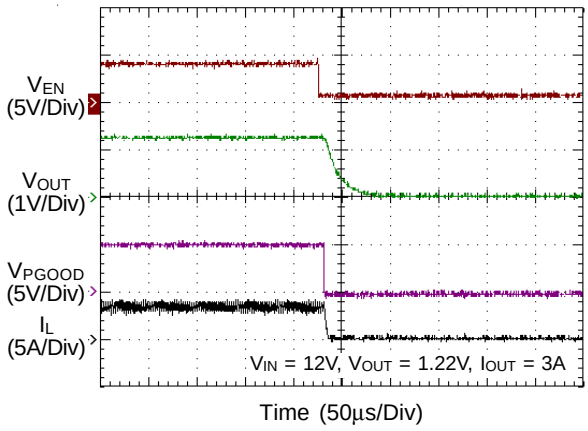
Power Off from V_{IN}



Power On from EN



Power Off from EN



Application Information

The IC is a synchronous high voltage buck converter that can support the input voltage range from 4.5V to 21V and the output current can be up to 3A.

Output Voltage Setting

The output voltage is set by an external resistive divider according to the following equation :

$$V_{OUT} = V_{FB}\left(1+\frac{R1}{R2}\right)$$

where V_{FB} is the feedback reference voltage 0.808V (typ.).

The resistive divider allows the FB pin to sense a fraction of the output voltage as shown in Figure 1.

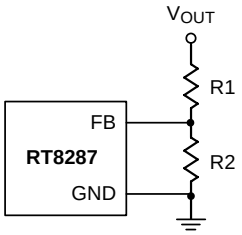


Figure 1. Output Voltage Setting

External Bootstrap Diode

Connect a 100nF low ESR ceramic capacitor between the BOOT pin and SW pin as shown in Figure 2. This capacitor provides the gate driver voltage for the high side MOSFET. It is recommended to add an external bootstrap diode between an external 5V and BOOT pin for efficiency improvement when input voltage is lower than 5.5V or duty ratio is higher than 65% .The bootstrap diode can be a low cost one such as IN4148 or BAT54. The external 5V can be a 5V fixed input from system or a 5V output of the IC. Note that the external boot voltage must be lower than 5.5V.

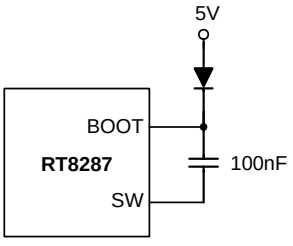


Figure 2. External Bootstrap Diode

Soft-Start

The IC contains an external soft-start clamp that gradually raises the output voltage. The soft-start timing is programmed by the external capacitor between SS pin and GND. The chip provides an internal 10μA charge current for the external capacitor. If 47nF capacitor is used to set the soft-start, the period will be 4.7ms (typ.).

Under Voltage Lockout Threshold

The IC includes an input Under Voltage Lockout Protection (UVLO). If the input voltage exceeds the UVLO rising threshold voltage (4.2V), the converter resets and prepares the PWM for operation. If the input voltage falls below the UVLO falling threshold voltage (3.8V) during normal operation, the device stops switching. The UVLO rising and falling threshold voltage includes a hysteresis to prevent noise caused reset.

Chip Enable Operation

The EN pin is the chip enable input. Pulling the EN pin low (<0.4V) will shut down the device. During shutdown mode, the IC quiescent current drops to lower than 1μA. Driving the EN pin high (>2V, < 5.5V) will turn on the device again. For external timing control (e.g.RC), the EN pin can also be externally pulled high by adding a R_{EN}* resistor and C_{EN}* capacitor from the VIN pin, as can be seen from the Figure 5.

An external MOSFET can be added to implement digital control on the EN pin when front age system voltage below 2.5V is available, as shown in Figure 3. In this case, a 100kΩ pull-up resistor, R_{EN}, is connected between V_{IN} and the EN pin. MOSFET Q1 will be under logic control to pull down the EN pin.

To prevent enabling circuit when V_{IN} is smaller than the V_{OUT} target value, a resistive voltage divider can be placed between the input voltage and ground and connected to the EN pin to adjust IC lockout threshold, as shown in Figure 4. For example, if an 8V output voltage is regulated from a 12V input voltage, the resistor R_{EN2} can be selected to set input lockout threshold larger than 8V.

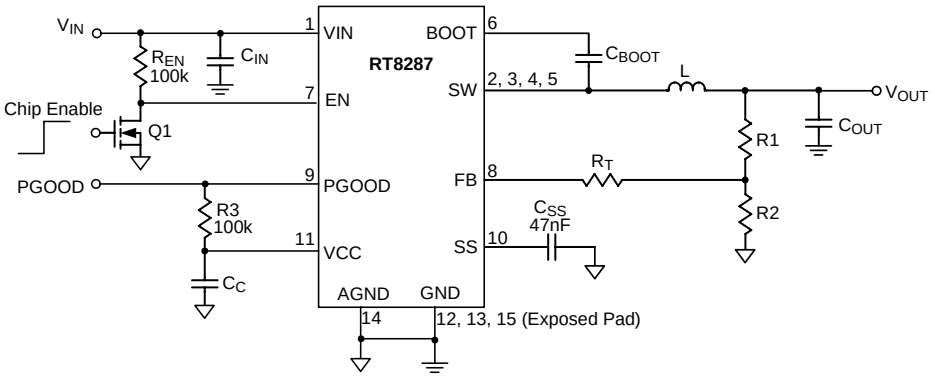


Figure 3. Enable Control Circuit for Logic Control with Low Voltage

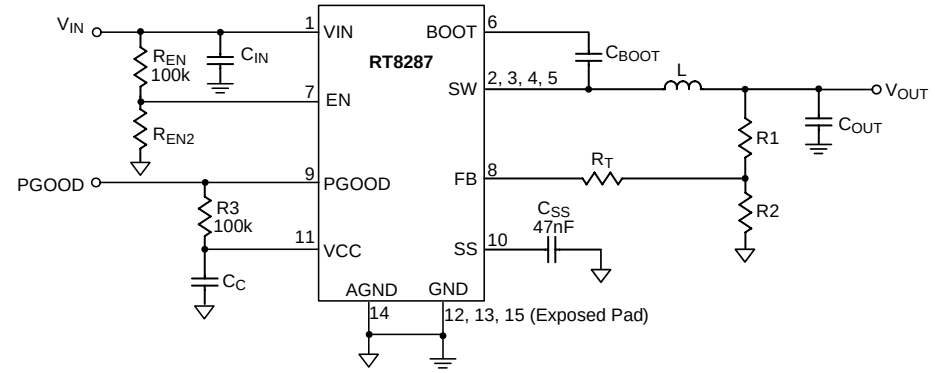


Figure 4. The Resistors can be Selected to Set IC Lockout Threshold

Power Good Output

The power good output is an open-drain output and requires a pull up resistor. When the output voltage is 70% below its set voltage, PGOOD will be pulled low. It is held low until the output voltage returns to within the allowed tolerances once more. During soft-start, PGOOD is actively held low and only allowed to transition high after soft-start is over and the output voltage has reached 90% of its set voltage.

Under Output Voltage Protection-Hiccup Mode

For the IC, Hiccup Mode of Under Voltage Protection (UVP) is provided. When the FB voltage drops below half of the feedback reference voltage, V_{FB}, the UVP function will be triggered and the IC will shut down for a period of time and then recover automatically. The Hiccup Mode of UVP can reduce input current in short-circuit conditions.

Inductor Selection

For a given input and output voltage, the inductor value and operating frequency determine the ripple current. The ripple current ΔI_L increases with higher V_{IN} and decreases with higher inductance.

$$\Delta I_L = \left[\frac{V_{OUT}}{f \times L}\right] \times \left[1 - \frac{V_{OUT}}{V_{IN}}\right]$$

Having a lower ripple current reduces not only the ESR losses in the output capacitors but also the output voltage ripple. Highest efficiency operation is achieved by reducing ripple current at low frequency, but it requires a large inductor to attain this goal.

For the ripple current selection, the value of $\Delta I_L = 0.24(I_{MAX})$ will be a reasonable starting point. The largest ripple current occurs at the highest V_{IN}. To guarantee that the ripple current stays below a specified maximum, the inductor value should be chosen according to the following equation :

$$L = \left[\frac{V_{OUT}}{f \times \Delta I_{L(MAX)}}\right] \times \left[1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right]$$

The inductor's current rating (caused a 40°C temperature rising from 25°C ambient) should be greater than the maximum load current and its saturation current should be greater than the short circuit peak current limit. Please see Table 2 for the inductor selection reference and it is highly recommended to keep inductor value as close as possible to the recommended inductor values for each V_{OUT} as shown in Table 1.

Table 2. Suggested Inductors for Typical Application Circuit

Component Supplier	Series	Dimensions (mm)
TDK	VLF10045	10 x 9.7 x 4.5
TDK	SLF12565	12.5 x 12.5 x 6.5
TAIYO YUDEN	NR8040	8 x 8 x 4

Input and Output Capacitors Selection

The input capacitance, C_{IN}, is needed to filter the trapezoidal current at the source of the high side MOSFET. To prevent large ripple current, a low ESR input capacitor sized for the maximum RMS current should be used. The RMS current is given by :

$$I_{RMS} = I_{OUT(MAX)} \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT} / 2$. This simple worst case condition is commonly used for design because even significant deviations do not offer much relief.

Choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design.

For the input capacitor, one 22µF low ESR ceramic capacitors are recommended. For the recommended capacitor, please refer to table 3 for more detail.

Table 3. Suggested Capacitors for C_{IN} and C_{OUT}

Location	Component Supplier	Part No.	Capacitance (µF)	Case Size
C_{IN}	**MURATA**	GRM32ER71C226M	22	1210
C_{IN}	**TDK**	C3225X5R1C226M	22	1210
C_{OUT}	**MURATA**	GRM31CR60J476M	47	1206
C_{OUT}	**TDK**	C3225X5R0J476M	47	1210
C_{OUT}	**MURATA**	GRM32ER71C226M	22	1210
C_{OUT}	**TDK**	C3225X5R1C226M	22	1210

The selection of C_{OUT} is determined by the required ESR to minimize voltage ripple.

Moreover, the amount of bulk capacitance is also a key for C_{OUT} selection to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response.

The output ripple, ΔV_{OUT}, is determined by :

$$\Delta V_{OUT} \leq \Delta I_L \left[ESR + \frac{1}{8fC_{OUT}} \right]$$

Higher values, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at input and output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, V_{IN}. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN} large enough to damage the part.

EMI Consideration

Since parasitic inductance and capacitance effects in PCB circuitry would cause a spike voltage on SW pin when high side MOSFET is turned-on/off, this spike voltage on

SW may impact on EMI performance in the system. In order to enhance EMI performance, there are two methods to suppress the spike voltage. One way is by placing an R-C snubber (R_S*, C_S*) between SW and GND and locating them as close as possible to the SW pin, as shown in Figure 5. Another method is by adding a resistor in series with the bootstrap capacitor, C_{BOOT}, but this method will decrease the driving capability to the high side MOSFET. It is strongly recommended to reserve the R-C snubber during PCB layout for EMI improvement. Moreover, reducing the SW trace area and keeping the main power in a small loop will be helpful on EMI performance. For detailed PCB layout guide, please refer to the section Layout Considerations.

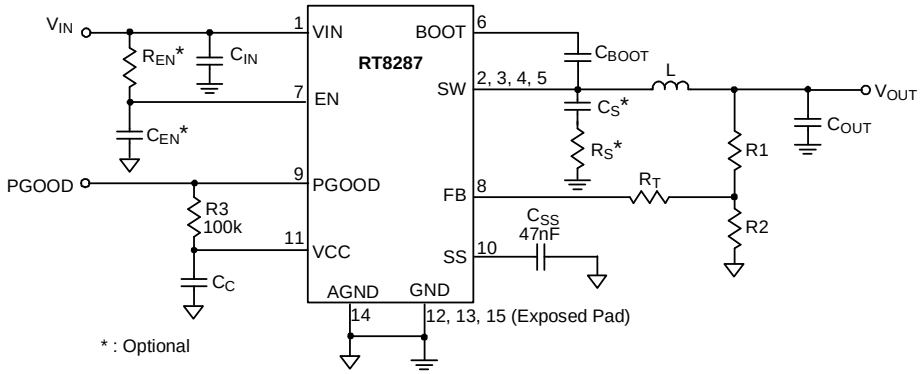


Figure 5. Reference Circuit with Snubber and Enable Timing Control

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications of the RT8287, the maximum junction temperature is 125°C and T_A is the ambient temperature. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For WDFN-14L 4x3 package, the thermal resistance, θ_{JA}, is 60°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (60°C/W) = 1.667W for WDFN-14L 4x3 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. For the RT8287 package, the derating curve in Figure 6 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

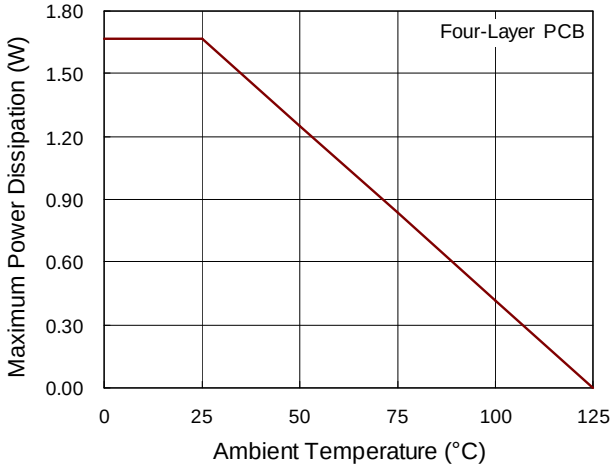


Figure 6. Derating Curve for RT8287 Package

Layout Considerations

Follow the PCB layout guidelines for optimal performance of the IC.

- Keep the traces of the main current paths as short and wide as possible.
- Put the input capacitor as close as possible to the device pins (VIN and GND).
- SW node is with high frequency voltage swing and should be kept at small area. Keep analog components away from the SW node to prevent stray capacitive noise pickup.
- Connect feedback network behind the output capacitors. Keep the loop area small. Place the feedback components near the IC.
- Connect all analog grounds to a command node and then connect the command node to the power ground behind the output capacitors.
- An example of PCB layout guide is shown in Figure 7 for reference.

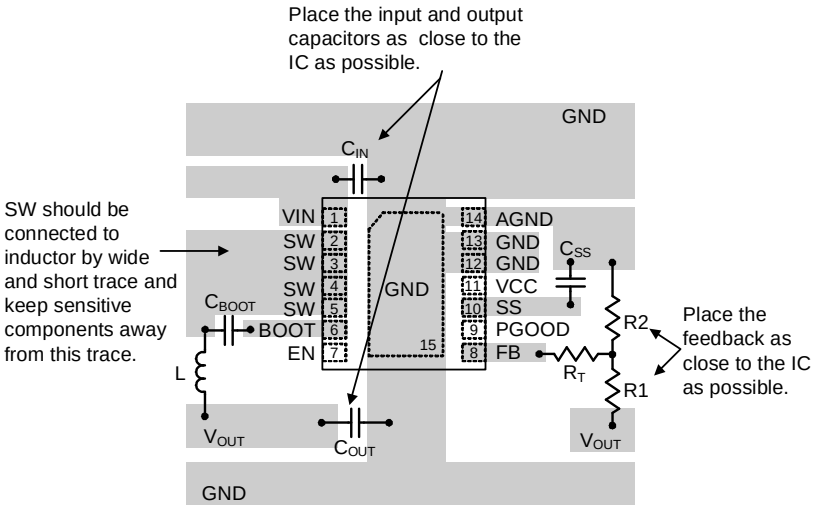
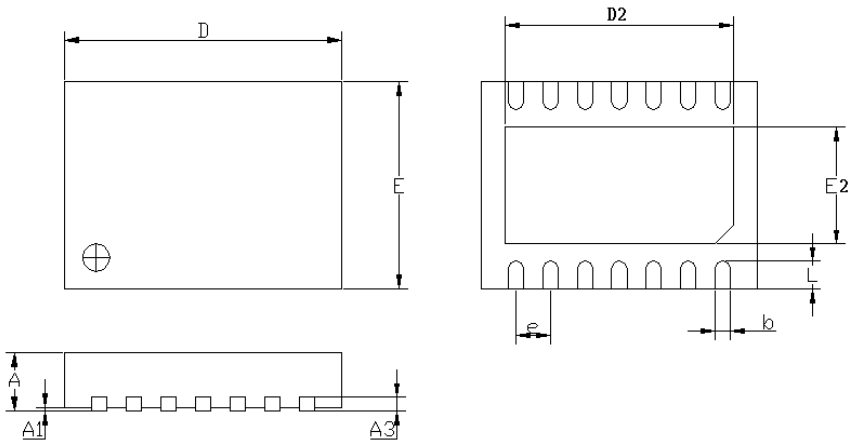


Figure 7. PCB Layout Guide

Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	3.900	4.100	0.154	0.161
D2	3.250	3.350	0.128	0.132
E	2.900	3.100	0.114	0.122
E2	1.650	1.750	0.065	0.069
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 14L DFN 4x3 Package

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