# NCS5021

*Product Preview*

# Dual Band EDGE Compatible PA Controller

The NCS5021 circuit is dedicated to RF Power amplifier control for GSM and DCS standards. It significantly reduces the number of external passive devices while giving the RF designer the capability to perfectly tune the control loop. This device is compatible with both constant and non−constant envelope modulations, which are used with GSM and GSM/EDGE.

### Features

- Integrated Two 50 Ω Matched RF Power Detectors
- Direct Supply from Battery Voltage
- Low Bandwidth Mode (EDGE)
- High Gain Integrator Requesting only One External Capacitor
- PA Control Buffer Compatible with Gate Controlled Amplifiers
- Generation of Pre−bias Level for PA at Start of Burst
- 12 Pins QFN 3 x 3

### Typical Applications

- Global System for Mobile Communication (GSM/DCS)
- Personal Communication Network (PCN)



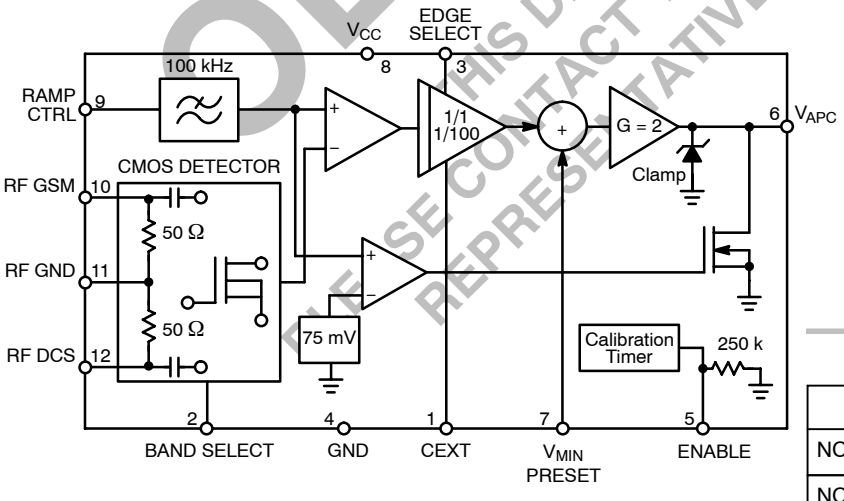


**Figure 1. Functional Block Diagram**

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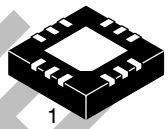
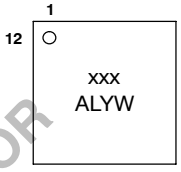
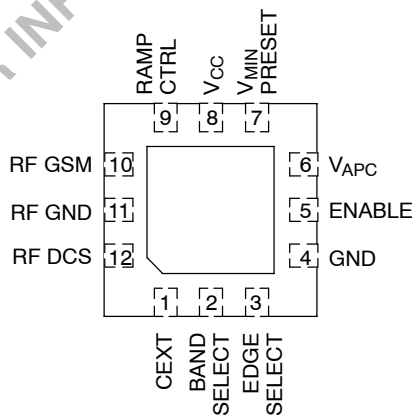


**QFN 3x3−12 LEAD**
**SQL SUFFIX**
**CASE 485N**

**MARKING DIAGRAM**




xxx = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week




**QFN3x3−12** (Top View)

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| NCS5021MN | QFN3x3−12 | Bulk/Railed/Tray |
| NCS5021MNR2 | QFN3x3−12 | Tape & Reel |

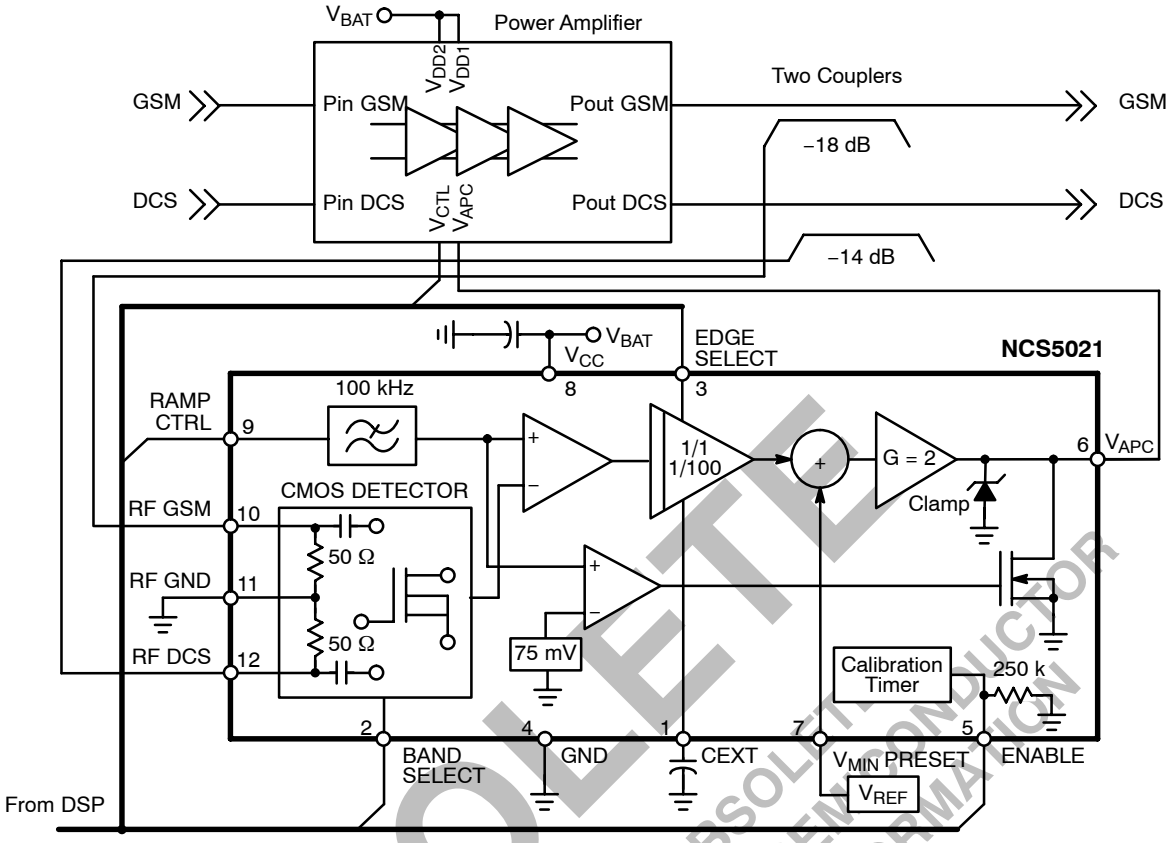



**Figure 2. Typical Application Circuit with Two Couplers**

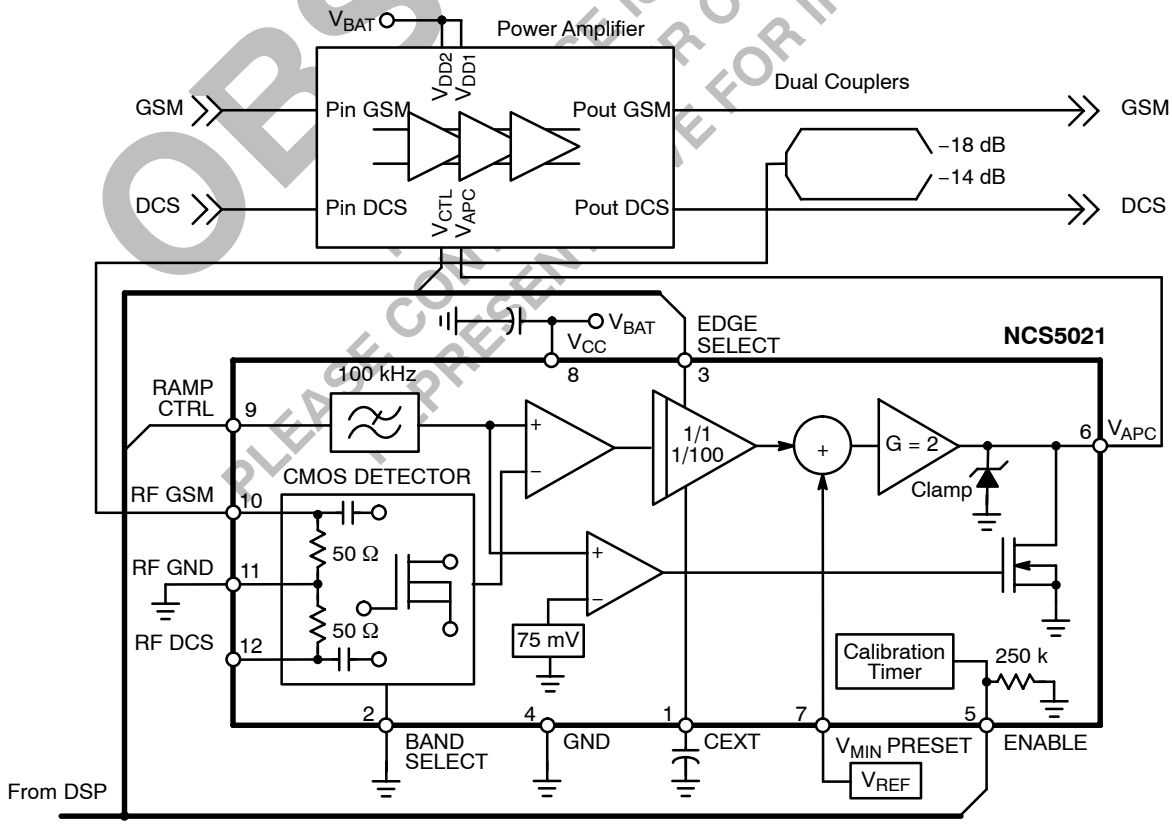



**Figure 3. Typical Application Circuit with Dual Couplers**

## PIN DESCRIPTION

| Pin | Name | Pin Description |
|---|---|---|
| 1 | CEXT | Integrator's external capacitor: The external capacitor is determining the integrator's frequency response and has a direct impact over the loop stability and its transient response. |
| 2 | BAND SELECT | GSM/DCS band selection: A logical "0" on this input pin select the GSM RF input and a logical "1" selects DCS RF input. |
| 3 | EDGE SELECT | EDGE mode selection: When the EDGE pin is switched to a logical "1", the integrator's bandwidth is divided by a factor of one hundred. The control loop becomes too slow to compensate the amplitude modulation created by EDGE. This mode is not activated during power ramp−up and ramp−down to allow the control loop to fit into the GSM time and frequency masks. |
| 4 | GND | Digital ground: To be connected to a digital ground. |
| 5 | ENABLE | Shutdown mode: A zero on this input pin switches off the output buffer $V_{APC}$. Also the Integrator's CEXT capacitor is Reset (shot circuited) and all other functions are in low power mode. This input must be high typically 25 μs before RAMP CONTROL raises. During this time the device is in calibration mode to cancel internal offset. Before each first burst, the device must be set from disable to enable in order to perform the calibration, excepted for a series of burst (GPRS). |
| 6 | $V_{APC}$ | Power Amplifier Control signal: This output pin controls the power amplifier. It remains at zero if ENABLE pin is low. When ENABLE pins high, $V_{APC}$ rises to the voltage level on VMIN PRESET with a gain of 2 only if RAMP CTRL is over than 75 mV. Then it remains at VMIN PRESET level until RAMP CTRL goes over 100 mV, then the loop is closed and $V_{APC}$ controls the PA power. So in order to protect the PA, the output buffer has a clamp at 2.8 V. |
| 7 | VMIN PRESET | Output voltage minimum value: This analog input pin defines the $V_{APC}$ minimum voltage. This level amplified by two should be slightly below the power amplifier amplification threshold. It helps the loop to quickly converge without overshoot when the output power begins to rise. |
| 8 | $V_{CC}$ | Power supply. |
| 9 | RAMP CTRL | Power control loop reference voltage: Due to the output detector offset voltage fixed at 100 mV in GSM and DCS a voltage higher than 100 mV must be applied to raise $V_{APC}$. The ramp control voltage does not give a direct power value. It indicates the voltage, which should be present at the power detector output. |
| 10 | RF GSM | GSM band: RF signal input: The RF signal may vary from 200 MHz to 2.5 GHz. The input power may reach +18 dBm.<br>When no RF is applied, the internal output detector offset is fixed at 100 mV. |
| 11 | RF GND | Ground Pin to be connected to the RF ground. So each internal 50 Ω required for matching is connected between RF input and this ground pin. |
| 12 | RF DCS | DCS band : RF input signal: The RF signal may vary from 200 MHz to 2.5 GHz. The input power may reach +18 dBm.<br>When no RF is applied, the internal output detector offset is fixed at 100 mV. |



## MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Maximum Input Power on RF Pins | $P_{MAX}$ | 23 | dBm |
| Maximum Power Supply | $V_{CCMAX}$ | 5.5 | V |
| Human Body Model (HBM) ESD Rating for RF GSM and RF DCS Pin.<br>All Other Pins are (Note 4) | ESD HBM | 1000<br>2000 | V |
| Machine Model (MM) ESD Rating for RF GSM and RF DCS Pin.<br>All Other Pins are (Note 5) | ESD MM | 100<br>200 | V |
| Operating Ambient Temperature | TA | −30 to +85 | °C |
| Storage Temperature | $T_{stg}$ | −65 to +150 | °C |
| Maximum Input DC Voltage on Pins | $V_{IMAX}$ | $V_{CC}$+ 0.3 | V |
| Minimum Input DC Voltage on Pins | $V_{IMIN}$ | −0.3 | V |
| Maximum Current on Pin $V_{APC}$ | $IO_{MAX}$ | 15 | mA |

1. Guaranteed by design.
2. Tested.
3. Guaranteed by design and characterized.
4. Human Body Model, 100 pF discharged through a 1.5 kΩ resistor following specification JESD22/A114.
5. Machine Model, 200 pF discharged through all pins following specification JESD22/A115.

**ELECTRICAL CHARACTERISTICS** Limits apply for TA between −30°C to +85°C (unless otherwise noted).

**Input Specifications**

| Pin | Rating | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| 8 | Operating Power Supply (Note 6) | $V_{CC}$ | 2.9 | – | 4.8 | V |
| 8 | Active Mode Current Consumption (Unloaded) (Note 6) | $I_{CC}$ | – | 4.7 | 7.0 | mA |
| 8 | Power Down Current Consumption (Note 6) | $I_{pdn}$ | – | 0.1 | 1.0 | μA |
| 5 | Wake Up Time (Notes 8 and 9) | $W_{ut}$ | TBD | 25 | 50 | μs |
| 10<br>12 | Operating Frequency Range Max (Note 8) | F_in | 200 | – | 2500 | MHz |
| 9 | Operating Voltage Range on Ramp CTRL (Note 8) | V Ramp CTRL | – | – | 1800 | mV |
| 7 | Operating voltage range on VMIN PRESET. Below 100 mV with 0 V from integrator, the transfer function is not guaranteed linear but lower than the straight line defined by GOP. (Note 6) | $V_{MIL}$ | 0.1 | – | 0.8 | V |

**Detector**

| | | | | | | |
|---|---|---|---|---|---|---|
| 10<br>12 | Linear Detection Range (Note 8)<br>With a ±1.0 dB Linearity in Nominal Conditions at +25°C<br>With a ±2.0 dB Linearity at −30°C < T < +85°C | Range Linear | −20 | – | 18 | dBm |
| 10<br>12 | Not Linear Detection Range (Note 8) | Range Not Linear | −25 | – | 20 | dBm |
| 10<br>12 | Detector Sensitivity (Note 8)<br>Fin = 2.0 GHz, $R_{fin}$ = −15 dBm<br>Fin = 800 MHz, $R_{fin}$ = 20 dBm | Det_Sens | <br>10<br>– | <br>–<br>– | <br>–<br>1800 | mV |
| 10<br>12 | Input Impedance on RF GSM and RF DCS Pin | R_in | – | 50 | – | Ω |
| 10<br>12 | Harmonic Return Loss by RF_IN up to 20 dBm @ 900 MHz (Note 8)<br>H2<br>H3 | H_Return | <br>–<br>– | <br>−38<br>−52 | <br>–<br>– | dBc |
| 10<br>12 | Voltage Standing Wave Ratio @ 25°C (Note 8) | VSWR | – | – | 2:1 | – |
| 10<br>12 | Internal Output Detector Delay to 90% Detected of RF Power Step (Note 7) | DD | – | 100 | 300 | ns |

**Filter and Comparator**

| | | | | | | |
|---|---|---|---|---|---|---|
| 9 | Ramp CTRL Threshold Offset Voltage to Close Loop @ 25°C and $V_{CC}$ = 3.6 V (Note 8) | O Ramp CTRL | 90 | 100 | 110 | mV |
| 9 | Ramp CTRL Drifting Threshold Voltage versus $V_{CC}$ and Temperature (Note 8) | D Ramp CTRL | – | – | 5.0 | mV |
| 9 | Smoothing Filter Corner Frequency @ 25°C (Note 7) | FCS | 100 | – | – | kHz |
| 9 | Smoothing Filter Attenuation @ 1.0 MHz @ 25°C (Note 7) | ATT | 45 | – | – | dB |
| 9 | Comparator Threshold to Switch on VMIN PRESET versus O Ramp CTRL. Due to hysteresis, add 5 mV for going up and remove 5 mV for going down (Note 6) | V THRD | 50 | 70 | 90 | mV |
| 9 | Comparator Hysteresis @ 25°C and 3.6 V (Note 8) | H THRD | – | 10 | – | mV |

6. Tested.
7. Guaranteed by design.
8. Guaranteed by design and characterized.
9. Time necessary for internal calibration, see “t1” on Figure 20. Typical Timing Chart for GSM and EDGE Application.

**ELECTRICAL CHARACTERISTICS** Limits apply for TA between −30°C to +85°C (unless otherwise noted).

**Integrator Section**

| Pin | Rating | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| – | DC Gain (Note 11) | GDC | 55 | 70 | – | dB |
| | Open Loop Band−Width from the Detector (RF GSM or RF DCS) to Output Buffer ($V_{APC}$) @ 25 °C and CEXT = 1 nF (Note 12)<br>EDGE SELECT = 0 (not active)<br>EDGE SELECT = 1 (active) | INT_BW | <br>–<br>– | <br>160<br>1.6 | <br>–<br>– | kHz |
| | Phase Margin (Note 12) | P_MARG | 60 | 75 | | ° |
| 5<br>7 | Step Level on $V_{APC}$ when EDGE is Switch in Close Loop with RAMP CTRL constant in operating range. Typical Value @ $V_{CC}$ = 3.6 V and 25°C (Note 11) | S EDGE | – | 2.5 | – | mV |

**Output Buffers and Logic Section**

| | | | | | | |
|---|---|---|---|---|---|---|
| 6 | Buffer Available Output Current (Note 10)<br>$V_{APC}$ = ($V_{APC}$ unloaded −100 mV)<br>$V_{APC}$ = ($V_{APC}$ unloaded + 100 mV))<br>$V_{APC}$ = 50 mV | $I_{out}$ | <br>10<br>−1.0<br>−0.1 | <br>–<br>–<br>– | <br>–<br>–<br>– | mA |
| 6 | Output Buffers Voltage Clamp (Note 10) | $V_{high}$ | 2.65 | 2.8 | 3.0 | V |
| – | Simulate Bandwidth With Out the Integrator Through Close Loop Way (Detector, Comparator, Adder and Output Buffer) (Note 11) | BW | 8.0 | 10 | – | MHz |
| 7 | From 0.1 to 0.8 Apply on VMIN PRESET and no voltage from Integrator. $V_{APC}$ is equal at Two Times VMIN PRESET (Note 10) | GOP | −10 | – | +10 | % |
| 6 | Ripple Rejection, (Ripple 0.2 Vp−p) @ 25°C in Close Loop. (Note 12)<br>= 1.0 kHz EDGE = 0<br>= 10 kHz EDGE = 0<br>= 1.0 kHz EDGE = 1<br>= 10 kHz EDGE = 1 | PSRR | <br>60<br>58<br>50<br>35 | <br>70<br>68<br>60<br>45 | <br>–<br>–<br>– | dB |
| 2, 3, 5 | Voltage Input Logic Low (Note 10) | $V_{IL}$ | – | – | 0.3 | V |
| 2, 3, 5 | Voltage Input Logic High (Note 10) | $V_{IH}$ | 1.5 | – | – | V |
| 2, 3 | Current Input Logic (Note 11) | Lin | – | 0.01 | 0.1 | μA |
| 5 | Pull down on ENABLE logic input to keep level low when the driver is in high impedance condition. (Note 12) | PDE | 150 | 250 | 400 | kΩ |

10. Tested.
11. Guaranteed by design.
12. Guaranteed by design and characterized.

## TYPICAL PERFORMANCE CHARACTERISTICS

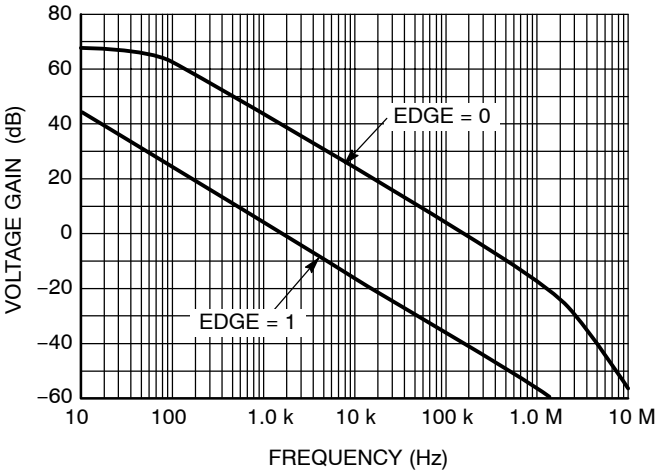



**Figure 4. Open−Loop Gain at CEXT = 1.0 nF**

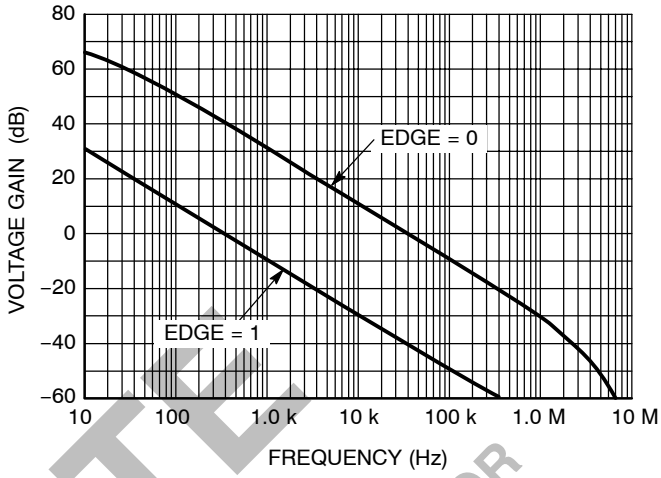



**Figure 5. Open−Loop Gain at CEXT = 4.7 nF**

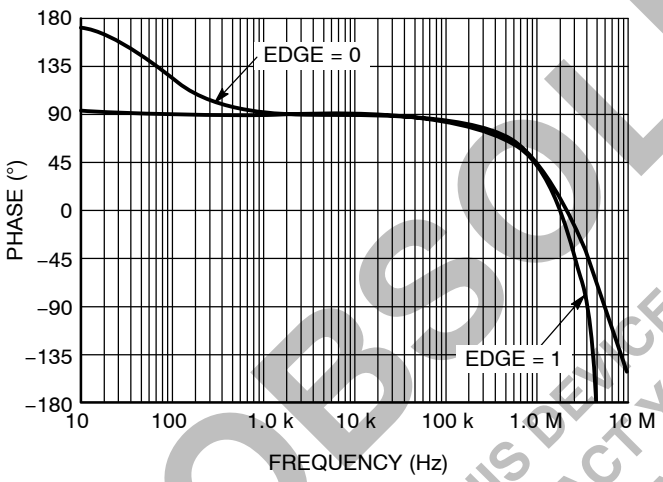



**Figure 6. Open−Loop Phase at CEXT = 1.0 nF**

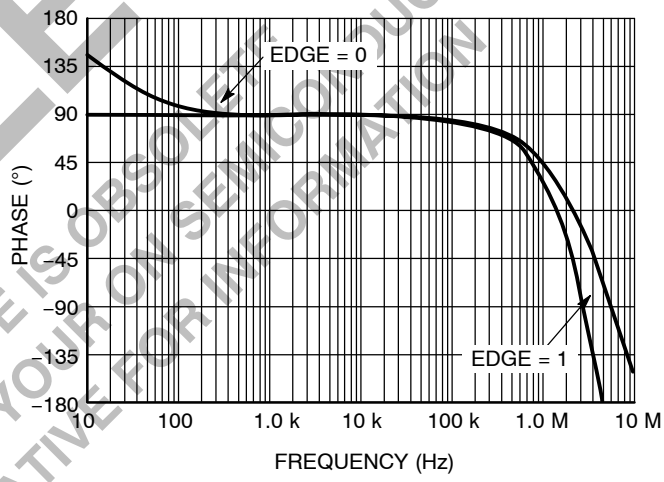



**Figure 7. Open−Loop Phase at CEXT = 4.7 nF**

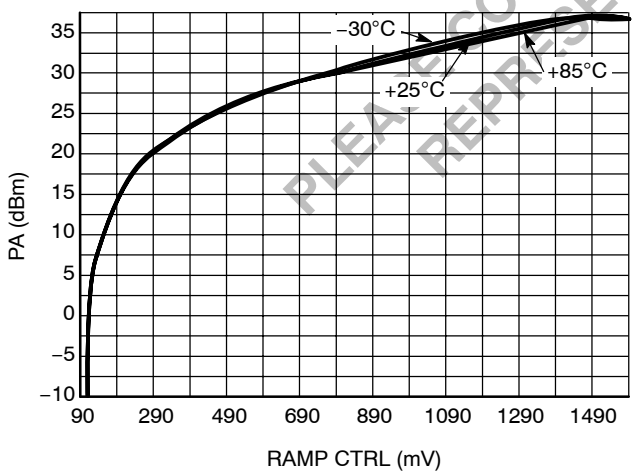



**Figure 8. Transfer Function with 18 dB Coupler at 900 MHz**

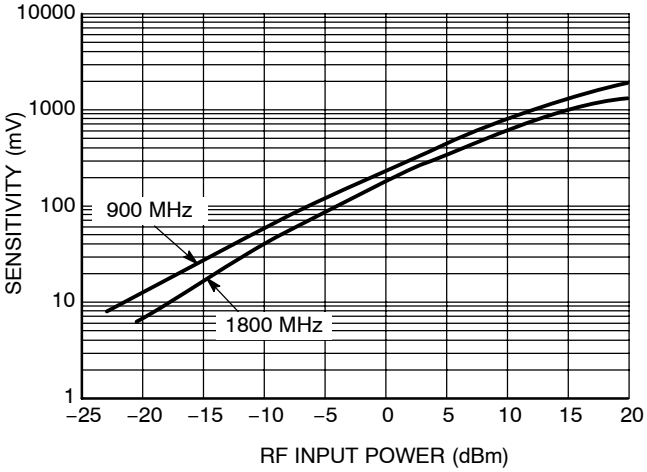



**Figure 9. Detector Characteristic**

## TYPICAL PERFORMANCE CHARACTERISTICS

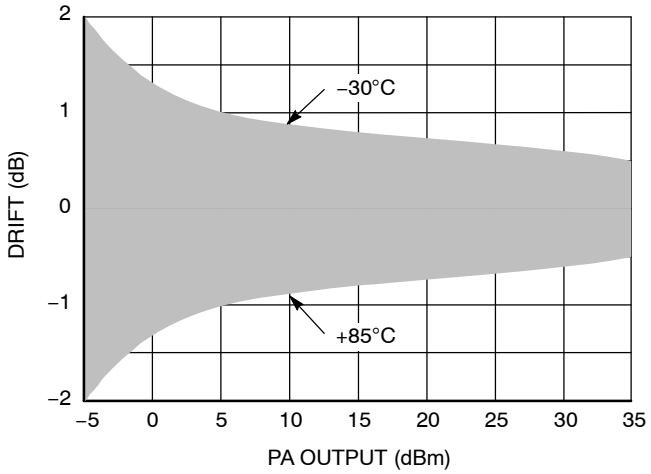



**Figure 10. PA Output Drift vs. Temperature with 18 dB Coupler at 900 MHz**

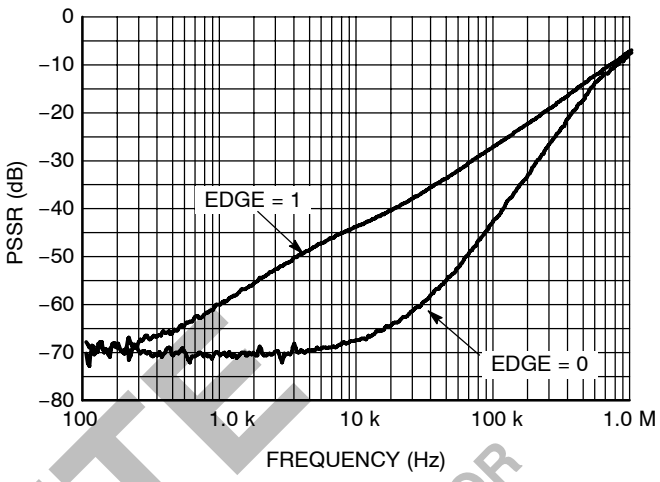



**Figure 11. PSRR at $V_{CC}$= 3.6 V and Ripple 0.2 Vp−p**

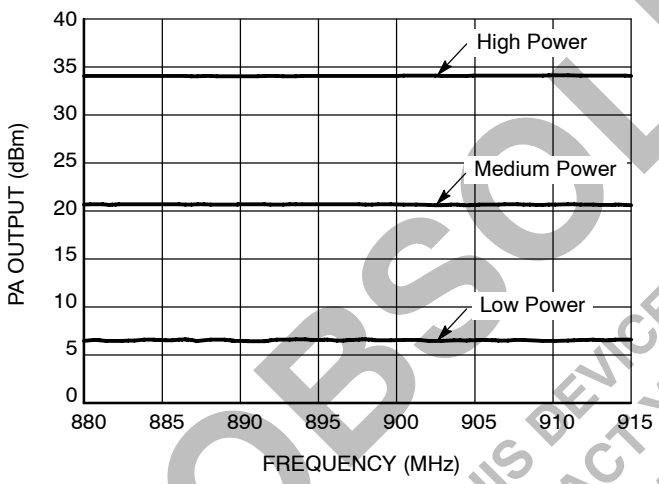



**Figure 12. PA Output vs. EGSM Frequency Range with 18 dB Coupler**

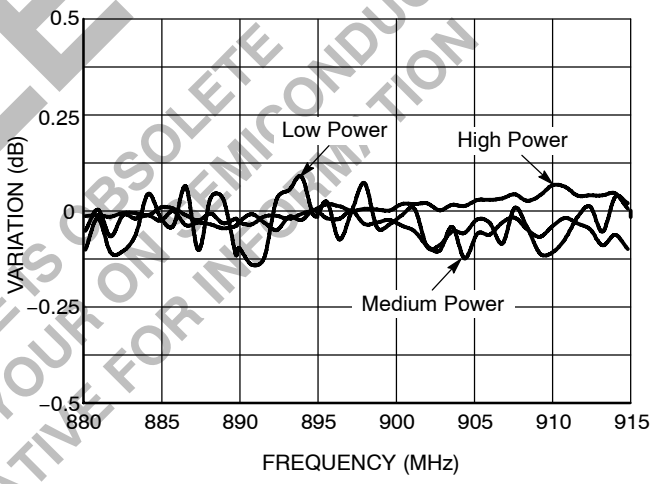



**Figure 13. Power Variation vs. EGSM Frequency Range**

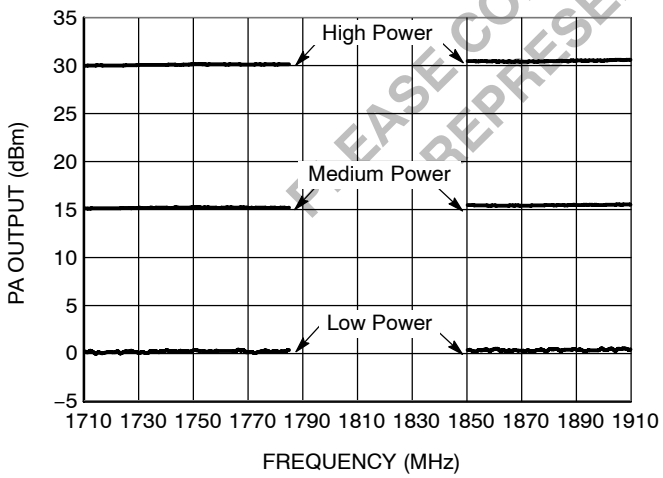



**Figure 14. PA Output vs. DCS/PCS Frequency Range with 14 dB Coupler**

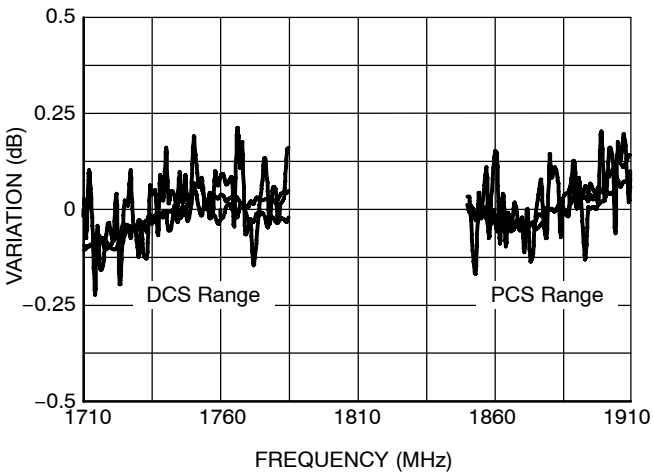



**Figure 15. Power Variation vs. DCS/PCS Frequency Range**

## TYPICAL PERFORMANCE CHARACTERISTICS

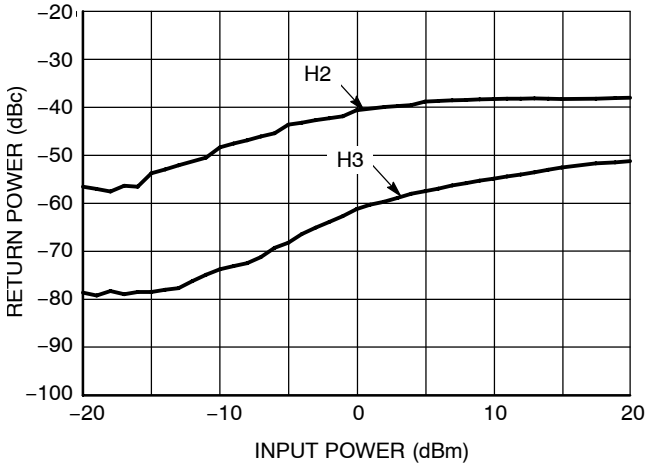



**Figure 16. Return Harmonic by Input RF GSM or RF DCS at 900 MHz**

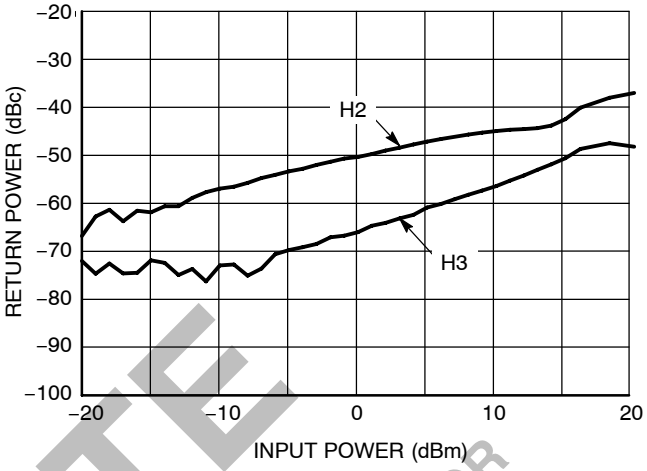



**Figure 17. Return Harmonic by Input RF GSM or RF DCS at 1.8 GHz**

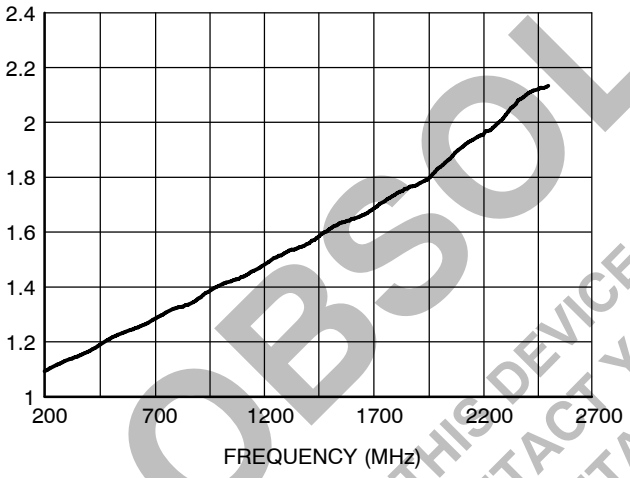



**Figure 18. VSWR for Input RF GSM or RF DCS**

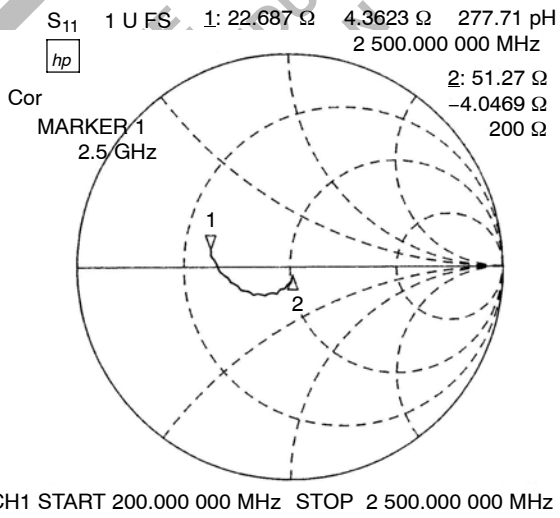



**Figure 19. S11 Parameter in Smith Chart for Input RF GSM or RF DCS**

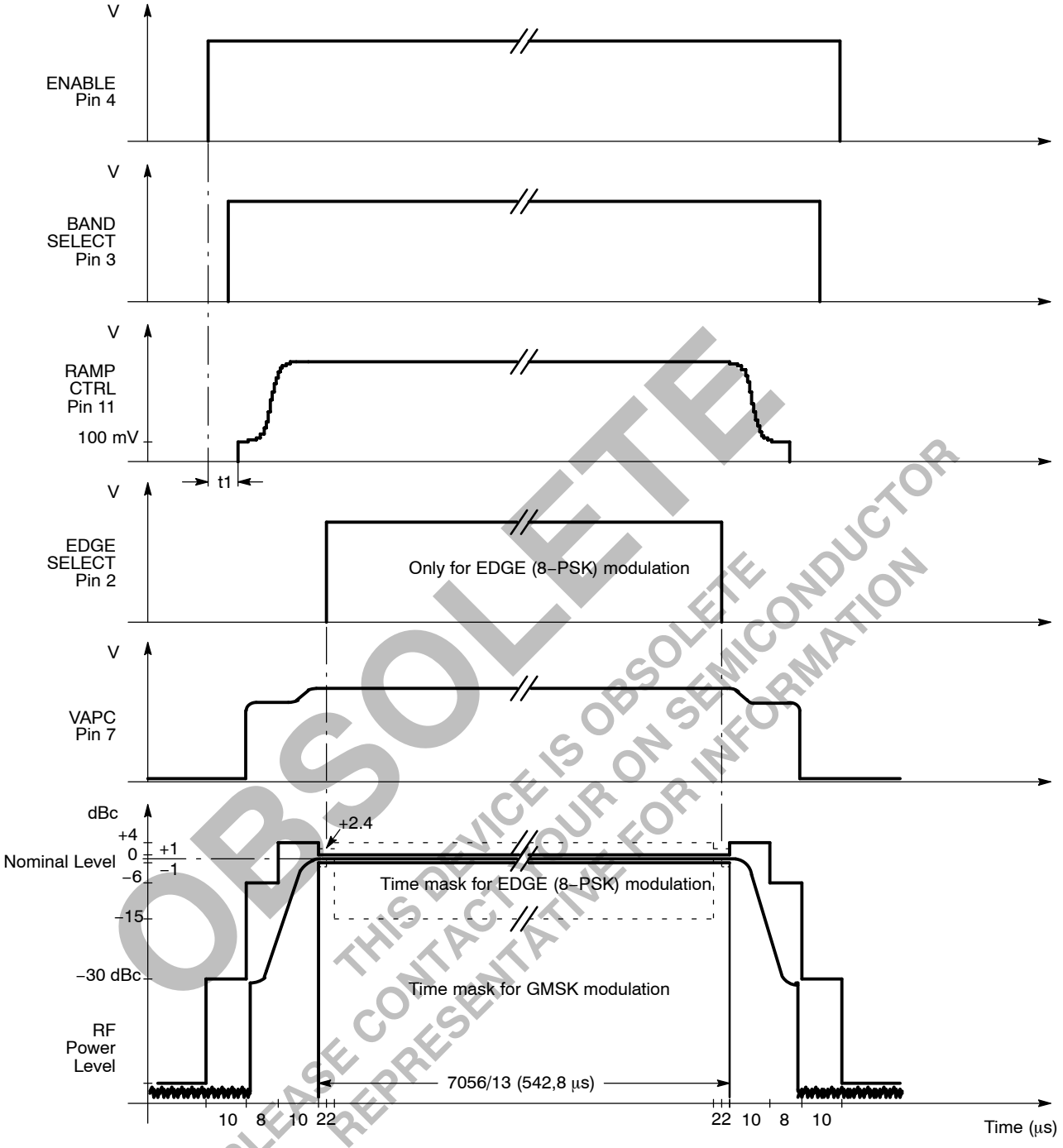





**Figure 20. Typical Timing Chart for GSM and EDGE Application**

## DETAILED OPERATING DESCRIPTION

### RF Power Detector

It performs the amplitude demodulation of applied RF input signal. Its dynamic range fully covers the different GSM power levels. The requested biasing signals are internally generated. The power detector is designed to fulfill the GSM 05.05 standard providing good peak power control over a 40 dB linear range. The 43 dB detection range allows the Figure 20 template to be respected during ramp−up and ramp down. The very low out−of−burst noise floor can be achieved by apply level from DAC lower than 75 mV to RAMP CTRL. The detector is designed to operate with a RF coupler providing a 18 dB attenuation in GSM mode and a 14 dB attenuation in DCS/PCS is recommended by Murata, for example. 8 bits DAC may be used as Reference signal generator. Nevertheless such low resolution DAC may result in a loss of accuracy at very low power levels (beginning of the ramp). The RF GSM and RF DCS inputs are both 50 Ω matched with DC coupling capacitor and provide a very good Voltage Standing Wave Radio (VSWR). Linearity detection versus frequency is there by excellent and could allow use of a frequency−correcting table. Nevertheless the coupler may a have coupling factor variation and downgraded the linearity.

### Reference Signal Filter

If we consider a close loop operation and an infinite integrator gain, the reference voltage will be equal to the internal detector output voltage. So, knowing the transfer function characteristics (see Figure 8), it defines the PA output power. The reference signal varies during the burst to reach the requested Tx power, to stand at the nominal power level, and then return to the specified out−of−burst level. This signal is generated with a clocked DAC, whose steps have to be smoothed to minimize switching transients. The third order Bessel filter's transfer function is defined to comply with GSM requirements in terms of switching transients and time and frequency masks. A systematic offset has been created on REF input to ensure that the loop remains closed even at very low output power whatever the internal offset voltages.

### Integrator

The integrator performs two different functions. Due to its very high gain, it minimizes the error signal resulting from detector's output and reference signal comparison, contributing to power control accuracy. Then, by the correct bandwidth setting, it guarantees the system stability and fits GSM time mask. Due to the system constraint, a fine frequency tuning is often requested. The NCS5021 circuit provides this flexibility by keeping the integrator capacitor external. To limit power consumption, the external capacitor charge and discharge current does not exceed 100 μA (typical). The minimal external capacitor should not be lower than 47 pF to guarantee loop stability and should not exceed 4.7 nF.

### Minimum Voltage Adder

The power amplifier control input needs to reach a certain threshold before the output power begins to rise. Due to the integrator's low bandwidth which has been chosen for stability reasons, an important delay may be present before the power begins to rise. Furthermore, some ringing may occur when the control loop switches from its inactive state, to normal, regulated state. An efficient way to solve these problems is to raise the PA control voltage to a $V_{MIN}$ Preset voltage, very close to the emission threshold. $V_{MIN}$ Preset signal is added to the integrator's output signal through the output buffer amplified by two.

### Output Buffer

The output buffer is providing the current capability to drive the PA control input. With Enable pin low, $V_{APC}$ remains low to make that sure RF power will not be supplied by the PA. So the device may be switched on typically by 25 μs before the burst to ramp−up, to allow the internal calibration sequence.

### Power−down Mode

During the unused time slots in Time Division Multiple Access (TDMA) systems, the NCS5021 must be in low power mode by applying a zero logic level on pin ENABLE. This function saves power from battery and put PA in low power by supplying very low level to output buffer $V_{APC}$. Also when power−down mode is active, the external capacitor is discharged to initial conditions for next burst. This input must be high typically by 25 μs before Ramp Control goes high.

## DEMO BOARD

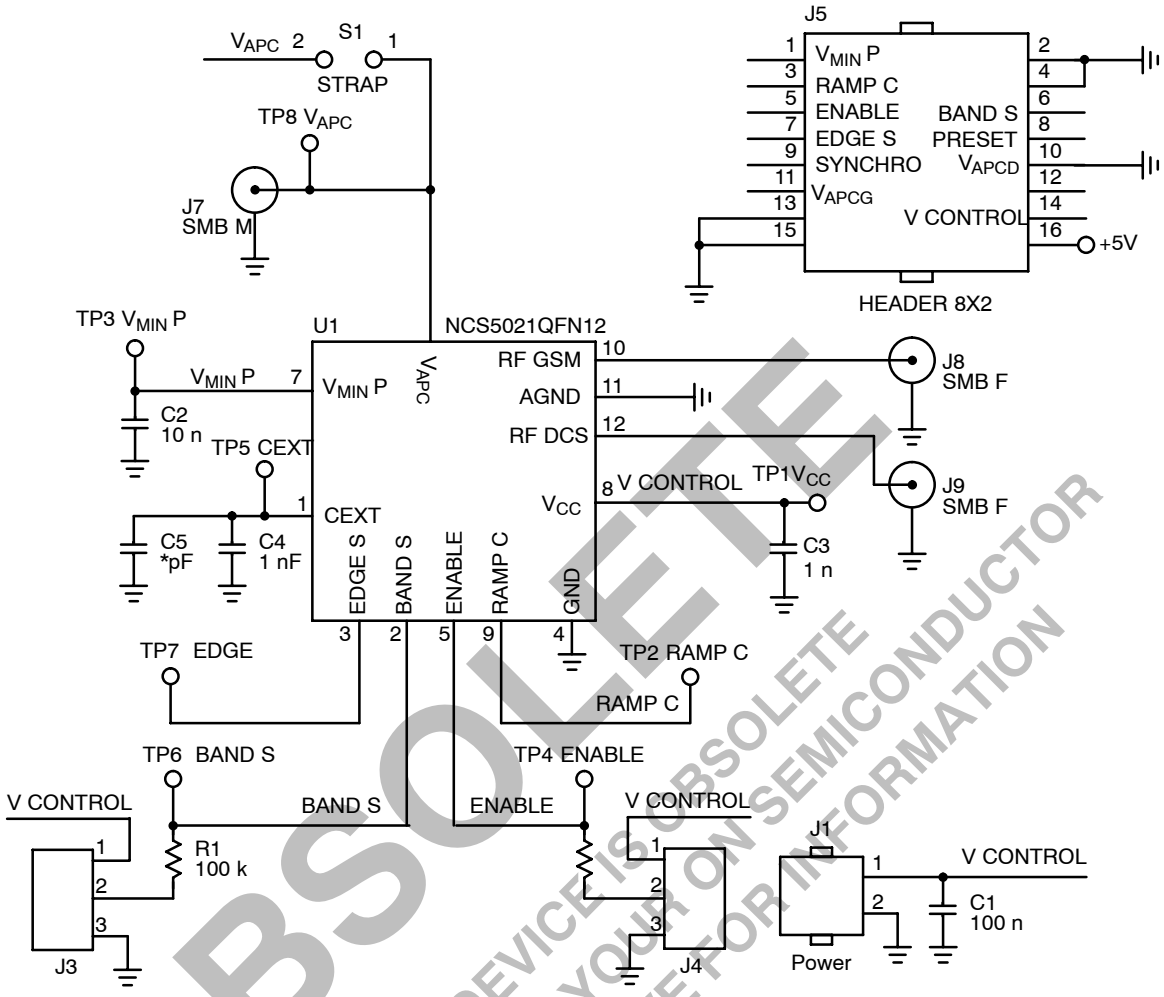



Figure 21. Demo Board Schematic

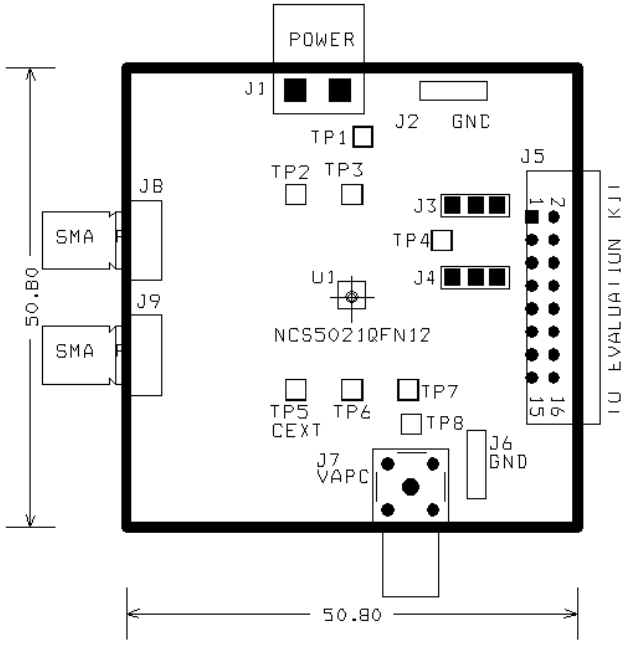



Figure 22. Silkscreen

## DEMO BOARD

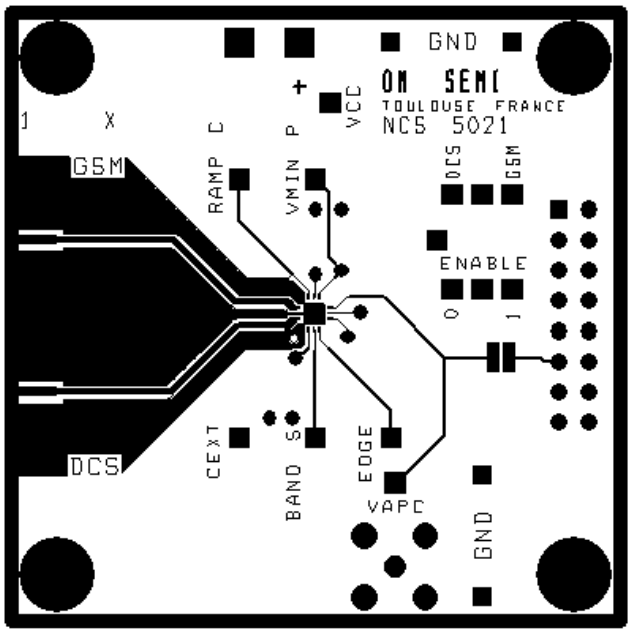



Figure 23. PCB Top View

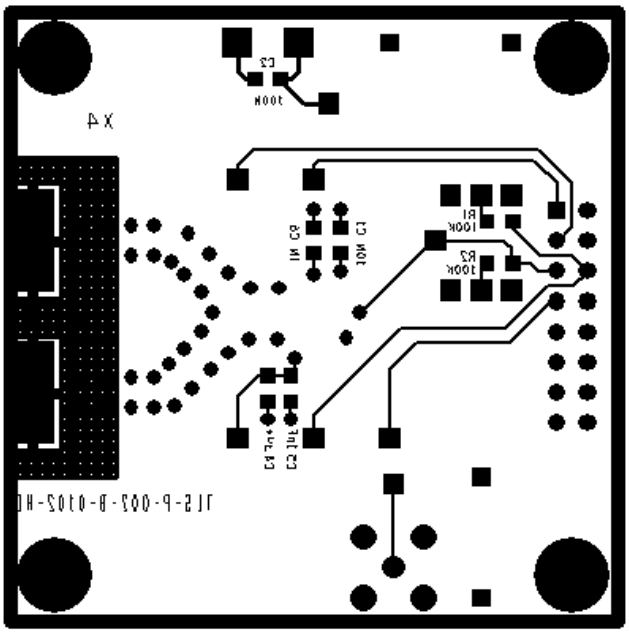
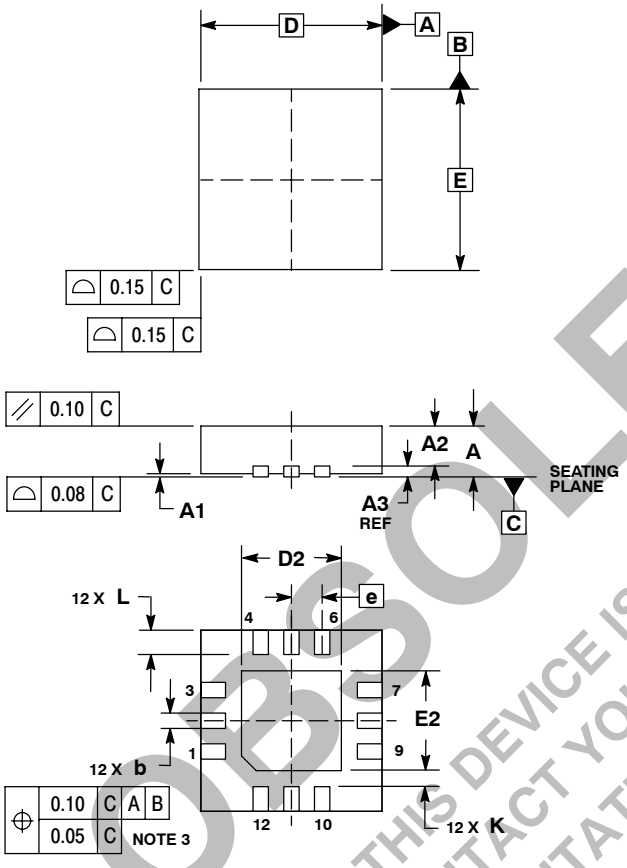


Figure 24. PCB Bottom View

## PACKAGE DIMENSIONS

**12 PIN, 3X3 QFN**
**CASE 485N−01**
**ISSUE O**




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 0.80 | 1.00 |
| A1 | 0.00 | 0.05 |
| A2 | 0.65 | 0.75 |
| A3 | 0.20 REF | |
| b | 0.20 | 0.30 |
| D | 3.00 BSC | |
| D2 | 1.50 | 1.80 |
| E | 3.00 BSC | |
| E2 | 1.50 | 1.80 |
| e | 0.50 BSC | |
| K | 0.20 | --- |
| L | 0.35 | 0.45 |





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