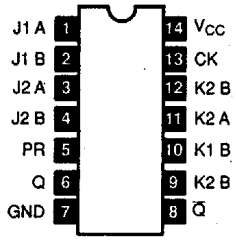
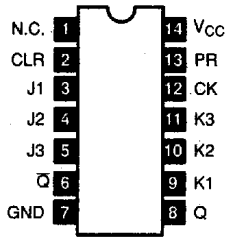
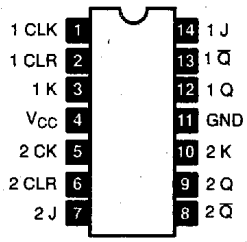
NTE74H71 14–Lead DIP, See Diag. 247
AND Gated J–K Master/Slave Flip–Flop w/Preset & Clear



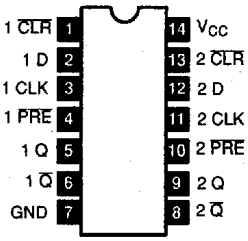
NTE7472, NTE74H72 14–Lead DIP, See Diag. 247
AND Gated J–K Master/Slave Flip–Flop w/Preset & Clear



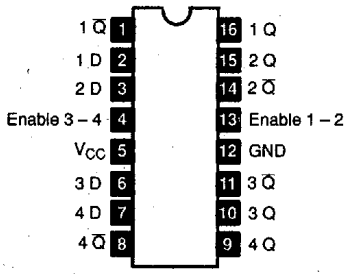
NTE7473, NTE74C73, NTE74H73, NTE74LS73 14–Lead DIP, See Diag. 247
Dual J–K Flip–Flop w/Clear



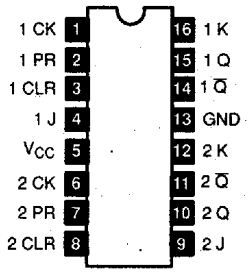
NTE7474, NTE74C74, NTE74H74, NTE74LS74A, NTE74S74 14–Lead DIP, See Diag. 247
Dual D–Type Positive Edge Triggered Flip–Flop w/Preset & Clear



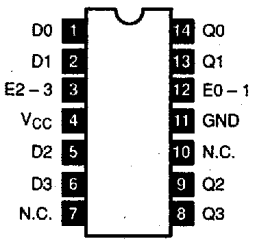
NTE7475, NTE74LS75 16–Lead DIP, See Diag. 249
4–Bit Bistable Latch



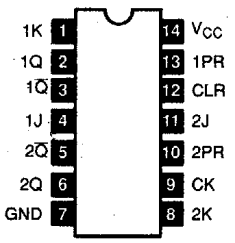
NTE7476, NTE74C76, NTE74H76, NTE74LS76A 16–Lead DIP, See Diag. 249
Dual J–K Flip–Flop w/Preset & Clear



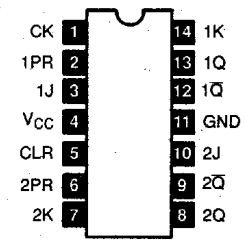
NTE74LS77 14–Lead DIP, See Diag. 247
4–Bit D–Type Latch



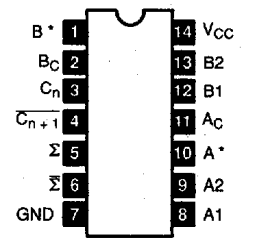
NTE74H78 14–Lead DIP, See Diag. 247
Dual J–K Flip–Flop w/Preset, Common Clear, & Common Clock



NTE74LS78 14–Lead DIP, See Diag. 247
Dual J–K Flip–Flop w/Preset, Common Clear, & Common Clock

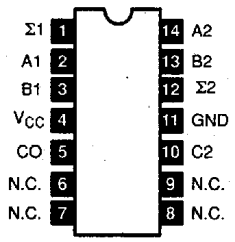


NTE7480 14–Lead DIP, See Diag. 247
Gated Full Adder w/Complementary Inputs & Complementary Sum Outputs

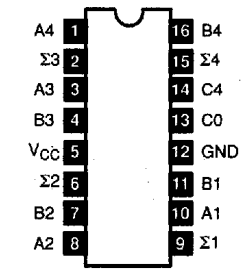


Note: This configuration is nonstable, that is, it will not presist when preset and clear inputs return to their inactice (High) level.

NTE7482 14–Lead DIP, See Diag. 247
2–Bit Binary Full Adder



NTE7483, NTE74LS83A 16–Lead DIP, See Diag. 249
4–Bit Binary Full Adder w/Fast Carry



See Diagrams, beginning on Page 1–293