FAIRCHILD SEMICONDUCTOR®

November 2010

FL6961
Single-Stage Flyback and Boundary Mode PFC Controller for Lighting

Features

- Boundary Mode PFC Controller
- Low Input Current THD
- Controlled On-Time PWM
- Zero-Current Detection
- Cycle-by-Cycle Current Limiting
- Leading-Edge Blanking instead of RC Filtering
- Low Startup Current: 10μA Typical
- Low Operating Current: 4.5mA Typical
- Feedback Open-Loop Protection
- Programmable Maximum On-Time (MOT)
- Output Over-Voltage Clamping Protection
- Clamped Gate Output Voltage 16.5V

Applications

- General LED Lighting
- Industrial, Commercial and Residential Fixtures
- Outdoor Lighting : Street, Roadway, Parking, Construction and Ornamental LED Lighting Fixtures

Description

The FL6961 is general lighting power controller for low to high power lumens applications requiring power factor correction. It is designed for flyback, or boost converter operating in boundary-mode. The FL6961 provides a controlled on-time to regulate the output DC voltage and achieve natural power factor correction. The maximum on-time of the external switch is programmable to ensure safe operation during AC brownouts. An innovative multi-vector error amplifier is built in to provide rapid transient response and precise output voltage clamping. A built-in circuit disables the controller if the output feedback loop is opened. The startup current is lower than 20μA and the operating current has been reduced to under 6mA. The supply voltage can be up to 25V, maximizing application flexibility.

Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
FL6961MY	-40°C to +125°C	8-Pin, Small Outline Package (SOP)	Tape & Reel

Application Diagram

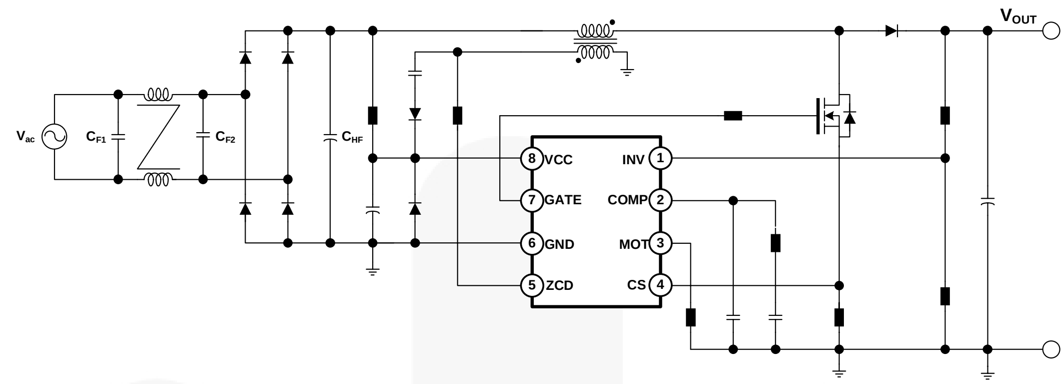


Figure 1. Typical Application Circuit for Step-up Converter

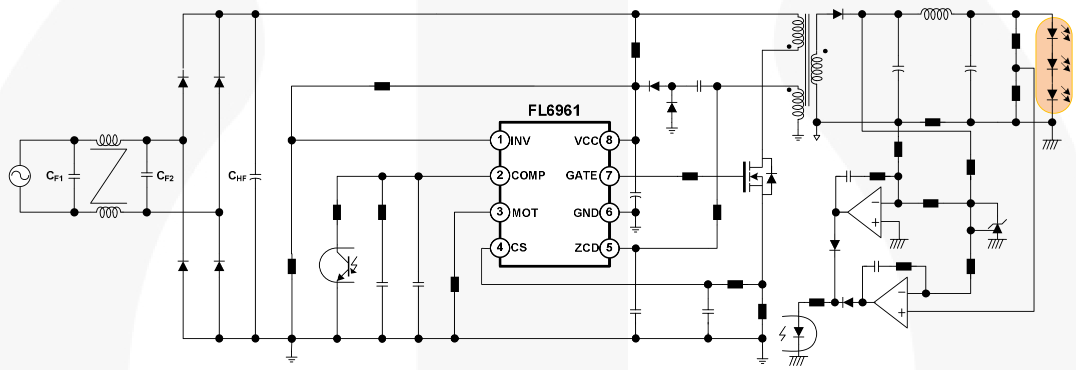


Figure 2. Typical Application Circuit for Single Stage PFC Converter

Block Diagram

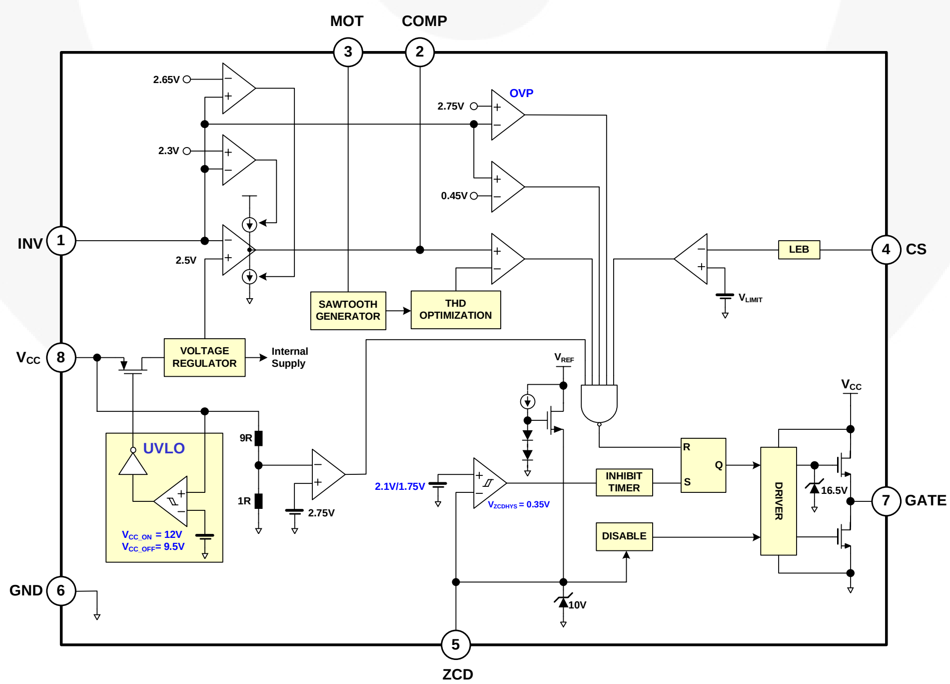
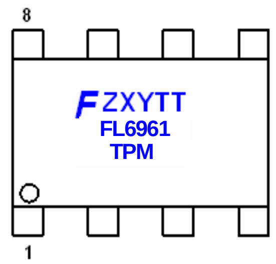


Figure 3. Function Block Diagram

Marking Information



F- Fairchild Logo
Z- Plant Code
X- Year Code
Y- Week Code
TT: Die Run Code
T: Package Type (M=SOP)
P: Z: Pb Free Y: Green Compound
M: Manufacture Flow Code

Figure 4. Marking Information

Pin Configuration

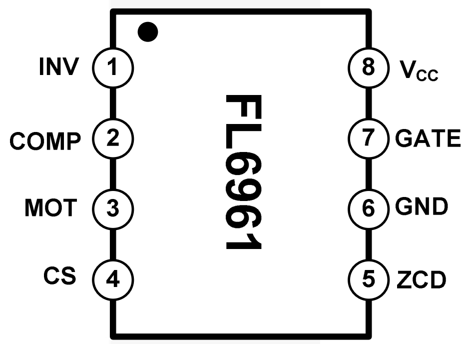


Figure 5. Pin Configuration (Top View)

Pin Definitions

Pin #	Name	Description
1	INV	**Inverting Input of the Error Amplifier**. INV is connected to the converter output via a resistive divider. This pin is also used for over-voltage clamping and open-loop feedback protection.
2	COMP	**Output of the Error Amplifier**. To create a precise clamping protection, a compensation network between this pin and GND is suggested.
3	MOT	**Maximum On Time**. A resistor from MOT to GND is used to determine the maximum on-time of the external power MOSFET. The maximum output power of the converter is a function of the maximum on time.
4	CS	**Current Sense**. Input to the over-current protection comparator. When the sensed voltage across the sense resistor reaches the internal threshold (0.8V), the switch is turned off to activate cycle-by-cycle current limiting.
5	ZCD	**Zero Current Detection**. This pin is connected to an auxiliary winding via a resistor to detect the zero crossing of the switch current. When the zero crossing is detected, a new switching cycle is started. If it is connected to GND, the device is disabled.
6	GND	**Ground**. The power ground and signal ground. Placing a 0.1µF decoupling capacitor between VCC and GND is recommended.
7	GATE	**Driver Output**. Totem-pole driver output to drive the external power MOSFET. The clamped gate output voltage is 16.5V.
8	V_{CC}	**Power Supply**. Driver and control circuit supply voltage.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. All voltage values, except differential voltage, are given with respect to GND pin.

Symbol	Parameter	Min.	Max.	Unit
V_{VCC}	DC Supply Voltage		30	V
V_{HIGH}	Gate Driver	-0.3	30.0	V
V_{LOW}	Others (INV, COMP, MOT, CS)	-0.3	7.0	V
V_{ZCD}	Input Voltage to ZCD Pin	-0.3	12.0	V
P_D	Power Dissipation		400	mW
T_J	Operating Junction Temperature	-40	+125	°C
θ_{JA}	Thermal Resistance (Junction-to-Air)		150	°C/W
T_{STG}	Storage Temperature Range	-65	+150	°C
T_L	Lead Temperature (Wave Soldering or IR, 10 Seconds)		+230	°C
ESD	Human Body Model: JESD22-A114		2.5	KV
	Machine Model: JESD22-A115		200	V

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_A	Operating Ambient Temperature	-40		+125	°C

Electrical Characteristics

Unless otherwise noted, V_{CC}=15V and T_J=-40°C to 125°C. Current is defined as positive into the device and negative out of the device.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{CC} Section						
V_{CC-OP}	Continuous Operation Voltage				24.5	V
V_{CC-ON}	Turn-On Threshold Voltage		11.5	12.5	13.5	V
V_{CC-OFF}	Turn-Off Threshold Voltage		8.5	9.5	10.5	V
I_{CC-ST}	Startup Current	$V_{CC}=V_{CC-ON}$ – 0.16V		10	20	µA
I_{CC-OP}	Operating Supply Current	V_{CC}=12V, V_{CS}=0V, C_L=3nF, f_{SW}=60KHz		4.5	6	mA
V_{CC-OVP}	V_{DD} Over-Voltage Protection Level		26.8	27.8	28.8	V
$t_{D-VCCOVP}$	V_{DD} Over-Voltage Protection Debounce			30		µs
Error Amplifier Section						
V_{REF}	Reference Voltage		2.475	2.500	2.525	V
Gm	Transconductance			125		µmho
V_{INVH}	Clamp High Feedback Voltage			2.65	2.70	V
V_{INVL}	Clamp Low Feedback Voltage		2.25	2.30		V
$V_{OUT\ HIGH}$	Output High Voltage		4.8			V
V_{OZ}	Zero Duty Cycle Output Voltage		1.15	1.25	1.35	V
$V_{INV-OVP}$	Over-Voltage Protection for INV Input		2.70	2.75	2.80	V
$V_{INV-UVP}$	Under-Voltage Protection for INV Input		0.40	0.45	0.50	V
I_{COMP}	Source Current	V_{INV}=2.35V, V_{COMP}=1.5V	10	20		µA
		V_{INV}=1.5V	550	800		
	Sink Current	V_{INV}=2.65V, V_{COMP}=5V	10	20		
Current-Sense Section						
V_{PK}	Threshold Voltage for Peak Current Limit Cycle-by-Cycle Limit		0.77	0.82	0.87	V
t_{PD}	Propagation Delay				200	ns
t_{LEB}	Leading-Edge Blanking Time	R_{MOT}=24kΩ, V_{COMP}=5V		400	500	ns
		R_{MOT}=24kΩ, $V_{COMP}=V_{OZ}$+50mV		270	350	
Gate Section						
V_{Z-OUT}	Output Voltage Maximum (Clamp)	V_{CC}=25V	14.5	16.0	17.5	V
V_{OL}	Output Voltage Low	V_{CC}=15V, I_O=100mA			1.4	V
V_{OH}	Output Voltage High	V_{CC}=14V, I_O=100mA	8			V
t_R	Rising Time	V_{CC}=12V, C_L=3nF, 20~80%		80		ns
t_F	Falling Time	V_{CC}=12V, C_L=3nF, 80~20%		40		ns

Continued on the following page…

Electrical Characteristics

Unless otherwise noted, V_{CC}=15V and T_J=-40°C to 125°C. Current is defined as positive into the device and negative out of the device.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Zero Current Detection Section						
V_{ZCD}	Input Threshold Voltage Rising Edge	V_{ZCD} Increasing	1.9	2.1	2.3	V
H_{YS} of V_{ZCD}	Threshold Voltage Hysteresis	V_{ZCD} Decreasing		0.35		V
$V_{ZCD\text{-}HIGH}$	Upper Clamp Voltage	I_{ZCD}=3mA			12	V
$V_{ZCD\text{-}LOW}$	Lower Clamp Voltage	I_{ZCD}=-1.5mA	0.3			V
t_{DEAD}	Maximum Delay, ZCD to Output Turn-On	V_{COMP}=5V, f_{SW}=60KHz	100		400	ns
$t_{RESTART}$	Restart Time	Output Turned Off by ZCD	300	500	700	µs
t_{INHIB}	Inhibit Time (Maximum Switching Frequency Limit)	R_{MOT}=24kΩ		2.8		µs
V_{DIS}	Disable Threshold Voltage		130	200	250	mV
$t_{ZCD\text{-}DIS}$	Disable Function Debounce Time	R_{MOT}=24kΩ, V_{ZCD}=100mV	800			µs
Maximum On Time Section						
V_{MOT}	Maximum On Time Voltage		1.25	1.30	1.35	V
$t_{ON\text{-}MAX}$	Maximum On Time Programming (Resistor Based)	R_{MOT}=24kΩ, V_{CS}=0V, V_{COMP}=5V		25		µs

Typical Performance Characteristics

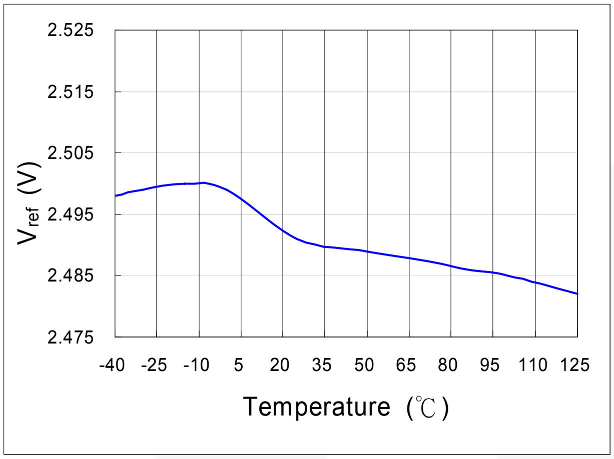


Figure 6. V_{REF} vs. T_A

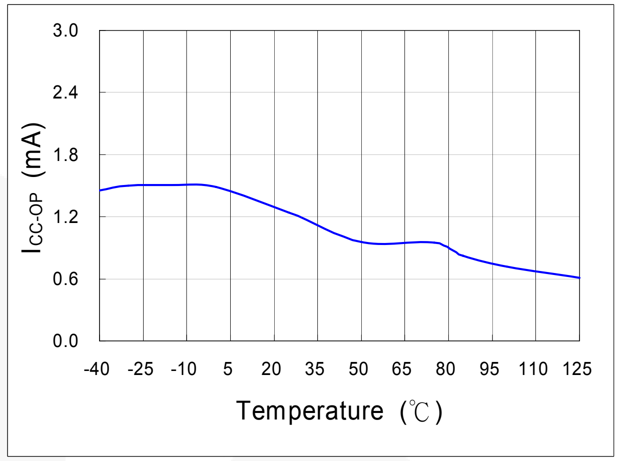


Figure 7. I_{CC-OP} vs. T_A

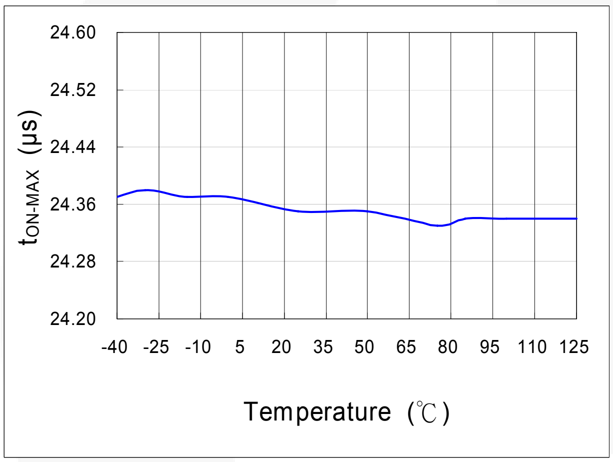


Figure 8. t_{ON-MAX} vs. T_A

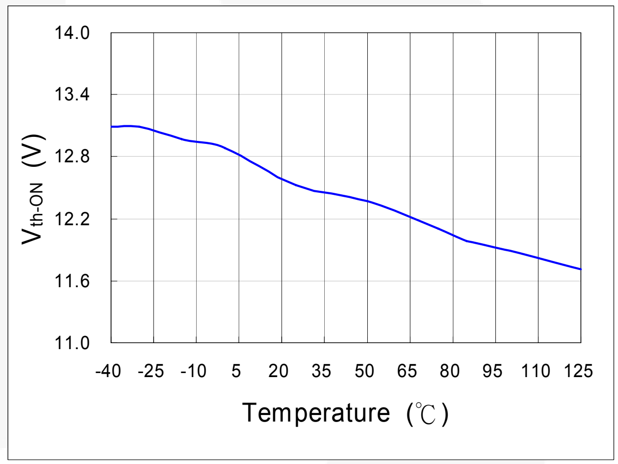


Figure 9. V_{th-ON} vs. T_A

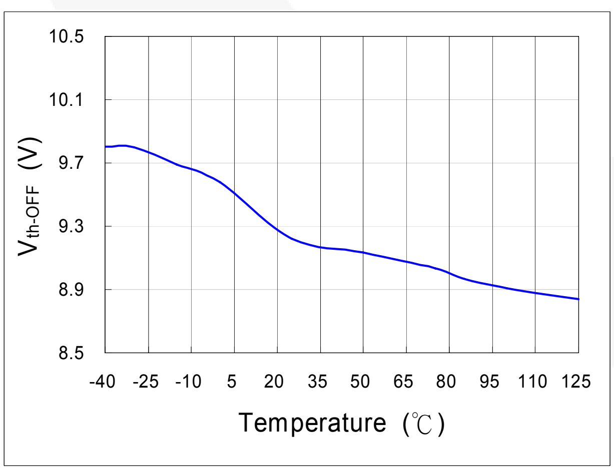


Figure 10. V_{th-OFF} vs. T_A

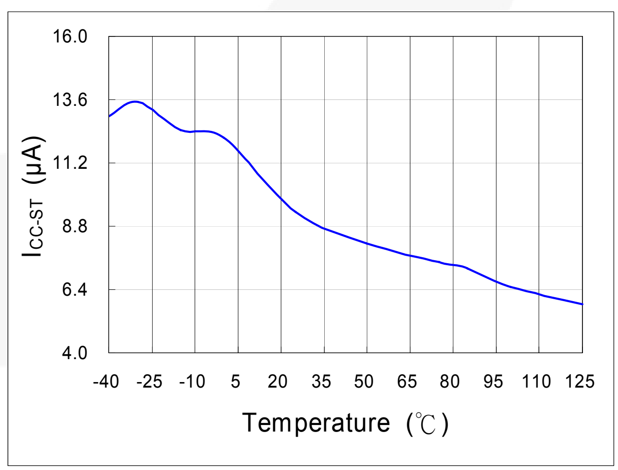


Figure 11. I_{CC-ST} vs. T_A

Typical Performance Characteristics (Continued)

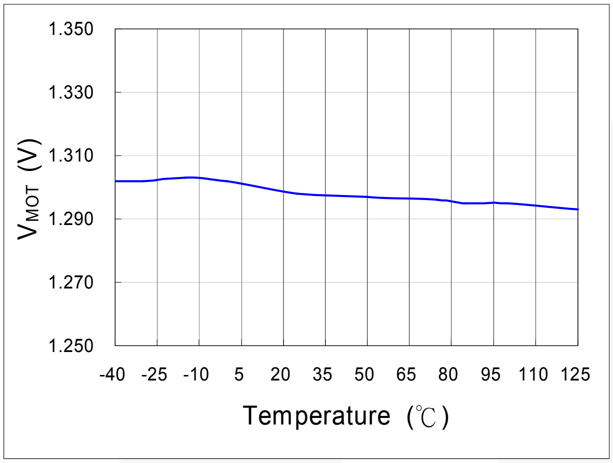


Figure 12. V_{MOT} vs. T_A

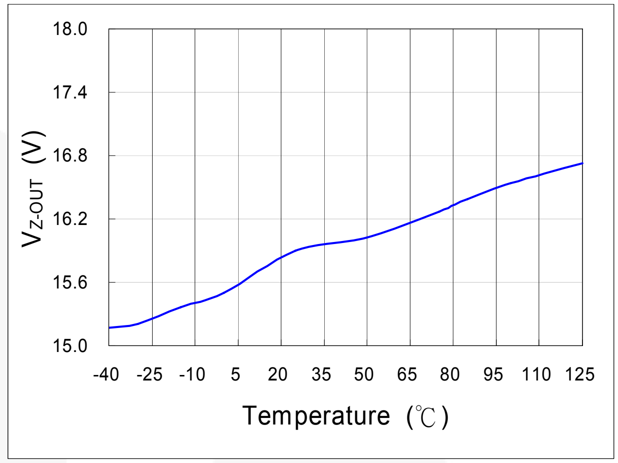


Figure 13. $V_{Z\text{-}OUT}$ vs. T_A

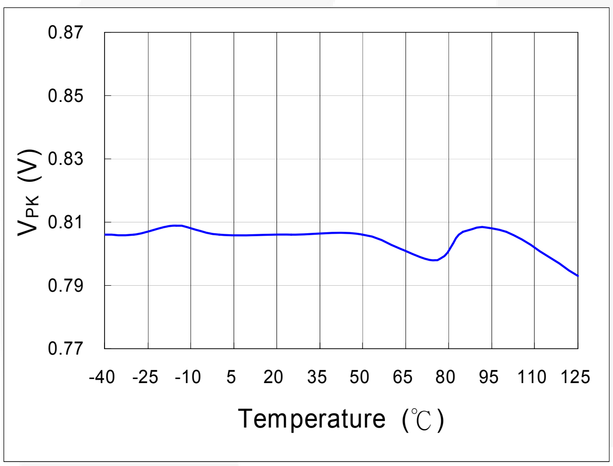


Figure 14. V_{PK} vs. T_A

Functional Description

Error Amplifier

The inverting input of the error amplifier is referenced to INV. The output of the error amplifier is referenced to COMP. The non-inverting input is internally connected to a fixed 2.5V ± 2% voltage. The output of the error amplifier is used to determine the on-time of the PWM output and regulate the output voltage. To achieve a low input current THD, the variation of the on time within one input AC cycle should be very small. A multi-vector error amplifier is built in to provide fast transient response and precise output voltage clamping.

For FL6961, connecting a capacitance, such as 1µF, between COMP and GND is suggested. The error amplifier is a trans-conductance amplifier that converts voltage to current with a 125µmho.

Startup Current

Typical startup current is less than 20µA. This ultra-low startup current allows the usage of high resistance, low-wattage startup resistor. For example, 1MΩ/0.25W startup resistor and a 10µF/25V (V_{CC} hold-up) capacitor are recommended for an AC-to-DC power adaptor with a wide input range 85-265V_{AC}.

Operating Current

Operating current is typically 4.5mA. The low operating current enables a better efficiency and reduces the requirement of V_{CC} hold-up capacitance.

Maximum On-Time Operation

Given a fixed inductor value and maximum output power, the relationship between on-time and line voltage is:

$$t_{on} = \frac{2 \bullet L \bullet P_o}{V_{rms}^2 \bullet \eta} \qquad (1)$$

If the line voltage is too low or the inductor value is too high, t_{ON} is too long. To avoid extra low operating frequency and achieve brownout protection, the maximum value of t_{ON} is programmable by one resistor, R_I, connected between MOT and GND. A 24kΩ resistor R_I generates corresponds to 25µs maximum on time:

$$t_{on(\max)} = R_I(k\Omega) \bullet \frac{25}{24}(\mu s) \qquad (2)$$

The range of the maximum on-time is designed as 10 ~ 50µs.

Peak Current Limiting

The switch current is sensed by one resistor. The signal is feed into CS pin and an input terminal of a comparator. A high voltage in CS pin terminates a switching cycle immediately and cycle-by-cycle current limit is achieved. The designed threshold of the protection point is 0.82V.

Leading-Edge Blanking (LEB)

A turn-on spike on CS pin appears when the power MOSFET is switched on. At the beginning of each switching pulse, the current-limit comparator is disabled for around 400ns to avoid premature termination. The gate drive output cannot be switched off during the blanking period. Conventional RC filtering is not necessary, so the propagation delay of current limit protection can be minimized.

Under-Voltage Lockout (UVLO)

The turn-on and turn-off threshold voltage is fixed internally at 12V/9.5V. This hysteresis behavior guarantees a one-shot startup with proper startup resistor and hold-up capacitor. With an ultra-low startup current of 20µA, one 1MΩ R_{IN} is sufficient for startup under low input line voltage, 85V_{rms}. Power dissipation on R_{IN} would be less than 0.1W even under high line (V_{AC}=265V_{rms}) condition.

Output Driver

With low on resistance and high current driving capability, the output driver can drive an external capacitive load larger than 3000pF. Cross conduction current has been avoided to minimize heat dissipation, improving efficiency and reliability. This output driver is internally clamped by a 16.5V Zener diode.

Zero-Current Detection (ZCD)

The zero-current detection of the inductor is achieved using its auxiliary winding. When the stored energy of the inductor is fully released to output, the voltage on ZCD goes down and a new switching cycle is enabled after a ZCD trigger. The power MOSFET is always turned on with zero inductor current such that turn-on loss and noise can be minimized. The converter works in boundary-mode and peak inductor current is always exactly twice of the average current. A natural power factor correction function is achieved with the low-bandwidth, on-time modulation. An inherent maximum off time is built in to ensure proper start-up operation. This ZCD pin can be used as a synchronous input.

Noise Immunity

Noise on the current sense or control signal can cause significant pulse-width jitter, particularly in the boundary-mode operation. Slope compensation and built-in debounce circuit can alleviate this problem. Because the FL6961 has a single ground pin, high sink current at the output cannot be returned separately. Good high-frequency or RF layout practices should be followed. Avoiding long PCB traces and component leads, locating compensation and filter components near to the FL6961, and increasing the power MOSFET gate resistance improve performance.

Physical Dimensions

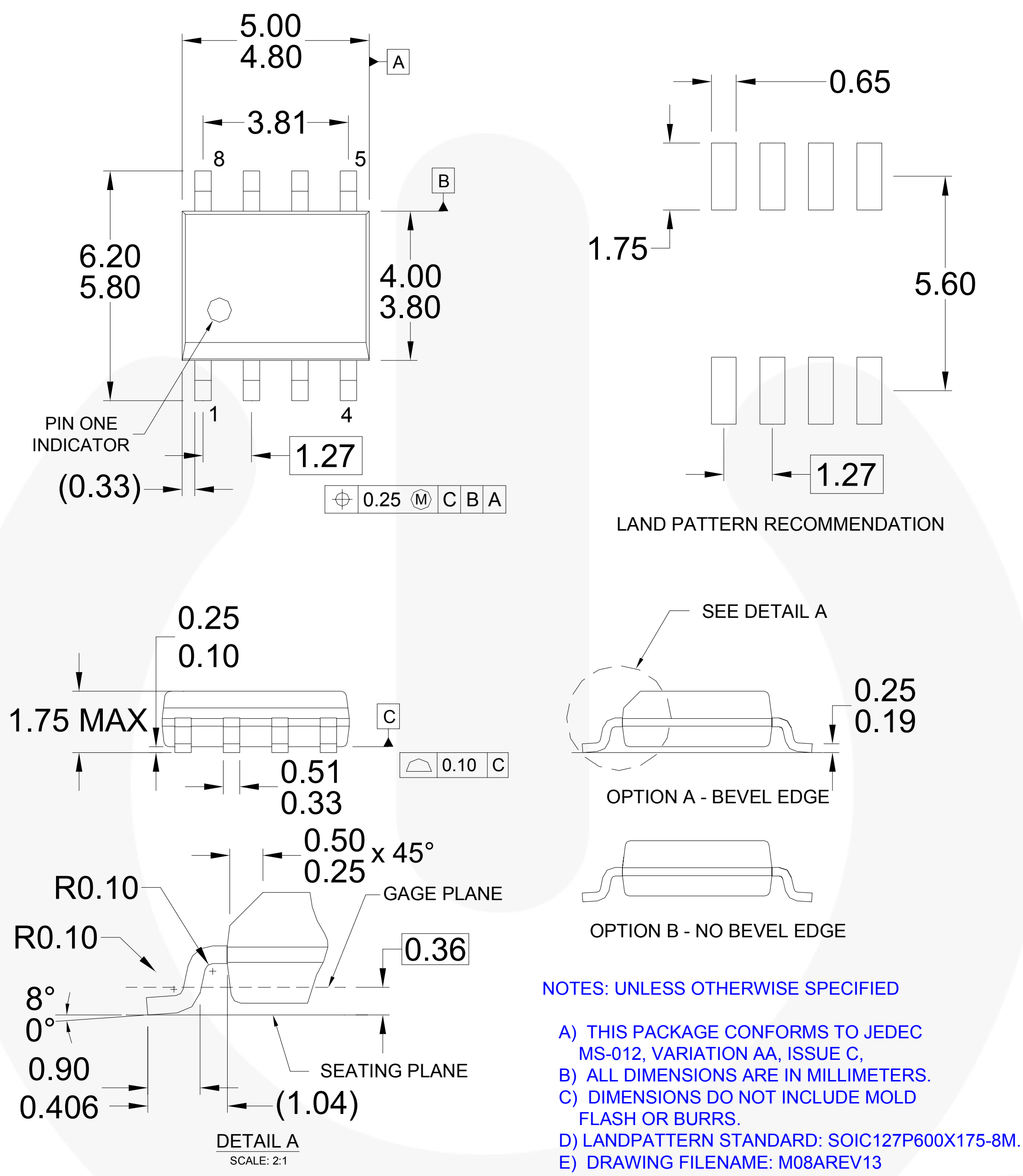


Figure 15. 8-Lead, SOIC,JEDEC MS-012, .150 Inch Narrow Body

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