EN5335QI

3A Voltage Mode Synchronous Buck PWM DC-DC Converter with Integrated Inductor 3-Pin Programmable Output

Description

This Enpirion solution is a Power System on Silicon DC-DC converter. It is specifically designed to meet the precise voltage and fast transient requirements of present and future high-performance, low-power processor, DSP, FPGA, memory boards and system level applications in a distributed power architecture. Advanced circuit techniques, ultra high switching frequency, and very advanced, high-density, integrated circuit and proprietary inductor technology deliver high-quality, ultra compact, non-isolated DC-DC conversion. Operating this converter requires as few as three external components that include small value input and output ceramic capacitors and a soft-start capacitor.

The Enpirion solution significantly helps in system design and productivity by offering greatly simplified board design, layout and manufacturing requirements. In addition, a reduction in the number of vendors required for the complete power solution helps to enable an overall system cost savings.

All Enpirion products are RoHS compliant and lead-free manufacturing environment compatible.

Typical Application Circuit

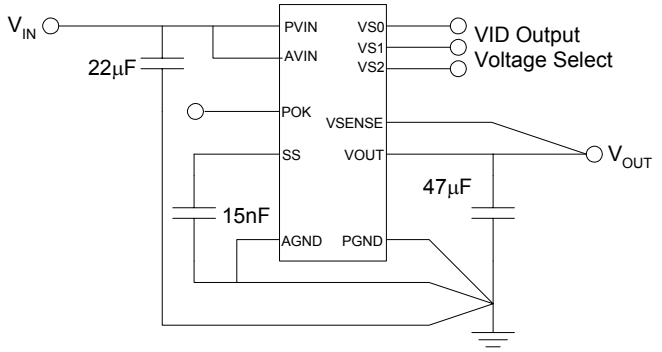


Figure 1. Simple Layout.

Features

- Integrated INDUCTOR, MOSFETS, Controller
- Footprint 1/3rd that of competing solutions.
- Low Part Count: only 3 MLC Capacitors.
- Up to 10W continuous output power.
- 5MHz operating frequency.
- High efficiency, up to 93%.
- V_{OUT} accuracy 2% over line, load and temp.
- Wide input voltage range of 2.375V to 5.5V.
- 3-pin VID output voltage select to chose one of 7 pre-programmed voltage levels.
- Output enable pin and Power OK signal.
- Programmable soft-start time.
- Programmable over-current protection.
- Thermal shutdown, short circuit, over-voltage and under-voltage protection.
- RoHS compliant, MSL level 3, 260C reflow.

Applications

- Point of load regulation for low-power processors, network processors, DSPs, FPGAs, and ASICs
- Notebook computers, servers, workstations
- Broadband, networking, LAN/WAN, optical
- Low voltage, distributed power architectures with 2.5V, 3.3V or 5V rails
- DSL, STB, DVR, DTV, iPC
- Ripple sensitive applications

Ordering Information

Part Number	Temp Rating (°C)	Package
EN5335QI-T	-40 to +85	44-pin QFN T&R
EN5335QI-E	QFN Evaluation Board	

Pin Configuration

Below is a top view diagram of the EN5335QI package.

NOTE: NC pins are not to be electrically connected to each other or to any external signal, ground, or voltage. However, they must be soldered to the PCB. Failure to follow this guideline may result in part malfunction or damage.

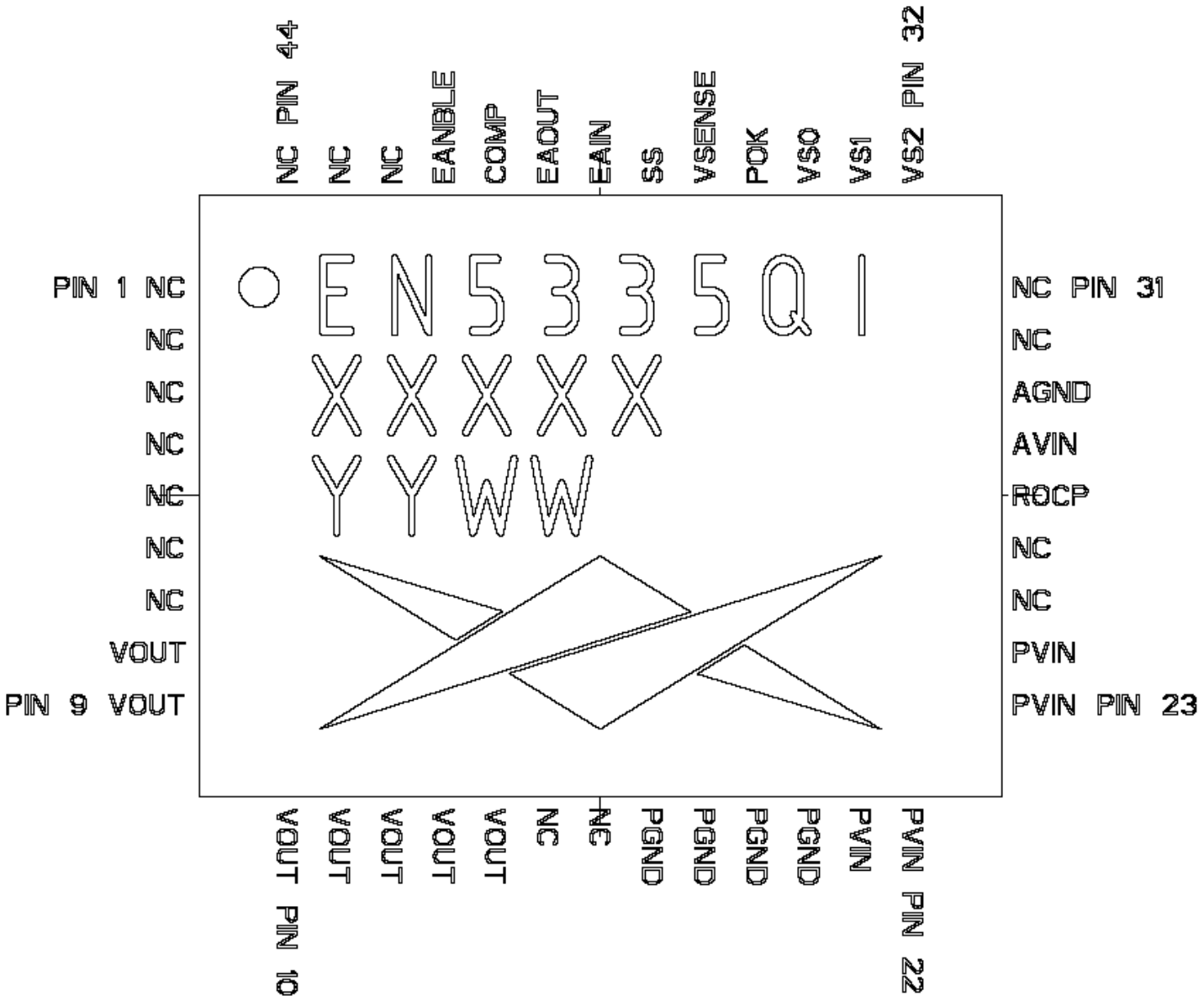


Figure 2. Pin-out diagram, top view.

Pin Descriptions

PIN	NAME	FUNCTION
1-7	NC	NO CONNECT – Do not electrically connect these pins to each other or to PCB. CAUTION!: May be internally connected.
8-14	VOUT	Regulated converter output. Connect these pins to the load and place output capacitor from these pins the PGND pins 17-18
15-16	NC	NO CONNECT – Do not electrically connect these pins to each other or to PCB. CAUTION!: Internally connected to switching node.
17-18	PGND	Output power ground. Connect these pins to the ground electrode of the output filter capacitors. Refer to layout guideline section.
19-20	PGND	Input power ground. Connect these pins to the ground electrode of the Input filter capacitors. Refer to layout guideline section
21-24	PVIN	Input power supply. Connect to input power supply. Decouple with input capacitor to PGND (pins 19-20).
25-26	NC	NO CONNECT – Do not electrically connect these pins to each other or to PCB. CAUTION! May be internally connected.
27	ROCP	Optional Over Current Protection adjust pin. Place ROCP resistor between this pin and AGND (pin 40) to adjust the over current trip point.
28	AVIN	Analog voltage input for the controller circuits. Connect this pin to the input power supply.
29	AGND	Analog ground for the controller circuits.
30-31	NC	NO CONNECT – Do not electrically connect these pins to each other or to PCB. CAUTION! May be internally connected.
32	VS2	Voltage select line 2 input. See Table 1.
33	VS1	Voltage select line 1 input. See Table 1.
34	VS0	Voltage select line 0 input. See Table 1.
35	POK	Power OK is an open drain transistor for power system state indication. POK is a logic high when VOUT is with -10% to +20% of VOUT nominal.
36	VSENSE	Remote voltage sense input. Connect this pin to the load voltage at the point to be regulated.
37	SS	Soft-Start node. The soft-start capacitor is connected between this pin and AGND. The value of this resistor determines the startup timing.
38	EAIN	Optional Error Amplifier input. Allows for customization of the control loop.
39	EAOUT	Optional Error Amplifier output. Allows for customization of the control loop.
40	COMP	Optional Error Amplifier Buffer output. Allows for customization of the control loop.
41	ENABLE	Input Enable. Applying a logic high, enables the output and initiates a soft-start. Applying a logic low disables the output.
42-44	NC	NO CONNECT – Do not electrically connect these pins to each other or to PCB. CAUTION! May be internally connected.

Block Diagram

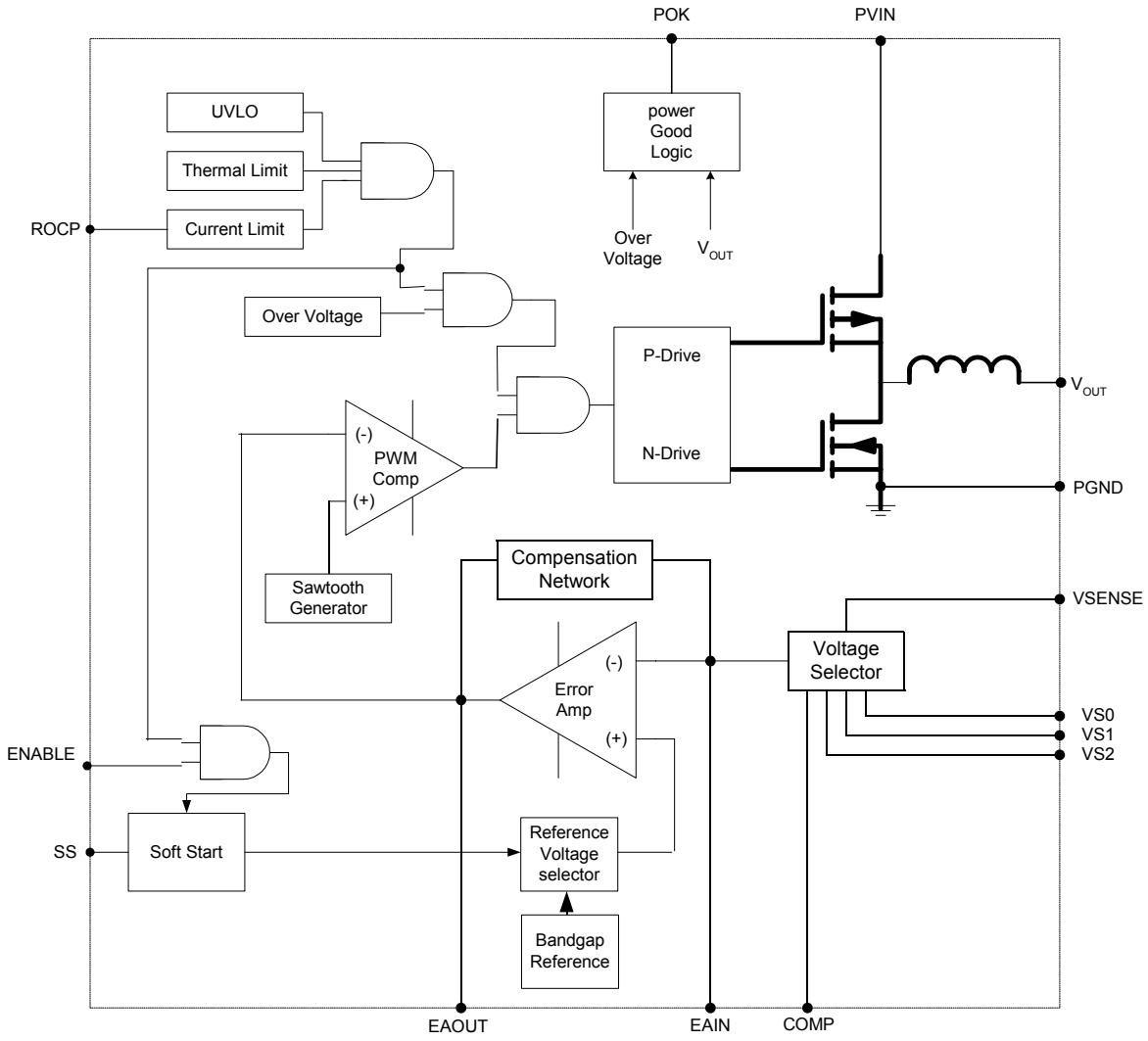


Figure 3. System block diagram.

Absolute Maximum Ratings

CAUTION: Absolute Maximum ratings are stress ratings only. Functional operation beyond recommended operating conditions is not implied. Stress beyond Absolute maximum ratings may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Maximum Electrical Ratings	Min	Max
Voltages on: V_{IN}, V_{OUT}	-0.3V	7.0V
Voltages on: V_{SENSE}	-0.3V	V_{IN} + 0.3V
Voltages on: V_{S0}-V_{S2}	-0.3V	V_{IN} + 0.3V
Voltages on: ENABLE	-0.3V	V_{IN} + 0.3V
Maximum Thermal Ratings		
Ambient operating range	-40°C	+85°C
Storage Temperature Range	-65°C	+150°C
Reflow Peak Body Temperature MSL3 (10 Sec)		+260°C

Thermal Characteristics

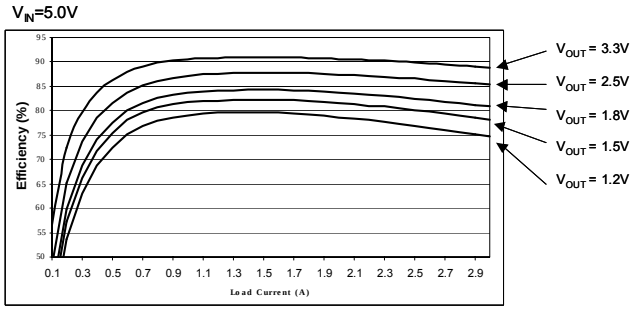
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Operating Junction Temp	T_J	-40		+125	°C
Thermal Shutdown	T_{SD}		150		°C
Thermal Shutdown Hysteresis	T_{SDH}		15		°C
Thermal Resistance: Junction to Case	θ_{JC}		3		°C/W
Thermal Resistance: Junction to Ambient	θ_{JA}		25		°C/W

Electrical Characteristics

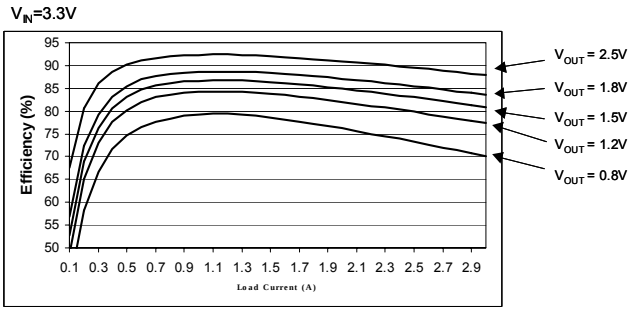
NOTE: V_{IN}=5.5V over operating temperature range unless otherwise noted. Typical values are at T_A = 25°C.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Operating Input Voltage	V_{IN}		2.375		5.5	V
VID Output Voltage Settings	V_{OUT}	VS2 VS1 VS0 0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1		3.3 2.5 1.8 1.5 1.25 1.2 0.8 reserved		V
Shut-Down Supply Current	I_S	ENABLE=0V		100		µA
Switching Frequency	F_{OSC}			5		MHz
Thermal Overload Trip Point	T_J			150		°C
V_{OUT}						
Output Voltage Regulation	V_{OUT}	Over line, load and temperature	-2.0		2.0	%
Maximum Continuous Output Current						
Maximum Continuous Output Current	$I_{OUT\_Max\_Cont}$		3			A
Over Current Trip Piont	I_{OCP}		4.5			A
Enable Operation						
Disable Threshold	$V_{DISABLE}$	Max voltage to ensure the converter is disabled			0.8	V
Enable Threshold	V_{ENABLE}	2.375V ≤ V_{IN} ≤ 5.5V 5.5V < V_{IN}	1.8 2.0			V
Voltage Select Operation						
Logic Low Threshold	$V_{SX\text{-}Low}$	Threshold voltage for Logic Low			0.8	V
Logic High Threshold	$V_{SX\text{-}High}$	Threshold voltage for Logic High (internally pulled high; can be left floating to achieve logic high)	1.8		V_{IN}	V
Power OK Operation						
POK low voltage	V_{POK}				0.4	V
Max POK Voltage	V_{POK}				5.5	V

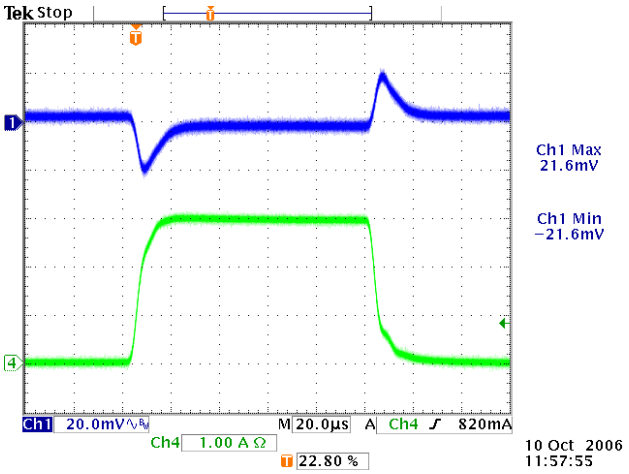
Typical Performance Characteristics



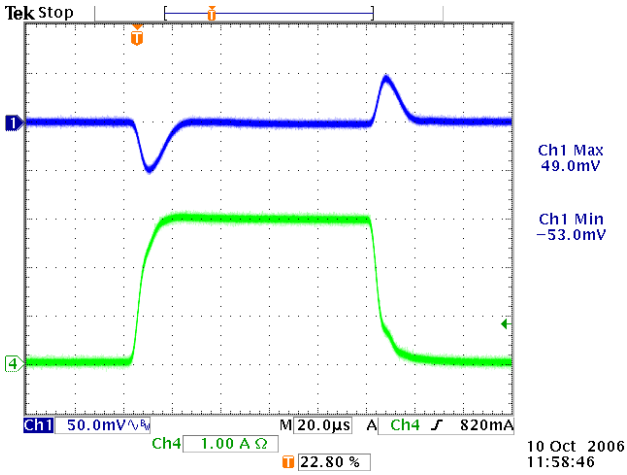
Efficiency versus Load, V_{IN} = 5.0V



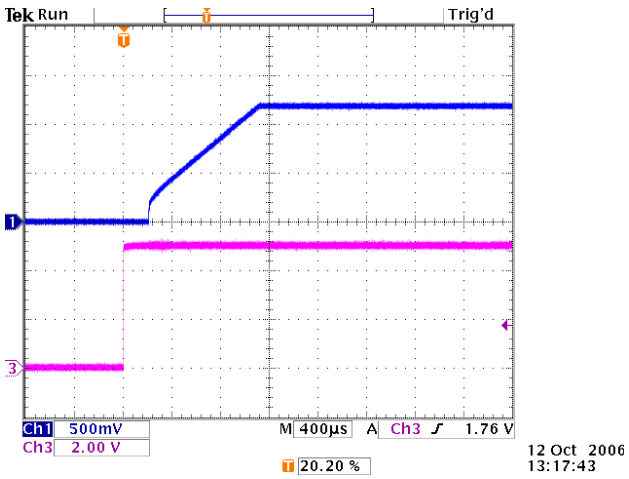
Efficiency versus Load, V_{IN} = 3.3V



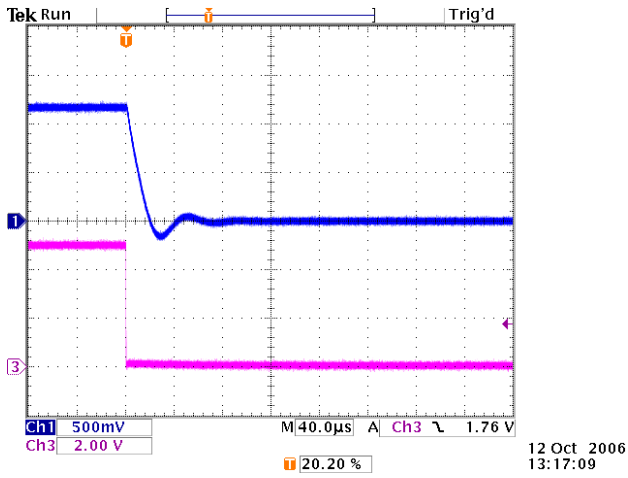
Load transient, 0 – 3A, V_{IN}/V_{OUT} = 5.5V/1.2V



Load transient, 0 – 3A, V_{IN}/V_{OUT} = 5.5V/3.3V



Start-up waveform, V_{IN}/V_{OUT} = 5.5V/1.2V



Shut-down waveform, V_{IN}/V_{OUT} = 5.5V/1.2V

Theory of Operation

Synchronous Buck Converter

The EN5335QI is a synchronous, pin programmable power supply with integrated power MOSFET switches and integrated inductor. The nominal input voltage range is 2.4-5.0V. The output can be set to common pre-set voltages by connecting appropriate combinations of 3 voltage selection pins to ground. The feedback control loop is a type III voltage-mode and the part uses a low-noise PWM topology. Up to 3A of output current can be drawn from this converter. The 5MHz operating frequency enables the use of small-size output capacitors.

The power supply has the following protection features:

- Programmable over-current protection (to protect the IC from excessive load current)
- Thermal shutdown with hysteresis.
- Over-voltage protection
- Under-voltage lockout circuit to disable the converter output when the input voltage is less than approximately 2.2V

Additional features include:

- Soft-start circuit, limiting the in-rush current when the converter is powered up.

Power good circuit indicating whether the output voltage is within 90%-120% of the programmed voltage.

Output Voltage Programming

The EN5335QI output voltage is programmed using a 3-pin voltage-ID or VID selector. Three binary VID pins allow the user to choose one of seven pre-set voltages. Refer to Table 1 for the proper VID pin settings to choose VOUT.

The voltage select pins, VS0, VS1, and VS2, are pulled-up internally and so will default to a logic high, or “1”, if left “open”. Connecting the voltage select pin to ground will result in a logic “0”.

Table 1: Output Voltage Select Table

VS2*	VS1*	VS0*	Output Voltage
0	0	0	3.3V
0	0	1	2.5V
0	1	0	1.8V
0	1	1	1.5V
1	0	0	1.25V
1	0	1	1.2V
1	1	0	0.8V
1	1	1	Reserved

Input Capacitor Selection

The EN5335QI requires between 10uF and 20uF of input capacitance. Low-cost, low-ESR ceramic capacitors should be used as input capacitors for this converter. The dielectric must be X5R or X7R rated. In some applications, lower value capacitors are needed in parallel with the larger, capacitors in order to provide high frequency decoupling. It is recommended to use 10V rated 1210 MLCC capacitors.

Table 2. Recommended input capacitors.

Description	MFG	P/N
22uF, 10V, X7R, 1210	Murata	GRM32ER71A226KE20L
	Taiyo Yuden	LMK325BJ226KM-T
47uF, 10V, X5R, 1210	Murata	GRM32ER71A476KE20L
	Taiyo Yuden	LMK325BJ476KM-T

Output Capacitor Selection

The EN5335QI has been optimized for use with approximately 47µF of output capacitance. Low ESR ceramic capacitors are required with X5R or X7R rated dielectric formulation. Y5V or equivalent dielectric formulations must not be used as these loose capacitance with frequency, temperature and bias voltage.

Output ripple voltage is determined by the aggregate output capacitor impedance. Output

impedance, denoted as Z, is comprised of effective series resistance, ESR, and effective series inductance, ESL:

Z = ESR + ESL.

Placing output capacitors in parallel reduces the impedance and will hence result in lower ripple voltage.

$$\frac{1}{Z_{Total}} = \frac{1}{Z_1} + \frac{1}{Z_2} + ... + \frac{1}{Z_n}$$

Typical ripple versus capacitance is given below:

Output Capacitor Configuration	Typical Output Ripple (mVp-p) (as measured on EN5335QI Evaluation Board)
1 x 47uF	20
5 x 10 uF	10

Table 3. Recommended output capacitors.

Description	MFG	P/N
10uF, 6.3V, X7R, 1206	Murata	GRM319R60J106KE19D
	Taiyo Yuden	LMK316BJ106KD-T
22uF, 6.3V, X5R, 1206	Murata	GRM31CR60J226KE19L
	Taiyo Yuden	LMK316BJ226KL-T
47uF, 6.3V, X5R, 1206	Murata	GRM31CR71A476ME19L
	Taiyo Yuden	LMK316BJ476KL-T

Enable Operation

The ENABLE pin provides a means to shut down the device, or enable normal operation. A logic low will disable the converter and cause it to shut down. A logic high will enable the converter into normal operation. When the ENABLE pin is asserted high, the device will undergo a normal soft start.

Soft-Start Operation

Soft start is a method to reduce in-rush current when the device is enabled. The output voltage is ramped up slowly upon start-up. The output rise time is controlled by choice of a soft-start capacitor, which is placed between the SS pin (pin 37) and the AGND pin (pin 29).

Rise Time: $T_R = C_{ss} * 80K\Omega$

During start-up of the converter, the reference voltage to the error amplifier is gradually increased to its final level by an internal current source of typically 10uA. Typical soft-start rise time is 1mS to 3mS. Typical SS capacitor values are in the range of 15nF to 30 nF.

POK Operation

The POK signal is an open drain signal from the converter indicating the output voltage is within the specified range. The POK signal will be a logic high when the output voltage is within 90% - 120% of the programmed output voltage. If the output voltage goes outside of this range, the POK signal will be a logic low until the output voltage has returned to within this range. In the event of an over-voltage condition the POK signal will go low and will remain in this condition until the output voltage has dropped to 95% of the programmed output voltage before returning to the high state (see also: Over Voltage Protection)

Over-Current Protection

The current limit function is achieved by sensing the current flowing through the sense P-MOSFET. When the sensed current exceeds the current limit, both NFET and PFET switches are turned off. If the over-current condition is removed, the over-current protection circuit will enable the PWM operation. If the over-current condition persists, the soft start capacitor will eventually discharge and cause the converter to go through a full soft-start cycle. This circuit is designed to provide high noise immunity.

It is possible to adjust the over-current set point by connecting a resistor between ROCP (pin 27) and GND (increase the trip point) or PVIN (decrease the trip point). The nominal over current trip point is set to 4.5A. The voltage at the ROCP pin is designed to be 0.8V.

In some cases, such as the start-up of FPGA devices, it is desirable to blank the over-current protection feature. In order to disable over-current protection, the ROCP pin should be tied to PVIN.

Over-Voltage Protection

When the output voltage exceeds 120% of the programmed output voltage, the PWM operation stops, the lower N-MOSFET is turned on and the POK signal goes low. When the output voltage drops below 95% of the programmed output voltage, normal PWM operation resumes and POK returns to its high state.

Thermal Overload Protection

Thermal shutdown will disable operation once the Junction temperature exceeds approximately 150ºC. Once the junction temperature drops by approx 25ºC, the converter will re-start with a normal soft-start.

Input Under-voltage Lock-out

Circuitry is provided to ensure that when the input voltage is below the specified voltage range, the converter will not start-up. Circuits for hysteresis, input de-glitch and output leading edge blanking are included to ensure high noise immunity and prevent false tripping.

Compensation

The EN5335QI is internally compensated through the use of a type 3 compensation network and is optimized for use with about 47µF of output capacitance and will provide excellent loop bandwidth and transient performance for most applications. (See the section on Capacitor Selection for details on recommended capacitor types.) Voltage mode operation provides high noise immunity at light load.

In some cases modifications to the compensation may be required. For more information, contact Enpirion Applications Engineering support.

Design Considerations for Lead-Frame Based Modules

Exposed Metal on Bottom Of Package

Lead frame offers many advantages in thermal performance, in reduced electrical lead resistance, and in overall foot print. However, they do require some special considerations.

In the assembly process lead frame construction requires that, for mechanical support, some of the lead-frame cantilevers be exposed at the point where wire-bond or internal passives are attached. This results in several small pads being exposed on the bottom of the package.

Only the large thermal pad and the perimeter pads are to be mechanically or electrically connected to the PC board. The PCB top layer under the EN5335QI should be clear of any metal except for the large thermal pad. The “grayed-out” area in Figure 4 represents the area that should be clear of any metal (traces, vias, or planes), on the top layer of the PCB.

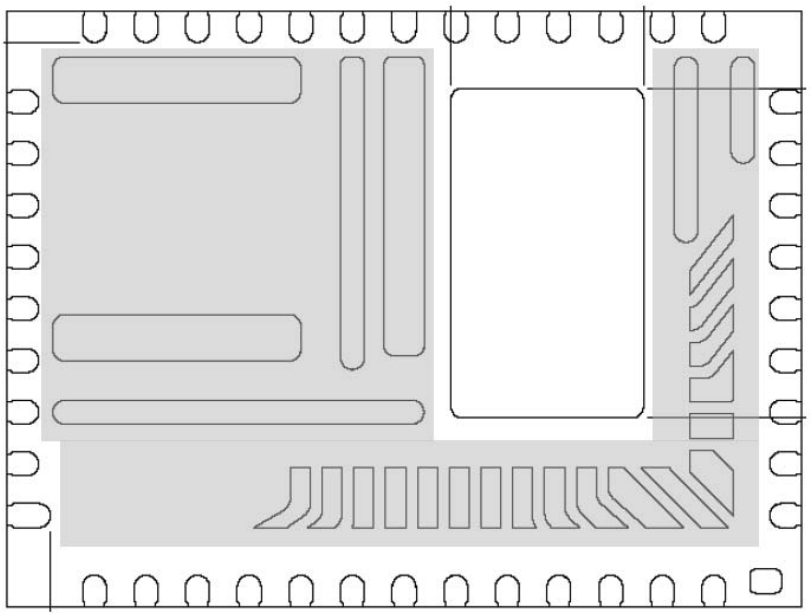


Figure 4. Lead-Frame exposed metal. Grey area highlights exposed metal that is not to be mechanically or electrically connected to the PWB.

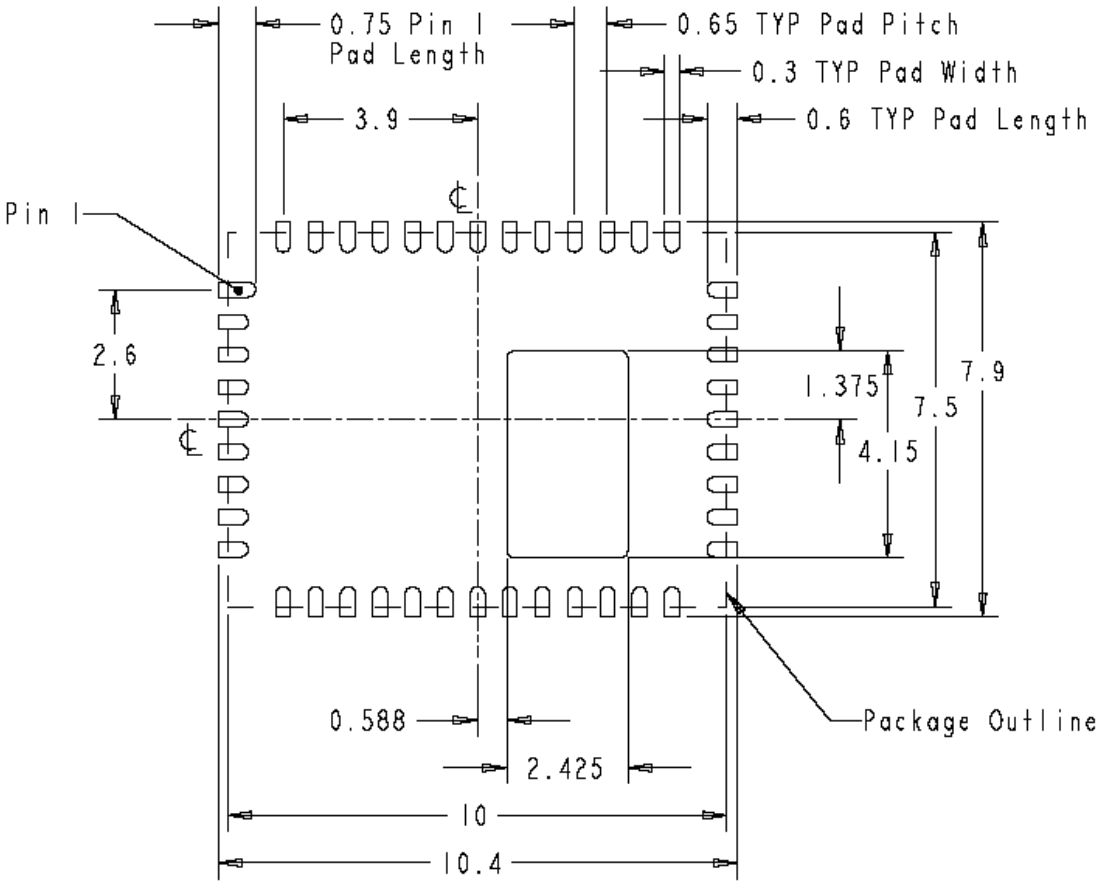


Figure 5. Recommended solder mask opening for PWB.

Package Dimensions

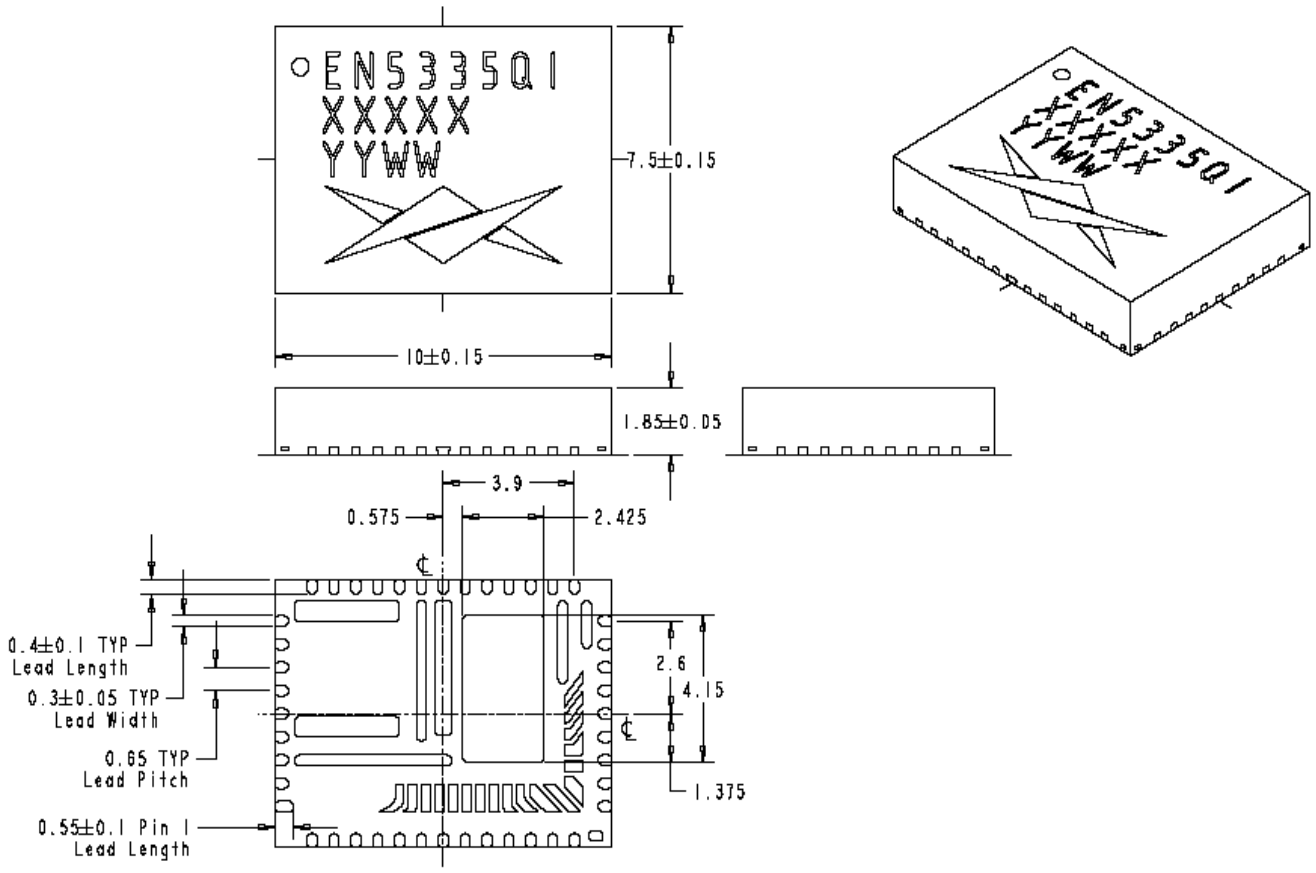


Figure 6. Package dimensions.

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