

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC7MET573AFK

Octal D-Type Latch with 3-State Output

The TC7MET573AFK is an advanced high speed CMOS octal latch with 3-state output fabricated with silicon gate C²MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

This 8-bit D-type latch is controlled by a latch enable input (LE) and an output enable input (\overline{OE}).

When the \overline{OE} input is high, the eight outputs are in a high impedance state.

The input voltage are compatible with TTL output voltage.

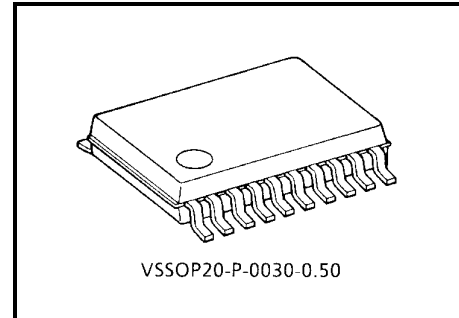
This device may be used as a level converter for interfacing 3.3 V to 5 V system.

Input protection and output circuit ensure that 0 to 5.5 V can be applied to the input and output (^{Note}) pins without regard to the supply voltage. These structure prevents device destruction due to mismatched supply and input/output voltages such as battery back up, hot board insertion, etc.

Note: $V_{CC} = 0\text{ V}$

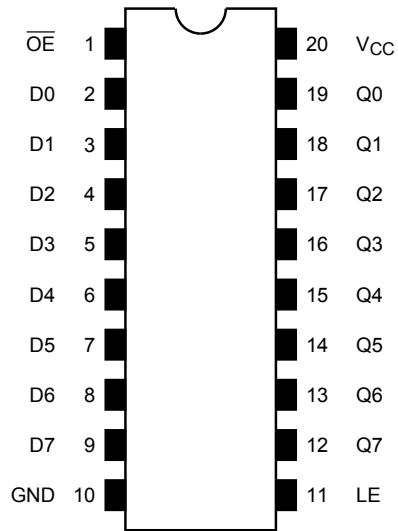
Features

- High speed: $t_{pd} = 7.7\text{ ns}$ (typ.) ($V_{CC} = 5\text{ V}$)
- Low power dissipation: $I_{CC} = 4\text{ }\mu\text{A}$ (max) ($T_a = 25^\circ\text{C}$)
- Compatible with TTL outputs: $V_{IL} = 0.8\text{ V}$ (max)
 $V_{IH} = 2.0\text{ V}$ (min)
- Power down protection is provided on all inputs and outputs.
- Balanced propagation delays: $t_{pLH} \approx t_{pHL}$
- Low noise: $V_{OLP} = 1.5\text{ V}$ (max)
- Pin and function compatible with the 74 series (74AC/HC/F/ALS/LS etc.) 573 type.

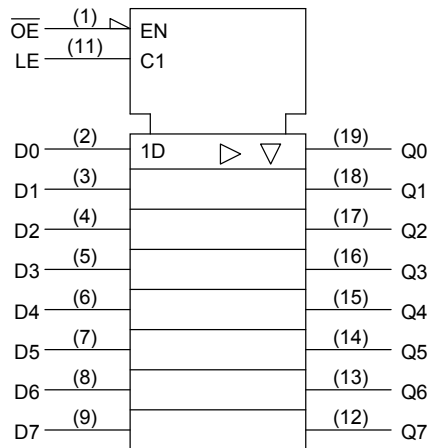


Weight: 0.03 g (typ.)

Pin Assignment (top view)



IEC Logic Symbol



Truth Table

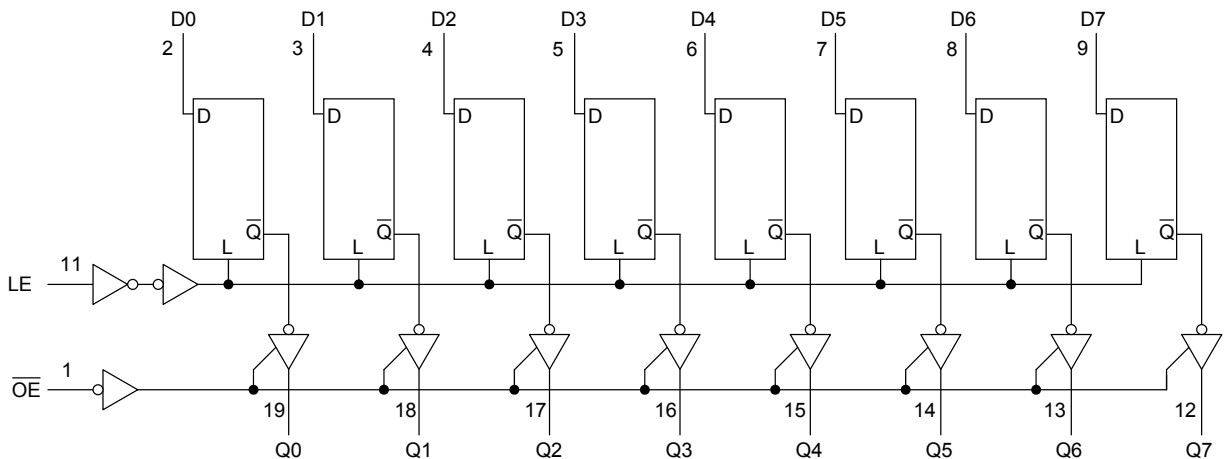
| Inputs | | | Outputs |
|-----------------|----|---|---------|
| \overline{OE} | LE | D | |
| H | X | X | Z |
| L | L | X | Q_n |
| L | H | L | L |
| L | H | H | H |

X: Don't care

Z: High impedance

Q_n : Q outputs are latched at the time when the LE input is taken to a low logic level.

System Diagram



Absolute Maximum Ratings (Note 1)

| Characteristics | Symbol | Rating | Unit |
|-----------------------------|-----------|-------------------------------|------|
| Supply voltage range | V_{CC} | -0.5~7.0 | V |
| DC input voltage | V_{IN} | -0.5~7.0 | V |
| DC output voltage | V_{OUT} | -0.5~7.0 (Note 2) | V |
| | | -0.5~ $V_{CC} + 0.5$ (Note 3) | |
| Input diode current | I_{IK} | -20 | mA |
| Output diode current | I_{OK} | ±20 (Note 4) | mA |
| DC output current | I_{OUT} | ±25 | mA |
| DC V_{CC} /ground current | I_{CC} | ±75 | mA |
| Power dissipation | P_D | 180 | mW |
| Storage temperature | T_{stg} | -65~150 | °C |

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: Output is off-state

Note 3: High or low state. I_{OUT} absolute maximum rating must be observed.

Note 4: $V_{OUT} < GND$, $V_{OUT} > V_{CC}$

Operating Ranges (Note 1)

| Characteristics | Symbol | Rating | Unit |
|--------------------------|-----------|----------------------|------|
| Supply voltage | V_{CC} | 4.5~5.5 | V |
| Input voltage | V_{IN} | 0~5.5 | V |
| Output voltage | V_{OUT} | 0~5.5 (Note 2) | V |
| | | 0~ V_{CC} (Note 3) | |
| Operating temperature | T_{opr} | -40~85 | °C |
| Input rise and fall time | dt/dv | 0~20 | ns/V |

Note 1: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either V_{CC} or GND.

Note 2: Output in off state

Note 3: High or low state

Electrical Characteristics

DC Characteristics

| Characteristics | | Symbol | Test Condition | Ta = 25°C | | | Ta = -40~85°C | | Unit | | |
|----------------------------------|------------|-------------------|---------------------------------------------------------------------------------------------------|--------------------------|-----|------|---------------|------|-------|------|---|
| | | | | V _{CC} (V) | Min | Typ. | Max | Min | | Max | |
| Input voltage | High level | V _{IH} | — | 4.5~5.5 | 2.0 | — | — | 2.0 | — | V | |
| | Low level | V _{IL} | — | 4.5~5.5 | — | — | 0.8 | — | 0.8 | | |
| Output voltage | High level | V _{OH} | V _{IN} = V _{IH} or V _{IL} | I _{OH} = -50 μA | 4.5 | 4.4 | 4.5 | — | 4.4 | — | V |
| | | | | I _{OH} = -8 mA | 4.5 | 3.94 | — | — | 3.80 | — | |
| | Low level | V _{OL} | V _{IN} = V _{IH} or V _{IL} | I _{OL} = 50 μA | 4.5 | — | 0 | 0.1 | — | 0.1 | |
| | | | | I _{OL} = 8 mA | 4.5 | — | — | 0.36 | — | 0.44 | |
| 3-state output off-state current | | I _{OZ} | V _{IN} = V _{IH} or V _{IL} V _{OUT} = V _{CC} or GND | 5.5 | — | — | ±0.25 | — | ±2.50 | μA | |
| Input leakage current | | I _{IN} | V _{IN} = 5.5 V or GND | 0~5.5 | — | — | ±0.1 | — | ±1.0 | μA | |
| Quiescent supply current | | I _{CC} | V _{IN} = V _{CC} or GND | 5.5 | — | — | 4.0 | — | 40.0 | μA | |
| | | I _{CCCT} | Per input: V _{IN} = 3.4 V Other input: V _{CC} or GND | 5.5 | — | — | 1.35 | — | 1.50 | mA | |
| Output leakage current | | I _{OPD} | V _{OUT} = 5.5 V | 0 | — | — | 0.5 | — | 5.0 | μA | |

Timing Requirements (Input: t_r = t_f = 3 ns)

| Characteristics | Symbol | Test Condition | Ta = 25°C | | Ta = -40~85°C | | Unit |
|-----------------------------|------------------------------------------|----------------|---------------------|------|---------------|-------|------|
| | | | V _{CC} (V) | Typ. | Limit | Limit | |
| Minimum pulse width (LE) | t _w (H) t _w (L) | — | 5.0 ± 0.5 | — | 6.5 | 8.5 | ns |
| Minimum set-up time | t _s | — | 5.0 ± 0.5 | — | 1.5 | 1.5 | ns |
| Minimum hold time | t _h | — | 5.0 ± 0.5 | — | 3.5 | 3.5 | ns |

AC Characteristics (Input: $t_r = t_f = 3$ ns)

| Characteristics | Symbol | Test Condition | Ta = 25°C | | | Ta = -40~85°C | | Unit | | |
|-------------------------------|----------------------------------------|-----------------------|---------------------|---------------------|-----|---------------|------|------|------|-----|
| | | | V _{CC} (V) | C _L (pF) | Min | Typ. | Max | | Min | Max |
| Propagation delay time (LE-Q) | t _{pLH} t _{pHL} | — | 5.0 ± 0.5 | 15 | — | 7.7 | 12.3 | 1.0 | 13.5 | ns |
| | | | | 50 | — | 8.5 | 13.3 | 1.0 | 14.5 | |
| Propagation delay time (D-Q) | t _{pLH} t _{pHL} | — | 5.0 ± 0.5 | 15 | — | 5.1 | 8.5 | 1.0 | 9.5 | ns |
| | | | | 50 | — | 5.9 | 9.5 | 1.0 | 10.5 | |
| 3-state output enable time | t _{pZL} t _{pZH} | R _L = 1 kΩ | 5.0 ± 0.5 | 15 | — | 6.3 | 10.9 | 1.0 | 12.5 | ns |
| | | | | 50 | — | 7.1 | 11.9 | 1.0 | 13.5 | |
| 3-state output disable time | t _{pLZ} t _{pHZ} | R _L = 1 kΩ | 5.0 ± 0.5 | 50 | — | 8.8 | 11.2 | 1.0 | 12.0 | ns |
| Output to output skew | t _{osLH} t _{osHL} | (Note 1) | 5.0 ± 0.5 | 50 | — | — | 1.0 | — | 1.0 | ns |
| Input capacitance | C _{IN} | — | — | — | — | 4 | 10 | — | 10 | pF |
| Output capacitance | C _{OUT} | — | — | — | — | 9 | — | — | — | pF |
| Power dissipation capacitance | C _{PD} | — | — | (Note 2) | — | 25 | — | — | — | pF |

Note 1: Parameter guaranteed by design.

$$t_{osLH} = |t_{pLHm} - t_{pLHn}|, t_{osHL} = |t_{pHLm} - t_{pHLn}|$$

Note 2: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{ (per latch)}$$

And the total C_{PD} when n pcs. of latch operate can be gained by the following equation:

$$C_{PD (total)} = 14 + 11 \cdot n$$

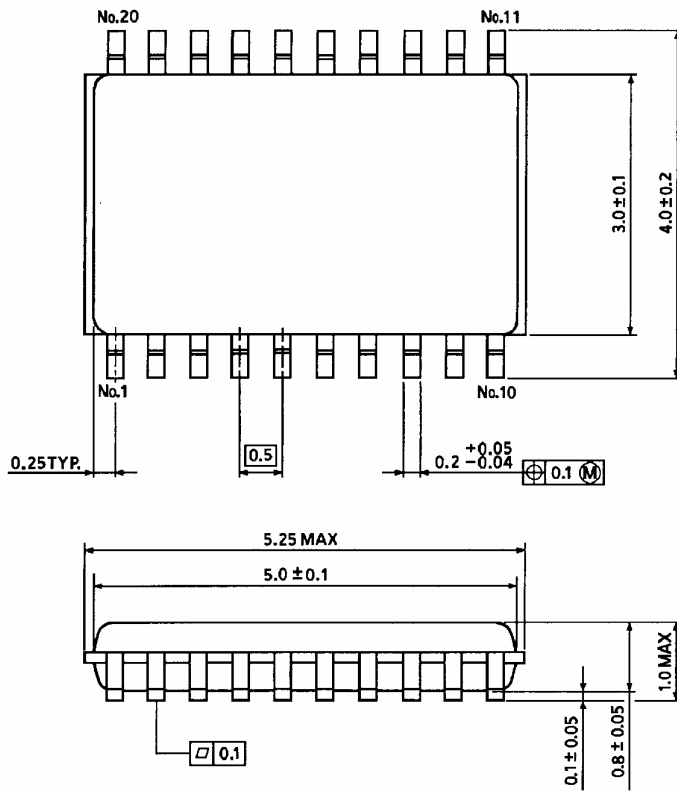
Noise Characteristics (Input: $t_r = t_f = 3$ ns)

| Characteristics | Symbol | Test Condition | Ta = 25°C | | | Unit |
|----------------------------------------------------------|------------------|------------------------|---------------------|------|-------|------|
| | | | V _{CC} (V) | Typ. | Limit | |
| Quiet output maximum dynamic V _{OL} | V _{OLP} | C _L = 50 pF | 5.0 | 1.1 | 1.5 | V |
| Quiet output minimum dynamic V _{OL} | V _{OLV} | C _L = 50 pF | 5.0 | -1.1 | -1.5 | V |
| Minimum high level dynamic input voltage V _{IH} | V _{IHD} | C _L = 50 pF | 5.0 | — | 2.0 | V |
| Maximum low level dynamic input voltage V _{IL} | V _{ILD} | C _L = 50 pF | 5.0 | — | 0.8 | V |

Package Dimensions

VSSOP20-P-0030-0.50

Unit : mm



Weight: 0.03 g (typ.)

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20070701-EN GENERAL

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