

TC7MH573FK

Octal D-Type Latch with 3-State Output

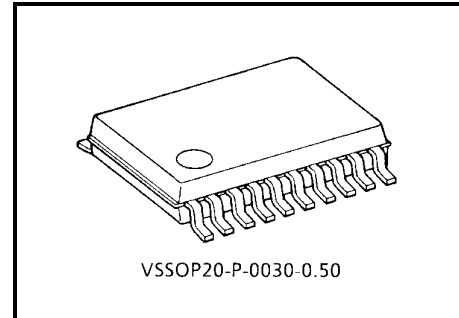
The TC7MH573FK is an advanced high speed CMOS octal latch with 3-state output fabricated with silicon gate C²MOS technology.

It achieves the high speed operation similar to equivalent bipolar schottky TTL while maintaining the CMOS low power dissipation.

This 8 bit D-type latch is controlled by a latch enable input (LE) and an output enable input (\overline{OE}).

When the \overline{OE} input is high, the eight outputs are in a high impedance state.

An input protection circuit ensures that 0 to 5.5 V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5 V to 3 V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

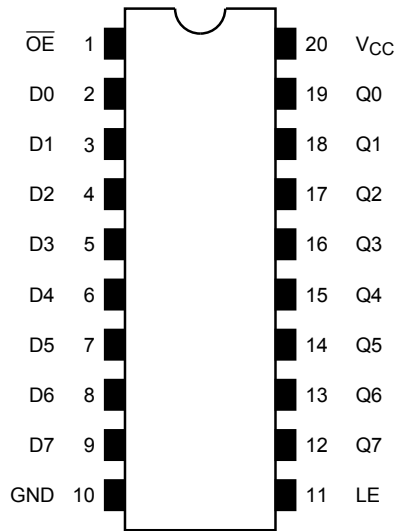


Weight: 0.03 g (typ.)

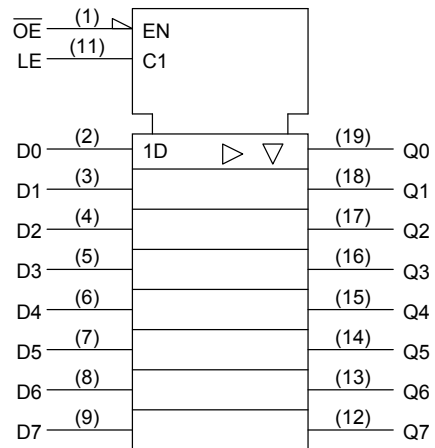
Features

- High speed: $t_{pd} = 4.5$ ns (typ.) ($V_{CC} = 5$ V)
- Low power dissipation: $I_{CC} = 4$ μ A (max) ($T_a = 25^\circ\text{C}$)
- High noise immunity: $V_{NIH} = V_{NIL} = 28\%$ V_{CC} (min)
- Power down protection is provided on all inputs.
- Balanced propagation delays: $t_{pLH} \approx t_{pHL}$
- Wide operating voltage range: $V_{CC}(\text{opr}) = 2\sim 5.5$ V
- Low noise: $V_{OLP} = 1.0$ V (max)
- Pin and function compatible with 74ALS573

Pin Assignment (top view)



IEC Logic Symbol



Truth Table

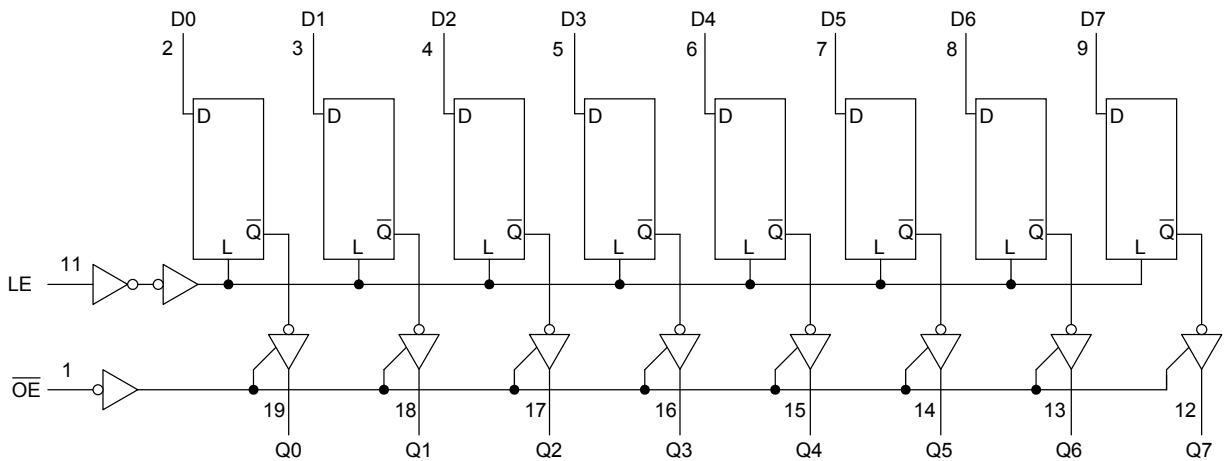
Inputs			Outputs
\overline{OE}	LE	D	
H	X	X	Z
L	L	X	Q_n
L	H	L	L
L	H	H	H

X: Don't care

Z: High impedance

Q_n : Q outputs are latched at the time when the LE input is taken to a low logic level.

System Diagram



Absolute Maximum Ratings (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V _{CC}	-0.5~7.0	V
DC input voltage	V _{IN}	-0.5~7.0	V
DC output voltage	V _{OUT}	-0.5~V _{CC} + 0.5	V
Input diode current	I _{IK}	-20	mA
Output diode current	I _{OK}	±20	mA
DC output current	I _{OUT}	±25	mA
DC V _{CC} /ground current	I _{CC}	±75	mA
Power dissipation	P _D	180	mW
Storage temperature	T _{stg}	-65~150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V _{CC}	2.0~5.5	V
Input voltage	V _{IN}	0~5.5	V
Output voltage	V _{OUT}	0~V _{CC}	V
Operating temperature	T _{opr}	-40~85	°C
Input rise and fall time	dt/dv	0~100 (V _{CC} = 3.3 ± 0.3 V)	ns/V
		0~20 (V _{CC} = 5 ± 0.5 V)	

Note: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either V_{CC} or GND.

Electrical Characteristics

DC Characteristics

Characteristics		Symbol	Test Condition	Ta = 25°C			Ta = -40~85°C		Unit		
				V _{CC} (V)	Min	Typ.	Max	Min		Max	
Input voltage	High level	V _{IH}	—	2.0	1.50	—	—	1.50	V		
				3.0~5.5	V _{CC} × 0.7	—	—	V _{CC} × 0.7		—	
	Low level	V _{IL}	—	2.0	—	—	0.50	—		0.50	
				3.0~5.5	—	—	V _{CC} × 0.3	—		V _{CC} × 0.3	
Output voltage	High level	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -50 μA	2.0	1.9	2.0	—	1.9	V	
					3.0	2.9	3.0	—	2.9		—
				I _{OH} = -4 mA	4.5	4.4	4.5	—	4.4		—
					3.0	2.58	—	—	2.48		—
	Low level	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 50 μA	2.0	—	0	0.1	—		0.1
					3.0	—	0	0.1	—		0.1
				I _{OL} = 4 mA	4.5	—	0	0.1	—		0.1
					3.0	—	—	0.36	—		0.44
				I _{OL} = 8 mA	4.5	—	—	0.36	—		0.44
					3.0	—	—	0.36	—		0.44
3-state output off-state current		I _{OZ}	V _{IN} = V _{IH} or V _{IL} V _{OUT} = V _{CC} or GND	5.5	—	—	±0.25	—	±2.50	μA	
Input leakage current		I _{IN}	V _{IN} = 5.5 V or GND	0~5.5	—	—	±0.1	—	±1.0	μA	
Quiescent supply current		I _{CC}	V _{IN} = V _{CC} or GND	5.5	—	—	4.0	—	40.0	μA	

Timing Requirements (Input: t_r = t_f = 3 ns)

Characteristics	Symbol	Test Condition	Ta = 25°C		Ta = -40~85°C		Unit
			V _{CC} (V)	Typ.	Limit	Limit	
Minimum pulse width (LE)	t _w (H)	—	3.3 ± 0.3	—	5.0	5.0	ns
			5.0 ± 0.5	—	5.0	5.0	
Minimum set-up time	t _s	—	3.3 ± 0.3	—	3.5	3.5	ns
			5.0 ± 0.5	—	3.5	3.5	
Minimum hold time	t _h	—	3.3 ± 0.3	—	1.5	1.5	ns
			5.0 ± 0.5	—	1.5	1.5	

AC Characteristics (Input: $t_r = t_f = 3 \text{ ns}$)

Characteristics	Symbol	Test Condition			Ta = 25°C			Ta = -40~85°C		Unit
			VCC (V)	CL (pF)	Min	Typ.	Max	Min	Max	
Propagation delay time (LE-Q)	t_{pLH} t_{pHL}	—	3.3 ± 0.3	15	—	7.6	11.9	1.0	14.0	ns
				50	—	10.1	15.4	1.0	17.5	
			5.0 ± 0.5	15	—	5.0	7.7	1.0	9.0	
				50	—	6.5	9.7	1.0	11.0	
Propagation delay time (D-Q)	t_{pLH} t_{pHL}	—	3.3 ± 0.3	15	—	7.0	11.0	1.0	13.0	ns
				50	—	9.5	14.5	1.0	16.5	
			5.0 ± 0.5	15	—	4.5	6.8	1.0	8.0	
				50	—	6.0	8.8	1.0	10.0	
3-state output enable time	t_{pZL} t_{pZH}	$R_L = 1 \text{ k}\Omega$	3.3 ± 0.3	15	—	7.3	11.5	1.0	13.5	ns
				50	—	9.8	15.0	1.0	17.0	
			5.0 ± 0.5	15	—	5.2	7.7	1.0	9.0	
				50	—	6.7	9.7	1.0	11.0	
3-state output disable time	t_{pLZ} t_{pHZ}	$R_L = 1 \text{ k}\Omega$	3.3 ± 0.3	50	—	10.7	14.5	1.0	16.5	ns
			5.0 ± 0.5	50	—	6.7	9.7	1.0	11.0	
Output to output skew	t_{osLH} t_{osHL}	(Note 1)	3.3 ± 0.3	50	—	—	1.5	—	1.5	ns
			5.0 ± 0.5	50	—	—	1.0	—	1.0	
Input capacitance	C_{IN}	—	—	—	4	10	—	10	pF	
Output capacitance	C_{OUT}	—	—	—	6	—	—	—	pF	
Power dissipation capacitance	C_{PD}	(Note 2)	—	—	29	—	—	—	pF	

Note 1: This parameter is guaranteed by design.

$$t_{osLH} = |t_{pLHm} - t_{pLHn}|, \quad t_{osHL} = |t_{pHLm} - t_{pHLn}|$$

Note 2: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{ (per latch)}$$

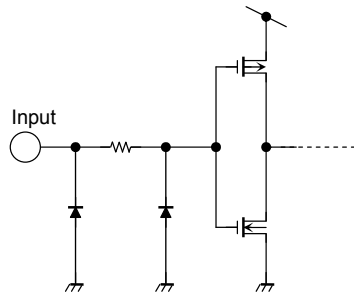
And the total C_{PD} when n pcs of latch operate can be gained by the following equation:

$$C_{PD}(\text{total}) = 21 + 8 \cdot n$$

Noise Characteristics (Input: $t_r = t_f = 3 \text{ ns}$)

Characteristics	Symbol	Test Condition	Ta = 25°C			Unit
			V _{CC} (V)	Typ.	Limit	
Quiet output maximum dynamic V _{OL}	V _{OLP}	C _L = 50 pF	5.0	0.8	1.0	V
Quiet output minimum dynamic V _{OL}	V _{OLV}	C _L = 50 pF	5.0	-0.8	-1.0	V
Minimum high level dynamic input voltage V _{IH}	V _{IHD}	C _L = 50 pF	5.0	—	3.5	V
Maximum low level dynamic input voltage V _{IL}	V _{ILD}	C _L = 50 pF	5.0	—	1.5	V

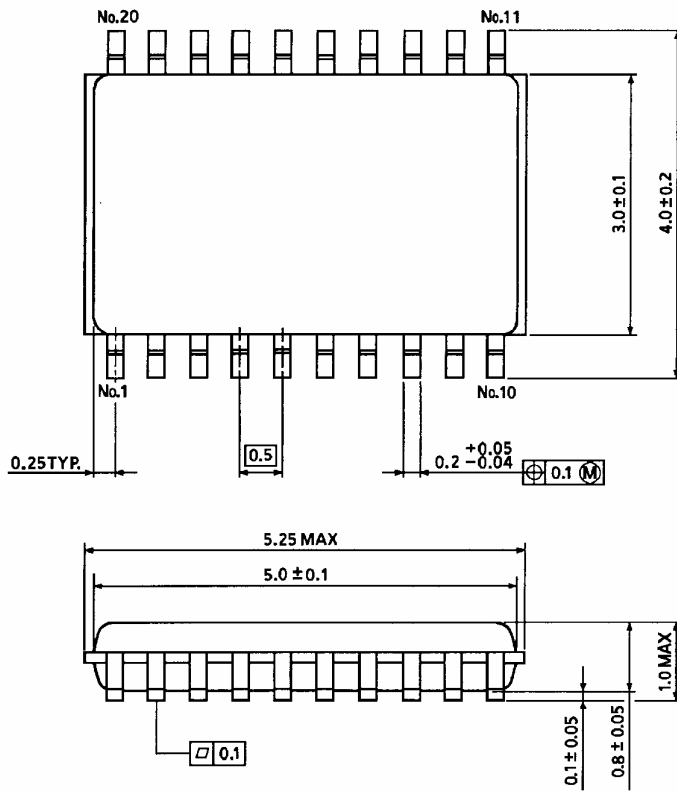
Input Equivalent Circuit



Package Dimensions

VSSOP20-P-0030-0.50

Unit : mm



Weight: 0.03 g (typ.)

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20070701-EN GENERAL

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