

TC7MH245FK

Octal Bus Transceiver

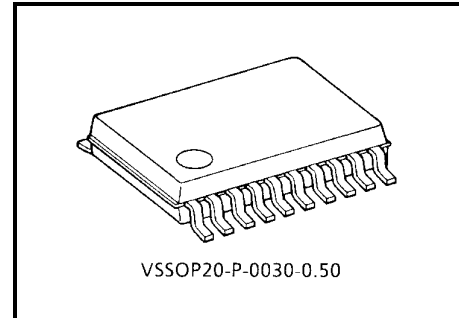
The TC7MH245FK is an advanced high speed CMOS octal bus transceiver fabricated with silicon gate C²MOS technology.

It achieves the high speed operation similar to equivalent bipolar schottky TTL while maintaining the CMOS low power dissipation.

It is intended for two-way asynchronous communication between data busses. The direction of data transmission is determined by the level of the DIR input.

The enable input (\bar{G}) can be used to disable the device so that the busses are effectively isolated.

All inputs are equipped with protection circuits against static discharge.



Weight: 0.03 g (typ.)

Features

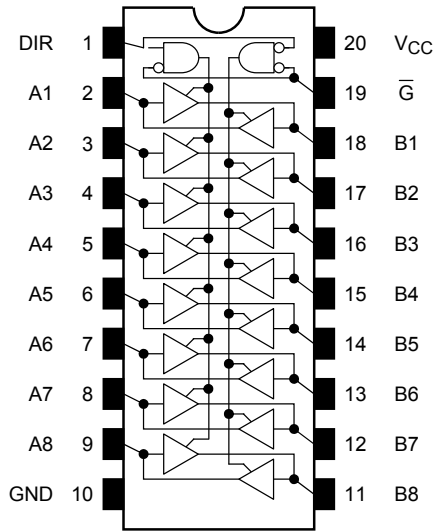
- High speed: $t_{pd} = 4.0$ ns (typ.) ($V_{CC} = 5$ V)
- Low power dissipation: $I_{CC} = 4$ μ A (max) ($T_a = 25^\circ$ C)
- High noise immunity: $V_{NIH} = V_{NIL} = 28\%$ V_{CC} (min)
- Balanced propagation delays: $t_{pLH} \approx t_{pHL}$
- Wide operating voltage range: $V_{CC (opr)} = 2\sim 5.5$ V
- Low noise: $V_{OLP} = 1.0$ V (max)
- Pin and function compatible with 74ALS245

Note: Do not apply a signal to any bus terminal when it is in the output mode. Damage may result.

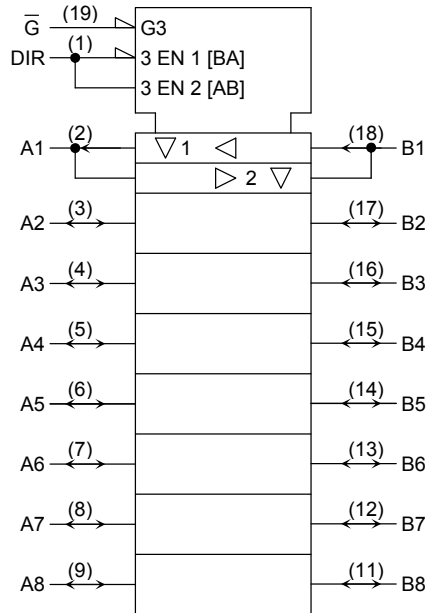
All floating (high impedance) bus terminals must have their input levels fixed by means of pull up or pull down resistors.

A parasitic diode is formed between the bus and V_{CC} terminals. Therefore bus terminal can not be used to interface 5 V to 3 V systems directly.

Pin Assignment (top view)



IEC Logic Symbol



Truth Table

Inputs		Outputs	Function	
G-bar	DIR		A-Bus	B-Bus
L	L	A = B	Output	Input
L	H	B = A	Input	Output
H	X	Z	Z	

X: Don't care

Z: High impedance

Absolute Maximum Rating (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V _{CC}	-0.5~7.0	V
DC input voltage (DIR, G-bar)	V _{IN}	-0.5~7.0	V
DC bus I/O voltage	V _{I/O}	-0.5~V _{CC} + 0.5	V
Input diode current (DIR, G-bar)	I _{IK}	-20	mA
Output diode current	I _{OK}	±20	mA
DC output current	I _{OUT}	±25	mA
DC V _{CC} /ground current	I _{CC}	±75	mA
Power dissipation	P _D	180	mW
Storage temperature	T _{stg}	-65~150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, may lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	2.0~5.5	V
Input voltage (DIR, \bar{G})	V_{IN}	0~5.5	V
Bus I/O voltage	$V_{I/O}$	0~ V_{CC}	V
Operating temperature	T_{opr}	-40~85	°C
Input rise and fall time	dt/dv	0~100 ($V_{CC} = 3.3 \pm 0.3$ V)	ns/V
		0~20 ($V_{CC} = 5 \pm 0.5$ V)	

Note: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs and bus inputs must be tied to either VCC or GND. Please connect both bus inputs and the bus outputs with VCC or GND when the I/O of the bus terminal changes by the function. In this case, please note that the output is not short-circuited.

Electrical Characteristics

DC Characteristics

Characteristics	Symbol	Test Condition	$T_a = 25^\circ\text{C}$				$T_a = -40\sim 85^\circ\text{C}$		Unit		
			V_{CC} (V)	Min	Typ.	Max	Min	Max			
Input voltage	High level	V_{IH}	—	2.0	1.50	—	—	1.50	—	V	
				3.0~5.5	$V_{CC} \times 0.7$	—	—	$V_{CC} \times 0.7$	—		
	Low level	V_{IL}	—	2.0	—	—	0.50	—	0.50		
				3.0~5.5	—	—	$V_{CC} \times 0.3$	—	$V_{CC} \times 0.3$		
Output voltage	High level	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -50 \mu\text{A}$	2.0	1.9	2.0	—	1.9	—	V
					3.0	2.9	3.0	—	2.9	—	
					4.5	4.4	4.5	—	4.4	—	
					3.0	2.58	—	—	2.48	—	
	Low level	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 50 \mu\text{A}$	2.0	—	0	0.1	—	0.1	
					3.0	—	0	0.1	—	0.1	
					4.5	—	0	0.1	—	0.1	
					3.0	—	—	0.36	—	0.44	
					4.5	—	—	0.36	—	0.44	
					—	—	—	—	—	—	
3-state output off-state current	I_{OZ}	$V_{IN} = V_{IH}$ or V_{IL} $V_{OUT} = V_{CC}$ or GND	5.5	—	—	± 0.25	—	± 2.50	μA		
Input leakage current	I_{IN}	$V_{IN} = 5.5$ V or GND	0~5.5	—	—	± 0.1	—	± 1.0	μA		
Quiescent supply current	I_{CC}	$V_{IN} = V_{CC}$ or GND	5.5	—	—	4.0	—	40.0	μA		

AC Characteristics (Input: $t_r = t_f = 3$ ns)

Characteristics	Symbol	Test Condition	Ta = 25°C				Ta = -40~85°C		Unit	
			VCC (V)	CL (pF)	Min	Typ.	Max	Min		Max
Propagation delay time	t_{pLH} t_{pHL}	—	3.3 ± 0.3	15	—	5.8	8.4	1.0	10.0	ns
				50	—	8.3	11.9	1.0	13.5	
			5.0 ± 0.5	15	—	4.0	5.5	1.0	6.5	
				50	—	5.5	7.5	1.0	8.5	
3-state output enable time	t_{pZL} t_{pZH}	RL = 1 kΩ	3.3 ± 0.3	15	—	8.5	13.2	1.0	15.5	ns
				50	—	11.0	16.7	1.0	19.0	
			5.0 ± 0.5	15	—	5.8	8.5	1.0	10.0	
				50	—	7.3	10.6	1.0	12.0	
3-state output disable time	t_{pLZ} t_{pHZ}	RL = 1 kΩ	3.3 ± 0.3	50	—	11.5	15.8	1.0	18.0	ns
			5.0 ± 0.5	50	—	7.0	9.7	1.0	11.0	
Output to output skew	$t_{oS LH}$ $t_{oS HL}$	(Note 1)	3.3 ± 0.3	50	—	—	1.5	—	1.5	ns
			5.0 ± 0.5	50	—	—	1.0	—	1.0	
Input capacitance	CIN	DIR, \bar{G}			—	4	10	—	10	pF
Bus input capacitance	C _{I/O}	A _n , B _n			—	8	—	—	—	pF
Power dissipation capacitance	CPD		(Note 2)		—	21	—	—	—	pF

Note 1: This parameter is guaranteed by design.

$$t_{oS LH} = |t_{pLHm} - t_{pLHn}|, t_{oS HL} = |t_{pHLm} - t_{pHLn}|$$

Note 2: CPD is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

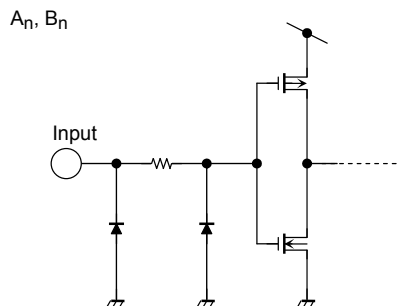
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{ (per bit)}$$

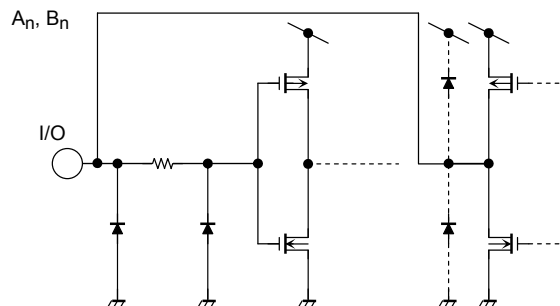
Noise Characteristics (Input: $t_r = t_f = 3$ ns)

Characteristics	Symbol	Test Condition	Ta = 25°C			Unit
			VCC (V)	Typ.	Limit	
Quiet output maximum dynamic V _{OL}	V _{OLP}	CL = 50 pF	5.0	0.7	1.0	V
Quiet output minimum dynamic V _{OL}	V _{OLV}	CL = 50 pF	5.0	-0.7	-1.0	V
Minimum high level dynamic input voltage V _{IH}	V _{IHD}	CL = 50 pF	5.0	—	3.5	V
Maximum low level dynamic input voltage V _{IL}	V _{ILD}	CL = 50 pF	5.0	—	1.5	V

Input Equivalent Circuit



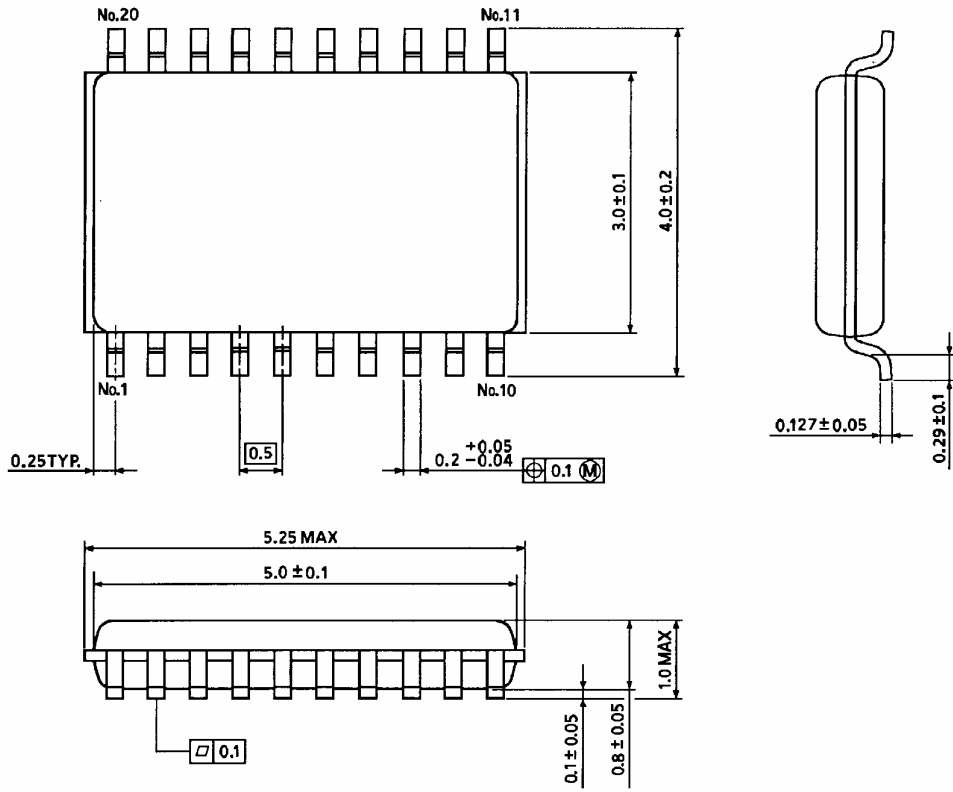
Bus Terminal Equivalent Circuit



Package Dimensions

VSSOP20-P-0030-0.50

Unit : mm



Weight: 0.03 g (typ.)

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20070701-EN GENERAL

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