

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

# TC7MH240FK, TC7MH244FK

## Octal Bus Buffer

TC7MH240FK Inverted, 3-State Outputs

TC7MH244FK Non-Inverted, 3-State Outputs

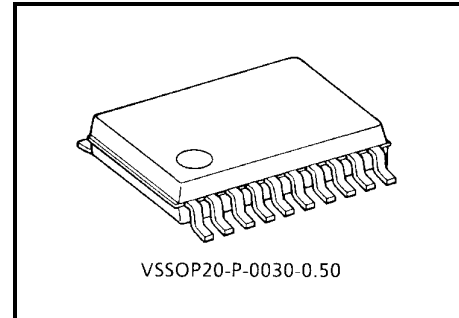
The TC7MH240FK and TC7MH244FK are advanced high speed CMOS octal bus buffers fabricated with silicon gate C<sup>2</sup>MOS technology.

They achieve the high speed operation similar to equivalent bipolar schottky TTL while maintaining the CMOS low power dissipation.

The TC7MH240FK is an inverting 3-state buffer having two active-low output enables. The TC7MH244FK is a non-inverting 3-state buffer, and has two active-low output enables.

These devices are designed to be used with 3-state memory address drivers, etc.

An input protection circuit ensures that 0 to 5.5 V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5 V to 3 V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

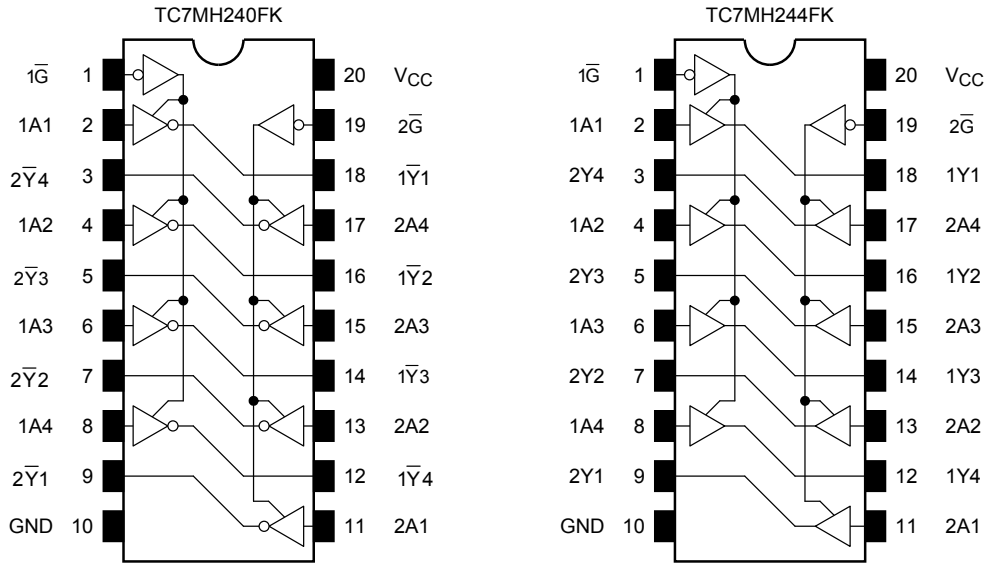


Weight: 0.03 g (typ.)

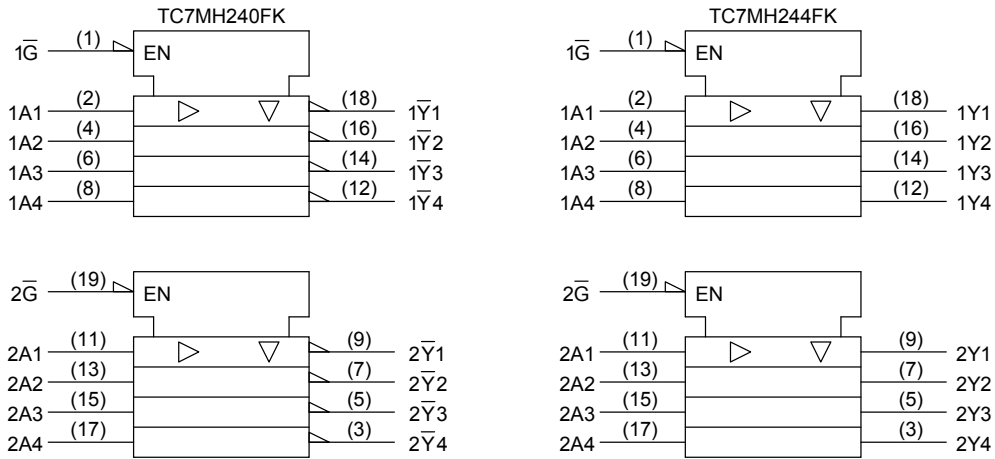
## Features

- High speed:  $t_{pd} = 3.9$  ns (typ.) ( $V_{CC} = 5$  V)
- Low power dissipation:  $I_{CC} = 4$   $\mu$ A (max) ( $T_a = 25^\circ$ C)
- High noise immunity:  $V_{NIH} = V_{NIL} = 28\%$   $V_{CC}$  (min)
- Power down protection is provided on all inputs.
- Balanced propagation delays:  $t_{pLH} \approx t_{pHL}$
- Wide operating voltage range:  $V_{CC(opr)} = 2\sim 5.5$  V
- Low noise:  $V_{OLP} = 0.8$  (max)
- Pin and function compatible with 74ALS240/244

**Pin Assignment (top view)**



**IEC Logic Symbol**



**Truth Table**

Inputs		Outputs	
$\bar{G}$	$A_n$	$Y_n$	$\bar{Y}_n$
L	L	L	H
L	H	H	L
H	X	Z	Z

X : Don't care

Z : High impedance

$Y_n$  : TC7MH244FK

$\bar{Y}_n$  : TC7MH240FK

## Absolute Maximum Ratings (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage range	$V_{CC}$	-0.5~7.0	V
DC input voltage	$V_{IN}$	-0.5~7.0	V
DC output voltage	$V_{OUT}$	-0.5~ $V_{CC} + 0.5$	V
Input diode current	$I_{IK}$	-20	mA
Output diode current	$I_{OK}$	$\pm 20$	mA
DC output current	$I_{OUT}$	$\pm 25$	mA
DC $V_{CC}$ /ground current	$I_{CC}$	$\pm 75$	mA
Power dissipation	$P_D$	180	mW
Storage temperature	$T_{stg}$	-65~150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

## Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	$V_{CC}$	2.0~5.5	V
Input voltage	$V_{IN}$	0~5.5	V
Output voltage	$V_{OUT}$	0~ $V_{CC}$	V
Operating temperature	$T_{opr}$	-40~85	°C
Input rise and fall time	dt/dv	0~100 ( $V_{CC} = 3.3 \pm 0.3$ V)	ns/V
		0~20 ( $V_{CC} = 5 \pm 0.5$ V)	

Note: The operating ranges must be maintained to ensure the normal operation of the device.  
Unused inputs must be tied to either VCC or GND.

## Electrical Characteristics

### DC Characteristics

Characteristics		Symbol	Test Condition	Ta = 25°C			Ta = -40~85°C		Unit			
				V <sub>CC</sub> (V)	Min	Typ.	Max	Min		Max		
Input voltage	High level	V <sub>IH</sub>	—	2.0	1.50	—	—	1.50	V			
				3.0~5.5	V <sub>CC</sub> × 0.7	—	—	V <sub>CC</sub> × 0.7		—		
	Low level	V <sub>IL</sub>	—	2.0	—	—	0.50	—		0.50		
				3.0~5.5	—	—	V <sub>CC</sub> × 0.3	—		V <sub>CC</sub> × 0.3		
Output voltage	High level	V <sub>OH</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -50 μA	2.0	1.9	2.0	—	1.9	V		
					3.0	2.9	3.0	—	2.9		—	
					4.5	4.4	4.5	—	4.4		—	
				I <sub>OH</sub> = -4 mA	3.0	2.58	—	—	2.48		—	
	4.5	3.94	—		—	3.80	—					
	Low level	V <sub>OL</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 50 μA	2.0	—	0	0.1	—		0.1	
					3.0	—	0	0.1	—		0.1	
					4.5	—	0	0.1	—		0.1	
					I <sub>OL</sub> = 4 mA	3.0	—	—	0.36		—	0.44
						4.5	—	—	0.36		—	0.44
I <sub>OL</sub> = 8 mA					4.5	—	—	0.36	—	0.44		
3-state output off-state current	I <sub>OZ</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>OUT</sub> = V <sub>CC</sub> or GND	5.5	—	—	±0.25	—	±2.50	μA			
Input leakage current	I <sub>IN</sub>	V <sub>IN</sub> = 5.5 V or GND	0~5.5	—	—	±0.1	—	±1.0	μA			
Quiescent supply current	I <sub>CC</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND	5.5	—	—	4.0	—	40.0	μA			

## AC Characteristics (Input: $t_r = t_f = 3$ ns)

Characteristics	Symbol	Test Condition			Ta = 25°C			Ta = -40~85°C		Unit
			VCC (V)	CL (pF)	Min	Typ.	Max	Min	Max	
Propagation delay time (TC7MH240FK)	$t_{pLH}$ $t_{pHL}$	—	$3.3 \pm 0.3$	15	—	5.3	7.5	1.0	9.0	ns
				50	—	7.8	11.0	1.0	12.5	
			$5.0 \pm 0.5$	15	—	3.6	5.5	1.0	6.5	
				50	—	5.1	7.5	1.0	8.5	
Propagation delay time (TC7MH244FK)	$t_{pLH}$ $t_{pHL}$	—	$3.3 \pm 0.3$	15	—	5.8	8.4	1.0	10.0	ns
				50	—	8.3	11.9	1.0	13.5	
			$5.0 \pm 0.5$	15	—	3.9	5.5	1.0	6.5	
				50	—	5.4	7.5	1.0	8.5	
3-state output enable time	$t_{pZL}$ $t_{pZH}$	$R_L = 1$ k $\Omega$	$3.3 \pm 0.3$	15	—	6.6	10.6	1.0	12.5	ns
				50	—	9.1	14.1	1.0	16.0	
			$5.0 \pm 0.5$	15	—	4.7	7.3	1.0	8.5	
				50	—	6.2	9.3	1.0	10.5	
3-state output disable time	$t_{pLZ}$ $t_{pHZ}$	$R_L = 1$ k $\Omega$	$3.3 \pm 0.3$	50	—	10.3	14.0	1.0	16.0	ns
			$5.0 \pm 0.5$	50	—	6.7	9.2	1.0	10.5	
Output to output skew	$t_{osLH}$ $t_{osHL}$	(Note 1)	$3.3 \pm 0.3$	50	—	—	1.5	—	1.5	ns
			$5.0 \pm 0.5$	50	—	—	1.0	—	1.0	
Input capacitance	$C_{IN}$	—	—	—	4	10	—	10	pF	
Output capacitance	$C_{OUT}$	—	—	—	6	—	—	—	pF	
Power dissipation capacitance (Note 2)	$C_{PD}$	TC7MH240FK	—	—	17	—	—	—	pF	
		TC7MH244FK	—	—	19	—	—	—		

Note 1: Parameter guaranteed by design.

$$t_{osLH} = |t_{pLHm} - t_{pLHn}|, t_{osHL} = |t_{pHLm} - t_{pHLn}|$$

Note 2:  $C_{PD}$  is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

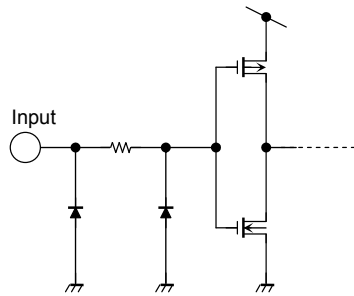
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{ (per bit)}$$

**Noise Characteristics (Input:  $t_r = t_f = 3 \text{ ns}$ )**

Characteristics	Symbol	Test Condition	Ta = 25°C			Unit
			V <sub>CC</sub> (V)	Typ.	Limit	
Quiet output maximum dynamic V <sub>OL</sub>	V <sub>OLP</sub>	C <sub>L</sub> = 50 pF	5.0	0.5	0.8	V
Quiet output minimum dynamic V <sub>OL</sub>	V <sub>OLV</sub>	C <sub>L</sub> = 50 pF	5.0	-0.5	-0.8	V
Minimum high level dynamic input voltage V <sub>IH</sub>	V <sub>IHD</sub>	C <sub>L</sub> = 50 pF	5.0	—	3.5	V
Maximum low level dynamic input voltage V <sub>IL</sub>	V <sub>ILD</sub>	C <sub>L</sub> = 50 pF	5.0	—	1.5	V

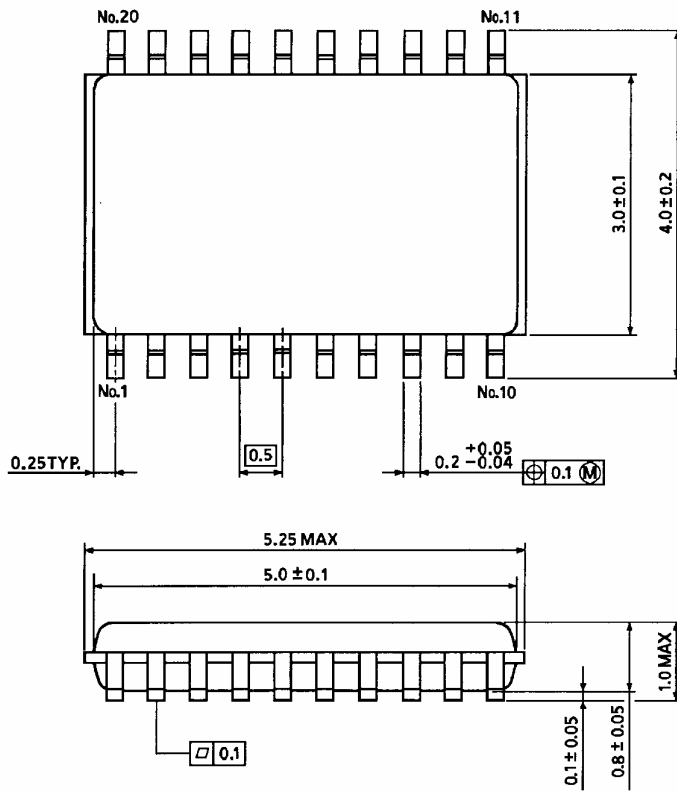
**Input Equivalent Circuit**



## Package Dimensions

VSSOP20-P-0030-0.50

Unit : mm



Weight: 0.03 g (typ.)

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20070701-EN GENERAL

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