

TC7MB3253FT, TC7MB3253FK

Dual 1-of-4 FET Multiplexer/Demultiplexer

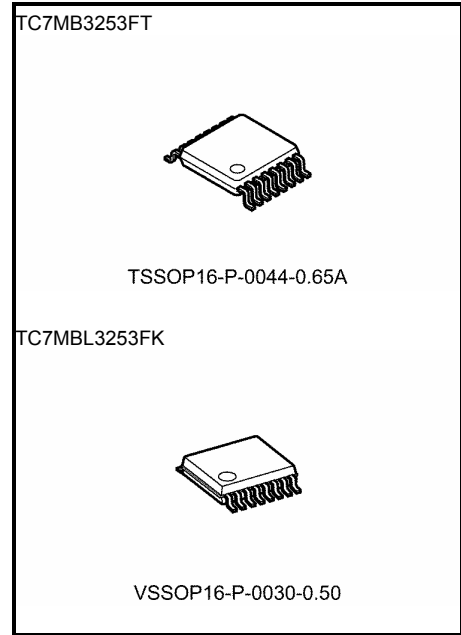
The TC7MB3253 is high-speed CMOS dual 1-4 Multiplexer/Demultiplexer. The low on resistance of the switch allows connections to be made with minimal propagation delay time.

This device consists of two individual two-inputs multiplexer/demultiplexer with common select inputs (S1, S0). The A inputs is connected to the corresponded B1 to B4 outputs determined by the combination both the select inputs (S1, S0) and output enable (\overline{OE}). When the output enable (\overline{OE}) input is held "H" level, the switches are open with regardless the state of select inputs and a high-impedance state exists between the switches.

All inputs are equipped with protection circuits against static discharge.

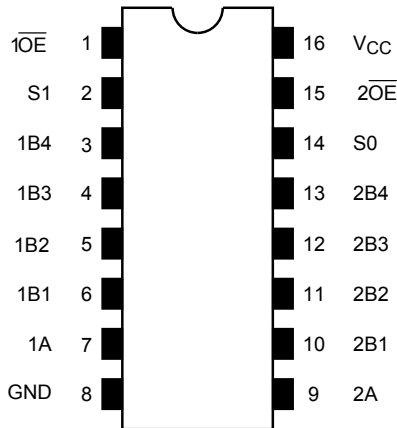
Features

- Operating voltage: $V_{CC} = 4.5$ to 5.5 V
- High speed: $t_{pd} = 0.25$ ns (max)
- Low on resistance: $R_{ON} = 5 \Omega$ (typ.)
- ESD performance: Machine model $\geq \pm 200$ V
Human body model $\geq \pm 2000$ V
- Compatible with TTL outputs (control inputs)
- Package: TSSOP16, VSSOP16 (US16)
- Pin compatible with the 74xx253 type.
Functionally equivalent to (FST/CBT) 3253.



Weight:
 TSSOP16-P-0044-0.65A : 0.06 g (typ.)
 VSSOP16-P-0030-0.50 : 0.02 g (typ.)

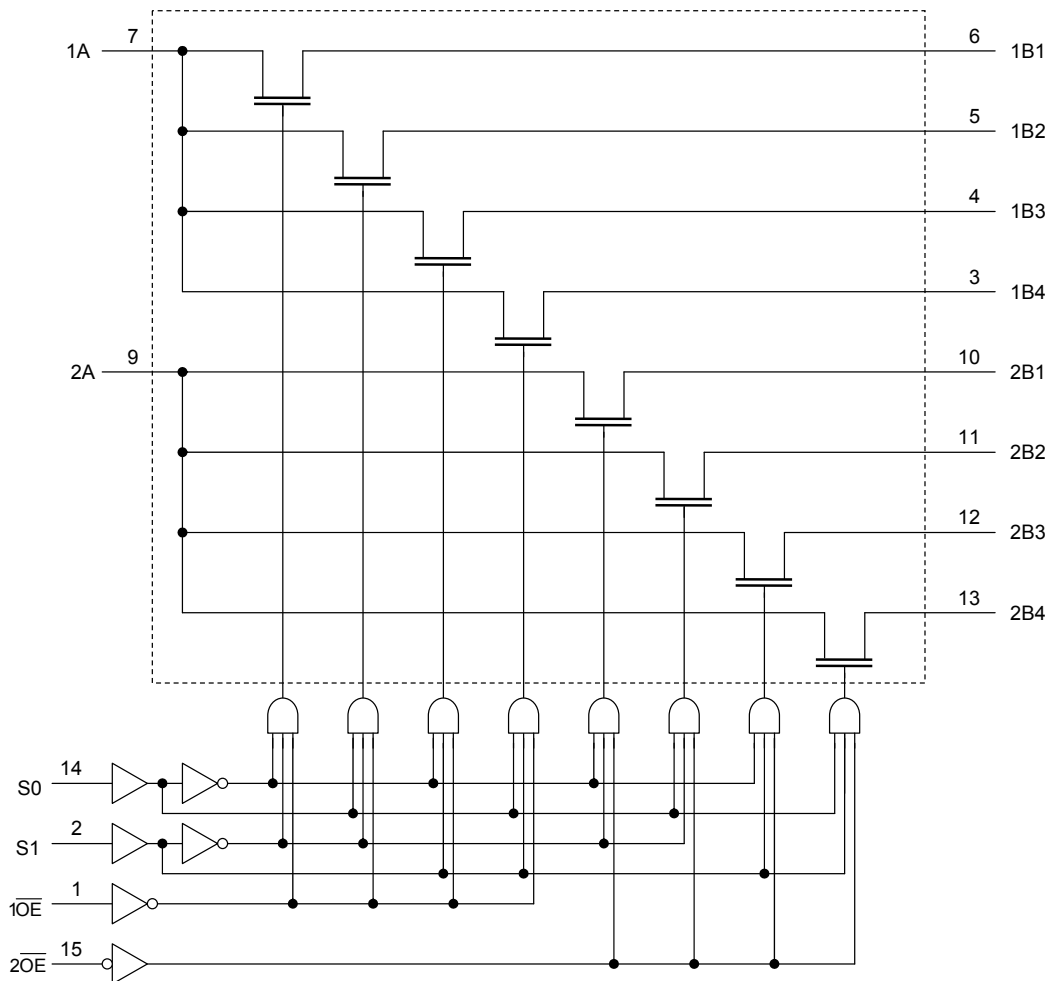
Pin Assignment (top view)



Truth Table

| Inputs | | | Function |
|-----------------|----|----|------------------|
| \overline{OE} | S1 | S0 | |
| L | L | L | A port = B1 port |
| L | L | H | A port = B2 port |
| L | H | L | A port = B3 port |
| L | H | H | A port = B4 port |
| H | X | X | Disconnect |

System Diagram



Absolute Maximum Ratings (Note)

| Characteristics | Symbol | Rating | Unit |
|----------------------------|------------------|-------------|-------------|
| Power supply range | V_{CC} | -0.5 to 7.0 | V |
| DC input voltage | V_{IN} | -0.5 to 7.0 | V |
| DC switch voltage | V_S | -0.5 to 7.0 | V |
| Input diode current | I_{IK} | -50 | mA |
| Continuous channel current | I_S | 128 | mA |
| Power dissipation | P_D | 180 | mW |
| DC V_{CC}/GND current | I_{CC}/I_{GND} | ± 100 | mA |
| Storage temperature | T_{stg} | -65 to 150 | $^{\circ}C$ |

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Operating Ranges (Note)

| Characteristics | Symbol | Rating | Unit |
|--------------------------|-----------|------------|-------------|
| Supply voltage | V_{CC} | 4.5 to 5.5 | V |
| Input voltage | V_{IN} | 0 to 5.5 | V |
| Switch voltage | V_S | 0 to 5.5 | V |
| Operating temperature | T_{opr} | -40 to 85 | $^{\circ}C$ |
| Input rise and fall time | dt/dv | 0 to 10 | ns/V |

Note: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either V_{CC} or GND.

Electrical Characteristics

DC Characteristics (Ta = -40 to 85°C)

| Characteristics | Symbol | Test Condition | V _{CC} (V) | Min | Typ. (Note 1) | Max | Unit | |
|--|------------------|--|-------------------------|------------|------------------|-----|------|----|
| | | | | | | | | |
| Input voltage | "H" level | V _{IH} | — | 4.5 to 5.5 | 2.0 | — | — | V |
| | "L" level | V _{IL} | — | 4.5 to 5.5 | — | — | 0.8 | |
| Input leakage current | I _{IN} | V _{IN} = 0 to 5.5 V | | 4.5~5.5 | — | — | ±1.0 | μA |
| Power off leakage current | I _{OFF} | A, B, \overline{OE} = 0 to 5.5 V | | 0 | — | — | ±1.0 | μA |
| Off-state leakage current (switch off) | I _{SZ} | A, B = 0 to 5.5 V, \overline{OE} = V _{CC} | | 4.5 to 5.5 | — | — | ±1.0 | μA |
| On resistance (Note 2) | R _{ON} | V _{IS} = 0 V | I _{IS} = 64 mA | 4.5 | — | 5 | 7 | Ω |
| | | | I _{IS} = 30 mA | 4.5 | — | 5 | 7 | |
| | | V _{IS} = 2.4 V, I _{IS} = 15 mA | | | 4.5 | — | 10 | |
| Quiescent supply current | I _{CC} | V _{IN} = V _{CC} or GND, I _{OUT} = 0 | | 5.5 | — | — | 10 | μA |
| Increase in I _{CC} per input | ΔI _{CC} | V _{IN} = 3.4 V (one input) | | 5.5 | — | — | 2.5 | mA |

Note 1: Typical values are at V_{CC} = 5 V, Ta = 25°C.

Note 2: Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins.

AC Characteristics (Ta = -40 to 85°C)

| Characteristics | Symbol | Test Condition | V _{CC} (V) | Min | Max | Unit |
|---|--------------------------------------|---------------------------|---------------------|-----|------|------|
| | | | | | | |
| Propagation delay time (bus to bus) | t _{pLH} t _{pHL} | Figure 1, Figure 2 (Note) | 4.5 | — | 0.25 | ns |
| Propagation delay time (S to bus) | t _{pLH} t _{pHL} | Figure 1, Figure 2 | 4.5 | — | 5.3 | ns |
| Output enable time (\overline{OE} to bus) | t _{pZL} t _{pZH} | Figure 1, Figure 3 | 4.5 | — | 5.3 | ns |
| Output enable time (S to bus) | t _{pZL} t _{pZH} | Figure 1, Figure 3 | 4.5 | — | 5.3 | ns |
| Output disable time (\overline{OE} to bus) | t _{pLZ} t _{pHZ} | Figure 1, Figure 3 | 4.5 | — | 5.3 | ns |
| Output disable time (S to bus) | t _{pLZ} t _{pHZ} | Figure 1, Figure 3 | 4.5 | — | 5.3 | ns |

Note: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical on resistance of the switch and the 50 pF load capacitance, when driven by an ideal voltage the source (zero output impedance).

Capacitive Characteristics (Ta = 25°C)

| Characteristics | Symbol | Test Condition | V _{CC} (V) | Typ. | Unit | |
|--|------------------|-----------------------------------|---------------------|------|------|----|
| | | | | | | |
| Control pin input capacitance (\overline{OE} , S) | C _{IN} | (Note) | 5.0 | 3 | pF | |
| Switch terminal capacitance (B) | C _{I/O} | \overline{OE} = V _{CC} | (Note) | 5.0 | 10 | pF |
| Switch terminal capacitance (A) | C _{I/O} | \overline{OE} = V _{CC} | (Note) | 5.0 | 31 | pF |

Note: This parameter is guaranteed by design.

AC Test Circuit

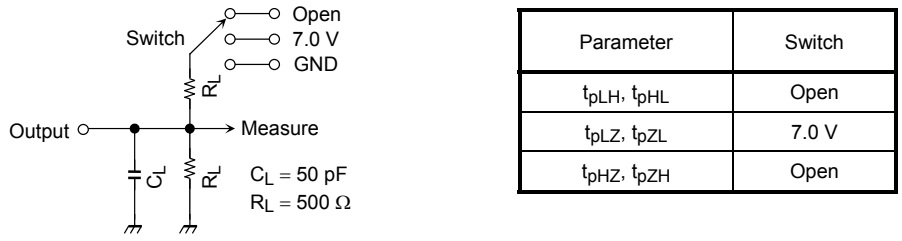


Figure 1

AC Waveform

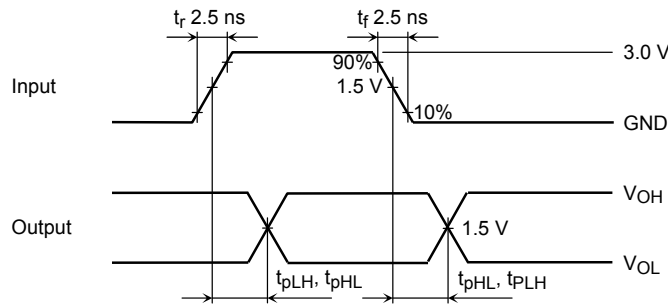


Figure 2 t_{pLH}, t_{pHL}

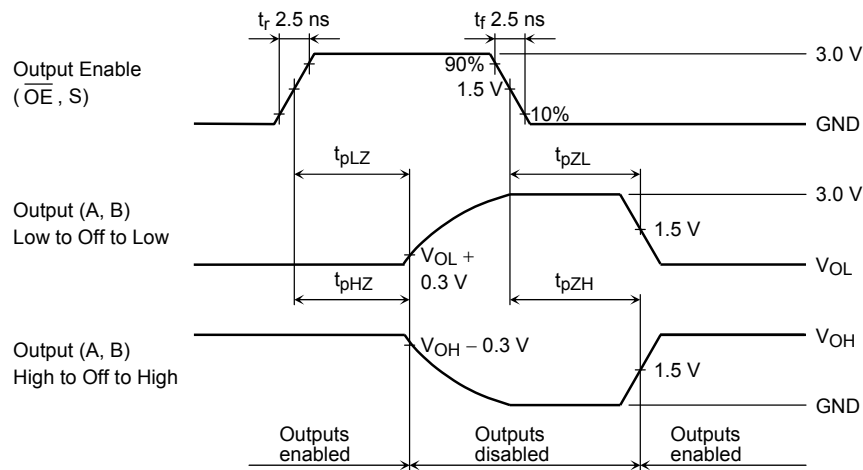
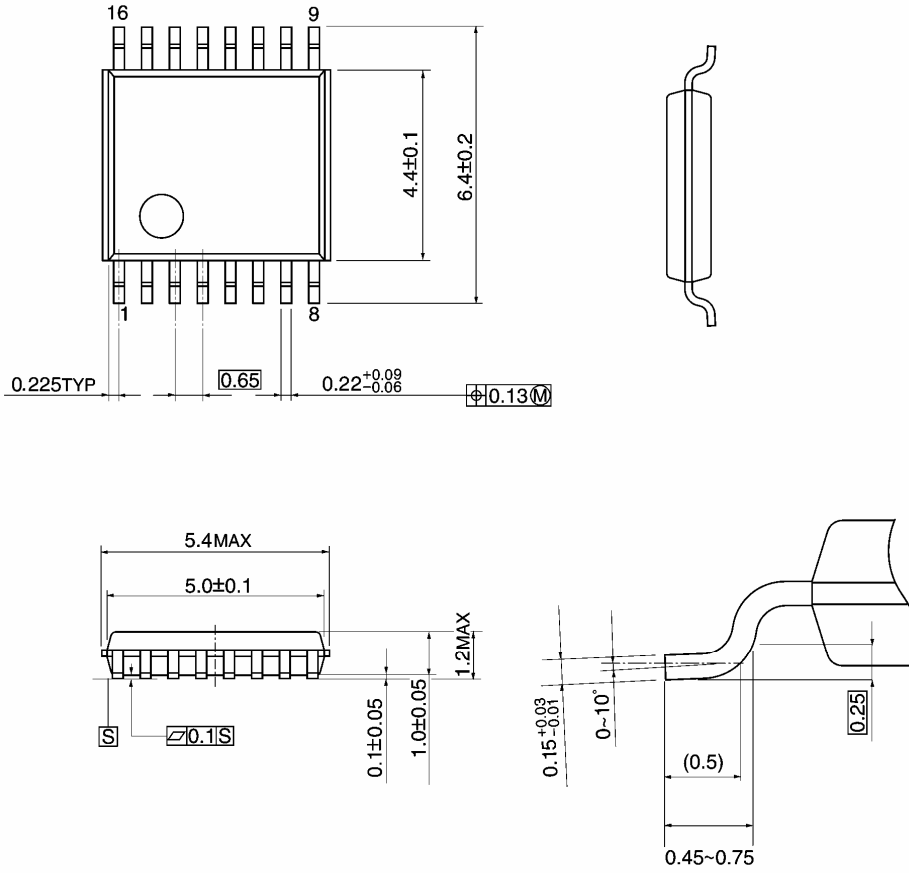


Figure 3 $t_{pLZ}, t_{pHZ}, t_{pZL}, t_{pZH}$

Package Dimensions

TSSOP16-P-0044-0.65A

Unit: mm

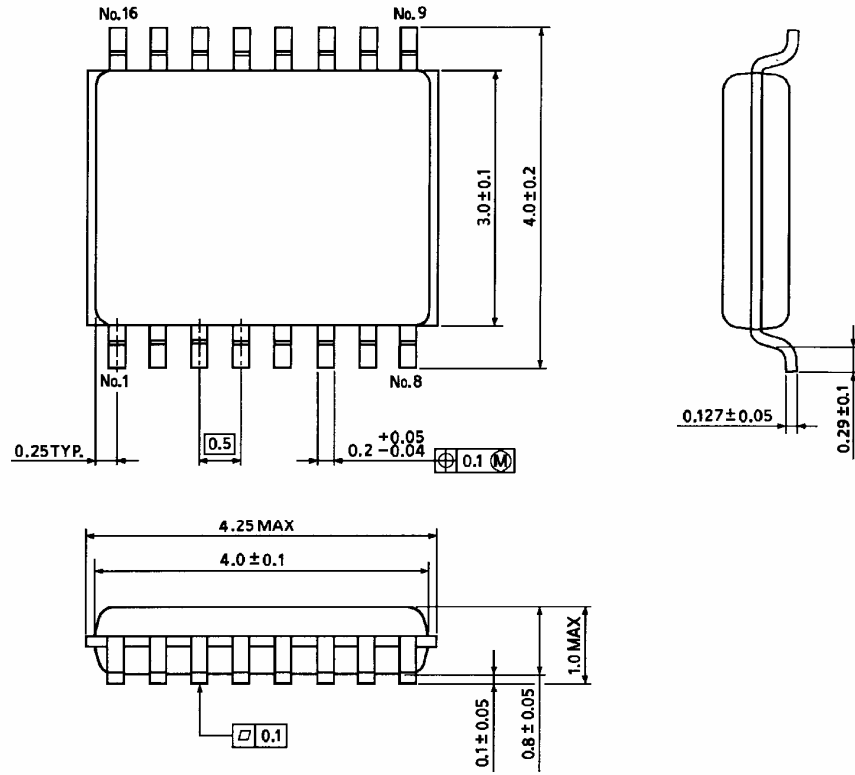


Weight: 0.06 g (typ.)

Package Dimensions

VSSOP16-P-0030-0.50

Unit : mm



Weight: 0.02 g (typ.)

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20070701-EN GENERAL

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