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TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC7MBL6353SFT, TC7MBL6353SFK, TC7MBL6353SFTG

Low Voltage/Low Capacitance Dual 1-of-2 Multiplexer/Demultiplexer

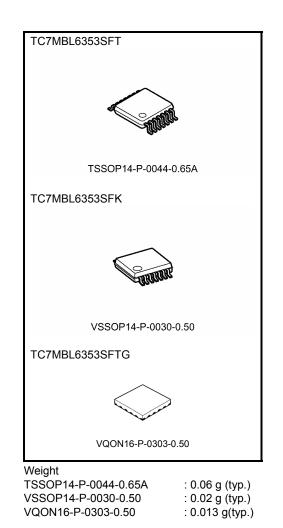
The TC7MBL6353S is a Low Voltage/Low Capacitance CMOS Dual 1-of-2 Multiplexer/Demultiplexer. The low on-resistance of the switch allows connections to be made with minimal propagation delay time.

This device consists of two individual two-inputs multiplexer/ demultiplexer with common select input (S) and output enable (\overline{OE}). The A input is connected to the B1 or B2 outputs as determined by the combination of both the select input (S) and output enable (\overline{OE}). When the output enable (\overline{OE}) input is held at "H" level, the switches are open regardless of the state of the select inputs, and a high-impedance state exists between the switches.

All inputs are equipped with protection circuits against static discharge.

Features

- Operating voltage: VCC = 1.65~3.6 V
- Low capacitance: $C_{I/O} = 15 \text{ pF}$ Switch On (typ.) @3 V
- Low on-resistance: $RON = 9 \Omega$ (typ.) @3 V
- ESD performance: Machine model $\geq \pm 200 \text{ V}$ Human body model $\geq \pm 2000 \text{ V}$
- Power-down protection for inputs (OE input only)
- Package: TSSOP14,VSSOP (US14), VQON16



Note: When mounting VQON package, the type of recommended flux is RA or RMA.

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12

11

10

9

8

1B1

1B2

2B1

2B2

FTG (VQON16-P-0303-0.50)

S NC V_{CC} \overline{OE} 15 14 13

NC GND NC NC

16

5 6 7

1A

NC

2A

NC

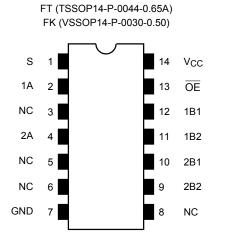
1

2

3

4

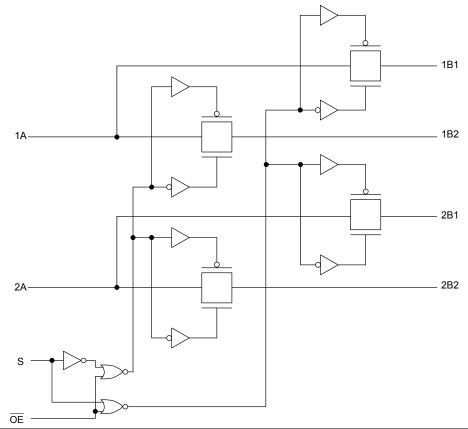
Pin Assignment (top view)



Truth Table

Inp	outs	Function		
S	ŌĒ	Function		
Х	Н	Disconnect		
L	L	nA port = nB1 port		
Н	L	nA port = nB2 port		

System Diagram



Absolute Maximum Ratings (Note)

Chara	cteristic	Symbol	Rating	Unit
Power supply rang	je	V _{CC}	-0.5~4.6	V
Control pin input v	oltage	V _{IN}	-0.5~4.6	V
Switch terminal I/C) voltage	Vs	$-0.5 \sim V_{CC} + 0.5$	V
Clump diode	Control input pin	lu.	-50	mA
current	Switch terminal	Ік	±50	mA
Switch I/O current		۱ _S	50	mA
Power dissipation		PD	180	mW
DC V _{CC} /GND curr	rent	I _{CC} /I _{GND}	±100	mA
Storage temperatu	ire	T _{stg}	-65~150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Operating Ranges (Note)

Characteristic	Symbol	Rating	Unit
Power supply voltage	V _{CC}	1.65~3.6	V
Control pin input voltage	VIN	0~3.6	V
Switch I/O voltage	VS	0~V _{CC}	V
Operating temperature	T _{opr}	-40~85	°C
Input rise and fall time	dt/dv	0~10	ns/V

Note: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either VCC or GND.

Electrical Characteristics

DC Characteristics (Ta = -40~85°C)

Parame	eter	Symbol	Test Condition V _{CC} (V)		Min	Тур.	Max	Unit	
Input voltage	"H" level	VIH	— 1.6		1.65~3.6	$0.7 \times V_{CC}$			V
input voltage	"L" level	VIL	_	1.65·		_		$0.3 \times V_{CC}$	v
Input leakage cur	rent (OE , S)	lin	$V_{IN} = 0 \sim 3.6 V$		1.65~3.6	_	_	±1.0	μA
Power-off leakage	e current	I _{OFF}	0E = 0∼3.6 V		0	_	_	1.0	μA
Off-state leakage (switch off)	current	I _{SZ}	$A, B = 0 \sim V_{CC}, \overline{OE} = V_{CC} \qquad 1.$		1.65~3.6	_	_	±1.0	μA
			$V_{IS} = 0 V, I_{IS} = 30 mA$	(Note1)	3.0	_	9	13	
			$V_{IS} = 3.0 \text{ V}, \ I_{IS} = 30 \text{ mA}$	(Note1)	3.0	_	15	20	
On resistance (Note2)		Davi	$V_{IS} = 2.4 \text{ V}, \ I_{IS} = 15 \text{ mA}$	(Note1)	3.0	_	19	27	Ω
		R _{ON}	$V_{IS} = 0$ V, $I_{IS} = 24$ mA	(Note1)	2.3		10	16	12
			$V_{IS} = 2.3 \text{ V}, \ I_{IS} = 24 \text{ mA}$	(Note1)	2.3	_	17	24	
			$V_{IS} = 2.0 \text{ V}, \ I_{IS} = 15 \text{ mA}$	(Note1)	2.3	_	21	30	
Increase in I _{CC} pe	er input	ICC	$V_{IN} = V_{CC} \text{ or } GND, I_{OUT} = 0$		3.6		_	10	μA

Note1: All typical values are at Ta=25°C.

Note2: Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins.

AC Characteristics (Ta = -40~85°C)

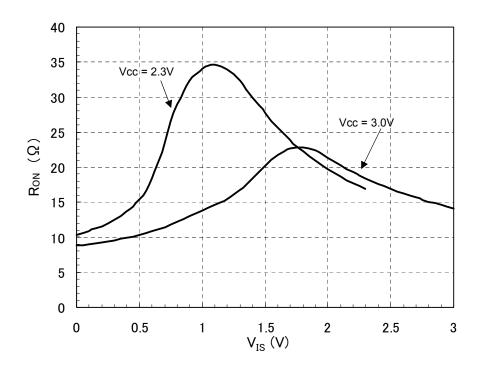
Characteristics	Symbol Test Condition			Min	Max	Unit
Characteristics	Cymbol		V _{CC} (V)	IVIIII	IVIAX	Offic
Dreportion dolou time			$\textbf{3.3}\pm\textbf{0.3}$		6	ns
Propagation delay time (S to bus)	t _{pLH}	Figure 1, Figure 2	2.5 ± 0.2	_	7	
(3 to bus)	t _{pHL}		1.8 ± 0.15	_	11	
			$\textbf{3.3}\pm\textbf{0.3}$		6	ns
Output enable time $(\overline{OE} \text{ to bus})$	t _{pZL} t _{pZH}	Figure 1, Figure 3	2.5 ± 0.2	_	7	
	۰р∠п		1.8 ± 0.15	_	11	
Output onable time	t _{pZL} t _{pZH}	Figure 1, Figure 3	$\textbf{3.3}\pm\textbf{0.3}$	_	6	ns
Output enable time (S to bus)			2.5 ± 0.2		7	
(0 (0 000)			1.8 ± 0.15		11	
Output disable time	t		$\textbf{3.3}\pm\textbf{0.3}$		6	ns
Output disable time $(\overline{OE} to bus)$	t _{pLZ} t _{pHZ}	Figure 1, Figure 3	2.5 ± 0.2		7	
			1.8 ± 0.15		11	
	t	Figure 1, Figure 3	$\textbf{3.3}\pm\textbf{0.3}$	_	6	ns
	t _{pLZ} t _{pHZ}		2.5 ± 0.2	_	7	
	γnz		1.8 ± 0.15	_	11	

Capacitive Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	V _{CC} (V)	Тур.	Unit
Control pin input capacitance ($\overline{\text{OE}}$, S)	CIN		3.0	3	pF
Switch terminal capacitance (B1~2)	C _{I/O}	$\overline{OE} = V_{CC}$ (switch off)	3.0	6	pF
Switch terminal capacitance (A)	C _{I/O}	$\overline{OE} = V_{CC}$ (switch off)	3.0	9	pF
Switch terminal capacitance	C _{I/O}	\overline{OE} = GND (switch on)	3.0	15	pF

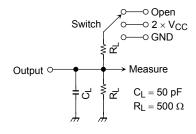
Note: This parameter is guaranteed by design

• RON Characteristic (typ.) Ta=25°C



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AC Test Circuit



Parameter	Switch
t _{pLH} , t _{pHL}	Open
tpLZ, tpZL	$2 \times V_{CC}$
t _{pHZ} , t _{pZH}	GND



AC Waveform

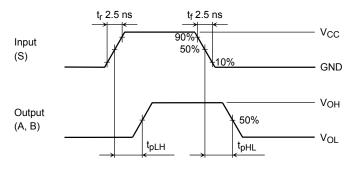


Figure 2 t_{pLH}, t_{pHL}

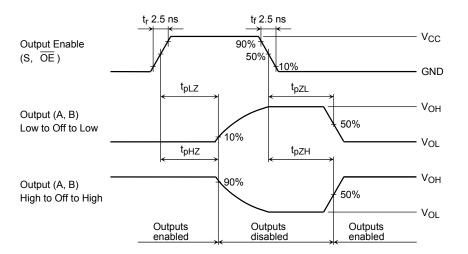


Figure 3 $t_{pLZ}, t_{pHZ}, t_{pZL}, t_{pZH}$

Rise and Fall Times (tr / tf) of the TC7MBL6353S I/O Signals

The tr(out) and tf(out) values of the output signals are affected by the CR time constant of the input, which consists of the switch terminal capacitance ($C_{I/O}$) and the on-resistance (R_{ON}) of the input.

In practice, the tr(out) and tf(out) values are also affected by the circuit's capacitance and resistance components other than those of the TC7MBL6353S.

The tr / tf (out) values can be approximated as follows. (Figure 4 shows the test circuit.)

tr / tf out (approx) = - ($C_{I/O} + C_L$) · ($R_{DRIVE+} R_{ON}$) · In ((($V_{OH} - V_{OL}$) - V_M) / ($V_{OH} - V_{OL}$))

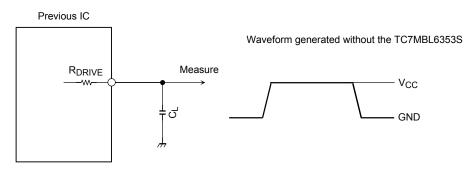
where, R_{DRIVE} is the output impedance of the previous-stage circuit.

Calculation example:

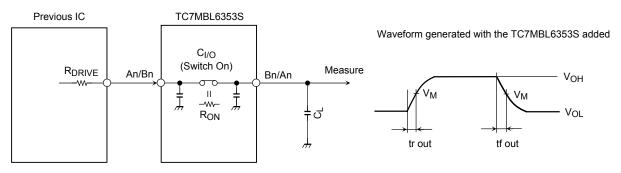
tr out (approx) = - (15 + 15)E-12 · (120 + 9) · ln (((3.0 - 0) - 1.5)/(3.0 - 0)) $\approx 2.7 \text{ ns}$

Calculation conditions:

 V_{CC} = 3.0V , C_L = 15pF , R_{DRIVE} = 120 Ω (output impedance of the previous IC), V_M = 1.5V (V_{CC} / 2) Output of the previous IC = digital (i.e., high-level voltage = V_{CC} ; low-level voltage = GND)



R_{DRIVE} = output impedance of the previous IC



R_{DRIVE} = output impedance of the previous IC

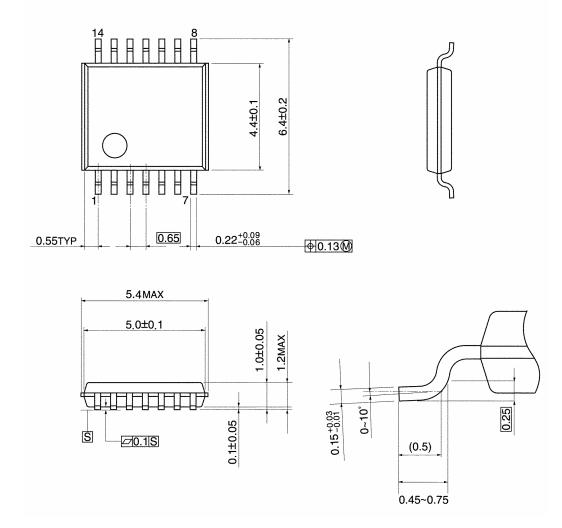
Paramete	-	V _{CC}					
i aramete	3.3 ± 0.3 V	$2.5 \pm 0.2 V$	1.8 ± 0.15 V				
VM	V _{CC} / 2	V _{CC} / 2	V _{CC} / 2				



Package Dimensions

TSSOP14-P-0044-0.65A

Unit: mm

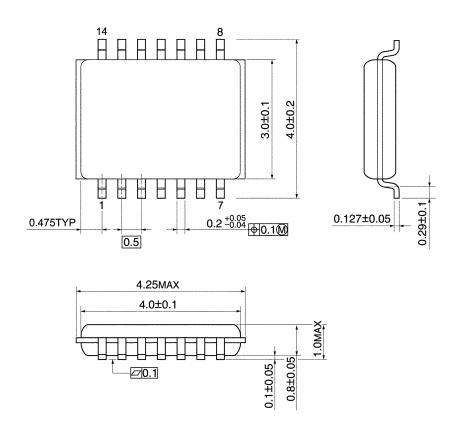


Weight: 0.06 g (typ.)

Package Dimensions

VSSOP14-P-0030-0.50

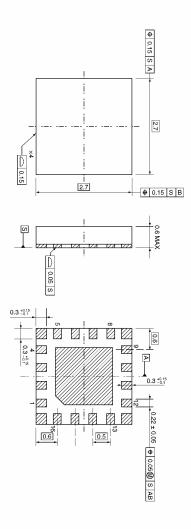
Unit: mm



Weight: 0.02 g (typ.)

Package Dimensions

VQON16-P-0303-0.50



Weight: 0.013 g (typ.)

Unit: mm

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20070701-EN GENERAL

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