WM8862

Multi-Channel High Definition Audio CODEC

DESCRIPTION

The WM8862 is a high performance PC audio subsystem for use in notebook, netbook, MID and tablet devices where a high level of audio performance is demanded. It is designed to minimise supporting components and board area, and enables the system designer to improve audio performance of a PC system while minimising design and implementation time.

The WM8862 is fully compliant with the High Definition Audio (HDA) interface specification (Revision 1.0), and also with the low-power DCN HDA015-B and dual-voltage DCN HDA024-A.

The device supports two stereo, single-ended analogue microphone/line inputs. This enables support for up to two analogue microphones inbuilt to a notebook screen, with simultaneous support for external microphone/line input connections. Microphone pre-amps are available, providing up to +30dB boost gain; a further pair of analogue PGAs provide an additional ±12dB of fine gain control. Two independent low-noise ECM bias sources are provided, further reducing the external system component count. The analogue inputs are digitised using high-performance multi-bit sigma-delta stereo ADCs.

Up to four digital microphones can be connected to the WM8862, providing support for advanced microphone arrays, eg. built into the lid of a portable PC system. Configurable notch filters are provided for the analogue or digital inputs, enabling known system noise sources (such as optical drives or fans) to be filtered from the audio input paths.

The WM8862 provides two stereo, 24-bit sigma-delta hi-fi DACs, supporting sample rates up to 192kHz. A ground-referenced headphone driver is provided, powered by an integrated charge pump, providing a true hi-fi performance output.

A stereo 2W/channel high-efficiency Class D speaker driver is also provided. Advanced digital signal processing is incorporated in the speaker path, enabling loudspeaker compensation to be realised using Wolfson's ReTune™ feature. Programmable compression / loudness control is also possible using the Dynamic Range Controller (DRC). This can be used at a hardware level to prevent very loud signals being applied to the speakers, avoiding distortion and damage.

Jack detect, GPIO functionality and an S/PDIF transmitter fully-compatible with IEC-60958-3 are also provided.

The CODEC and output drivers can operate from a single +5V supply, deriving all other necessary voltages using integrated regulators. The WM8862 supports separate I/O domains for the HDA interface and for the other digital interface pins, providing maximum system flexibility. The WM8862 is supplied in a small 48-pin QFN package.

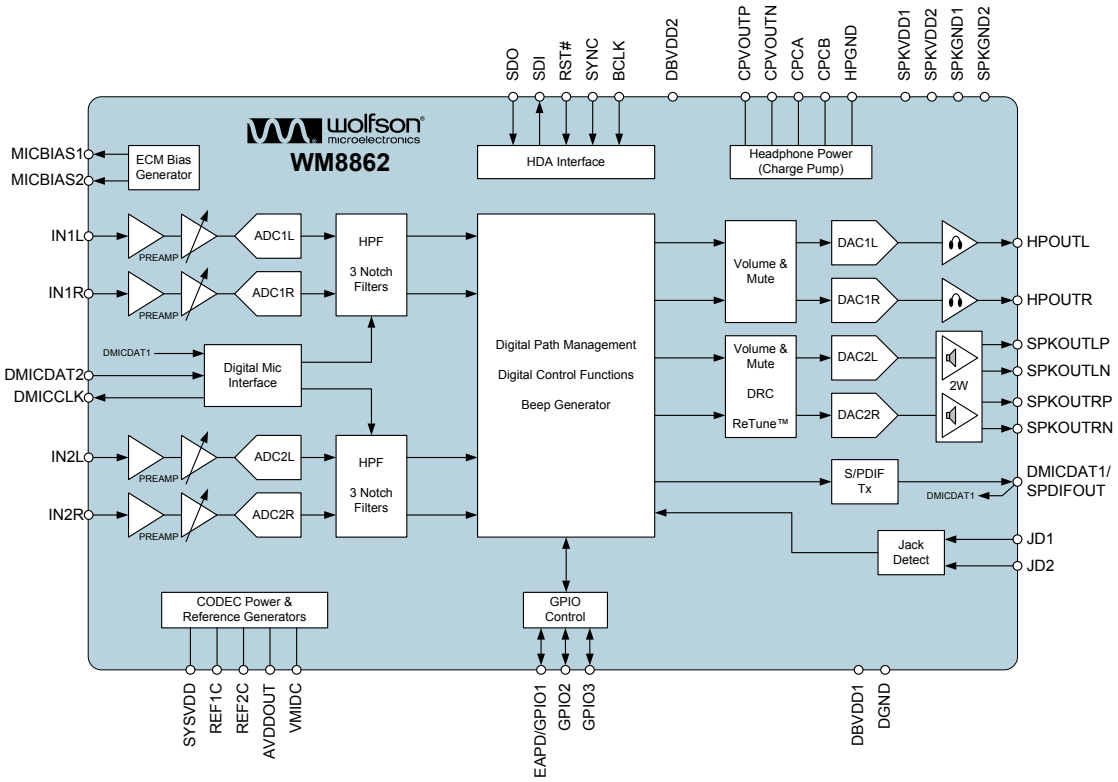
FEATURES

- Complete PC Audio Subsystem
- Fully Compatible with High Definition Audio Revision 1.0
  - Full support for low-power DCN HDA015-B
  - Full support for dual-voltage interface DCN HDA024-A
- Microsoft WLP Windows 7 logo compliant
  - Microsoft Windows Vista premium logo compliant
- Two Stereo Microphone/Line Inputs
  - 96dB SNR ('A-weighted')
  - -85dB THD
  - 44.1kHz to 96kHz sample rate support
  - 0dB to +30dB Mic boost, ±12dB PGA
- Stereo Capless Headphone/Line Output
  - 105dB SNR ('A-weighted')
  - -80dB THD (P_O = 40mW into 16Ω)
  - -90dB THD (0dBFS into 10kΩ)
  - 44.1kHz to 192kHz sample rate support
- Stereo Class D Speaker Output
  - 100dB SNR ('A-weighted')
  - -70dB THD (P_O=1W into 4Ω)
  - 1% THD (P_O=2W into 4Ω)
- Dynamic Range Controller
  - Compression and loudness on playback path
- Wolfson ReTune™
  - Speaker compensation
- Single-ended analogue microphone support
- Integrated dual microphone bias with impedance detect
- Four-channel digital microphone support
- Ground referenced stereo headphone driver
- 2W/channel stereo Class D speaker drivers
- IEC-60958-3 compatible S/PDIF transmitter
- Jack detect support
  - 4 Jack detect logic inputs
  - Support for combi-jacks, with impedance sensing
- GPIO Functionality
- EAPD support to control external subwoofer amplifier
- Digital beep generator with legacy analogue beep support
- Integrated Power Management
  - Low power operation
  - Integrated LDOs create required analogue and digital core supplies from +5V
- Independent digital I/O voltage domains:
  - HDA interface (DBVDD2): 1.41V to 3.6V
  - Other digital (DBVDD1): 1.62V to 3.6V
- 48-pin 7mm x 7mm QFN package

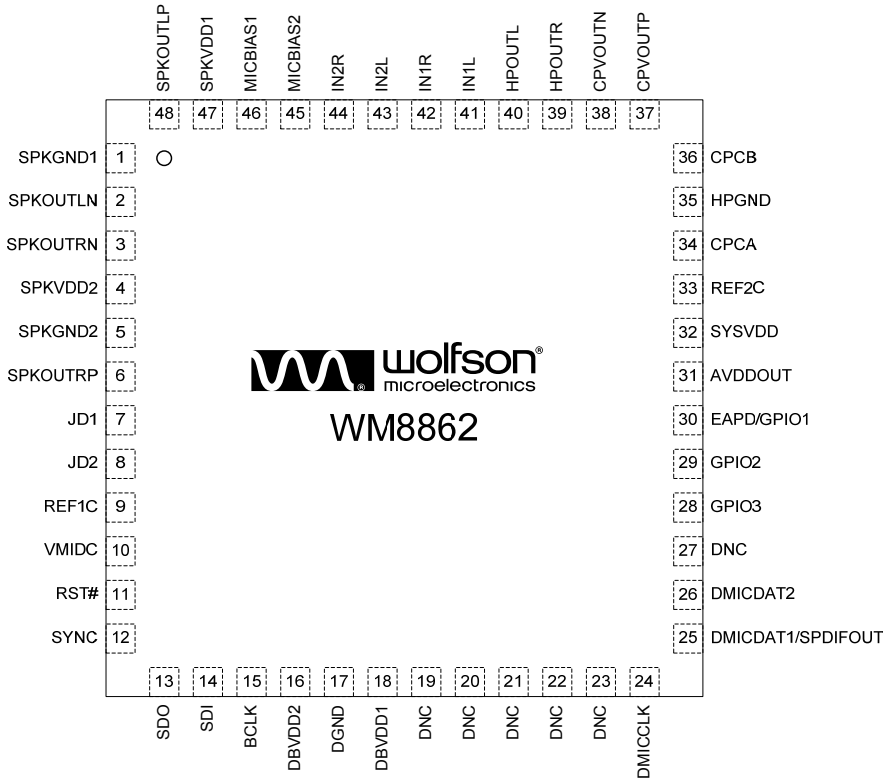
APPLICATIONS

- High performance computing
- Notebook PC
- Netbook PC
- Mobile Internet Devices (MID)
- Tablets

BLOCK DIAGRAM



PIN CONFIGURATION



ORDERING INFORMATION

ORDER CODE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM8862GEFL/V	-40°C to +85°C	48-pin QFN (Pb-free)	MSL3	260°C
WM8862GEFL/RV	-40°C to +85°C	48-pin QFN (Pb-free, Tape and reel)	MSL3	260°C

Note:
Reel quantity = 2200

PIN DESCRIPTION

PIN NO	NAME	TYPE	DESCRIPTION
P	PADDLE	Supply	Ground paddle connection
1	SPKGND1	Supply	Left Speaker driver ground
2	SPKOUTLN	Analogue output	Left Speaker negative output
3	SPKOUTRN	Analogue output	Right Speaker negative output
4	SPKVDD2	Supply	Right Speaker driver supply
5	SPKGND2	Supply	Right Speaker driver ground
6	SPKOUTRP	Analogue output	Right Speaker positive output
7	JD1	Analogue input	Jack detect sense 1
8	JD2	Analogue input	Jack detect sense 2
9	REF1C	Analogue output	Bandgap reference decoupling capacitor connection
10	VMIDC	Analogue output	Analogue midrail reference decoupling capacitor connection
11	RST#	Digital input	Global reset (active low)
12	SYNC	Digital input	HDA frame sync, 48kHz
13	SDO	Digital input	Serial data from HDA controller
14	SDI	Digital input / output	Serial data to HDA controller
15	BCLK	Digital input	HDA Link bit clock, 24MHz
16	DBVDD2	Supply	Digital buffer supply 2 (HDA link)
17	DGND	Supply	Digital Ground
18	DBVDD1	Supply	Digital buffer supply 1 (all digital input/output except HDA link)
19	DNC	n/a	Do Not Connect
20	DNC	n/a	Do Not Connect
21	DNC	n/a	Do Not Connect
22	DNC	n/a	Do Not Connect
23	DNC	n/a	Do Not Connect
24	DMICCLK	Digital output	Digital microphone clock output
25	DMICDAT1/ SPDIFOUT	Digital input / output	Digital microphone data input 1 / S/PDIF output
26	DMICDAT2	Digital input	Digital microphone data input 2
27	DNC	n/a	Do Not Connect
28	GPIO3	Digital input / output	General purpose digital input/output 3
29	GPIO2	Digital input / output	General purpose digital input/output 2
30	EAPD / GPIO1	Digital input / output	External Amplifier Power Down / General purpose digital input/output 1
31	AVDDOUT	Analogue output	Analogue supply rail (internally generated)
32	SYSVDD	Supply	Main system supply input
33	REF2C	Analogue output	Supplies reference decoupling capacitor connection
34	CPCA	Analogue output	Charge pump flyback capacitor pin 1
35	HPGND	Supply	Headphone driver ground
36	CPCB	Analogue output	Charge pump flyback capacitor pin 2
37	CPVOUTP	Analogue output	Headphone driver positive supply rail (internally generated)
38	CPVOUTN	Analogue output	Headphone driver negative supply rail (internally generated)
39	HPOUTR	Analogue output	Right Headphone output
40	HPOUTL	Analogue output	Left Headphone output
41	IN1L	Analogue input	Left channel 1 input
42	IN1R	Analogue input	Right channel 1 input
43	IN2L	Analogue input	Left channel 2 input
44	IN2R	Analogue input	Right channel 2 input
45	MICBIAS2	Analogue output	Microphone bias 2 output
46	MICBIAS1	Analogue output	Microphone bias 1 output
47	SPKVDD1	Supply	Left Speaker driver supply
48	SPKOUTLP	Analogue output	Left Speaker positive output

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
Main system supply voltage (SYSVDD)	-0.3V	+7V
Speaker drivers supply voltage (SPKVDD1, SPKVDD2)	-0.3V	+7V
Digital buffer supply voltage (DBVDD1, DBVDD2)	-0.3V	+7V
Voltage range digital inputs (excluding HDA link)	DGND -0.3V	DBVDD1 +0.3V
Voltage range digital inputs (HDA link)	DGND -0.3V	DBVDD2 +0.3V
Voltage range analogue inputs	AGND -0.3V	+3.6V
Operating temperature range, T_A	-40ºC	+85ºC
Junction temperature, T_J	-40ºC	+150ºC
Storage temperature after soldering	-65ºC	+150ºC
Thermal Resistance, Θ_{JA}	29°C/W	

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Main system supply voltage	SYSVDD	4.5	5.0	5.5	V
Speaker drivers supply voltage	SPKVDD1, SPKVDD2	4.5	5.0	5.5	V
Digital buffer supply voltage	DBVDD1	1.62	1.8 to 3.3	3.6	V
Digital buffer supply voltage	DBVDD2	1.41	1.5 to 3.3	3.6	V
Ground	DGND, AGND, HPGND		0		V

Notes:

1. Analogue and digital grounds must always be within 0.3V of each other.
2. All digital and analogue supplies are completely independent from each other (i.e. not internally connected).

ELECTRICAL CHARACTERISTICS

Test Conditions

SYSVDD = SPKVDD1 = SPKVDD2 = 5.0V. DBVDD1 = 3.3V. DBVDD2 = 3.3V.
T_A = +25°C, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analogue Inputs (IN1L, IN1R)						
Full-scale Input signal level	V_{INFS}			1.1 0		Vrms dBV
Input resistance	R_{IN}	+42dB gain		2.2		kΩ
		0dB gain		150		
Input capacitance	C_{IN}			10		pF
Input Gain Boost (Port-B node)						
Programmable Gain				0, 10, 20, 30		dB
Input Programmable Gain Amplifier (PGA1 node)						
Programmable Gain			-12		12	dB
Programmable Gain Step Size		Guaranteed monotonic		0.5		dB
PGA Gain accuracy				TBD		
PGA noise		20Hz - 20kHz, A-weighted		-100		dBV
Analogue Record Path (IN1L, IN1R to ADC1)						
Signal to Noise Ratio	SNR	A-weighted		96		dB
Total Harmonic Distortion	THD	-1dBFS output		TBD		dB
Total Harmonic Distortion Plus Noise	THD+N	-1dBFS output		-85		dB
Dynamic Range	DNR	A-weighted, -60dBFS input		96		dB
Channel Separation		1kHz		90		dB
		10kHz		85		
Power Supply Rejection Ratio (SYSVDD)	PSRR	100mV(peak-peak) 1kHz		TBD		dB
		100mV(peak-peak) 20kHz		TBD		
Channel Level Matching				+/-0.1		dB
Channel Phase Deviation				+/-0.1		degrees
Microphone Bias Output (MICBIAS1)						
Output voltage	$V_{MICBIAS1}$	VrefEn = 1h		1.65		V
		VrefEn = 4h		2.64		
Power Supply Rejection Ratio (SYSVDD)	PSRR			TBD		dB
Bias Current					3	mA
Output noise spectral density				20		nV/√Hz

Test Conditions

SYSVDD = SPKVDD1 = SPKVDD2 = 5.0V. DBVDD1 = 3.3V. DBVDD2 = 3.3V.

T_A = +25°C, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analogue Inputs (IN2L, IN2R)						
Full-scale Input signal level	V_{INFS}			1.1 0		Vrms dBV
Input resistance	R_{IN}	+42dB gain		2.2		kΩ
		0dB gain		150		
Input capacitance	C_{IN}			10		pF
Input Gain Boost (Port-C node)						
Programmable Gain				0, 10, 20, 30		dB
Input Programmable Gain Amplifier (PGA2 node)						
Programmable Gain			-12		12	dB
Programmable Gain Step Size		Guaranteed monotonic		0.5		dB
PGA Gain accuracy				TBD		
PGA noise		20Hz - 20kHz, A-weighted		-100		dBV
Analogue Record Path (IN2L, IN2R to ADC2)						
Signal to Noise Ratio	SNR	A-weighted		96		dB
Total Harmonic Distortion	THD	-1dBFS output		TBD		dB
Total Harmonic Distortion Plus Noise	THD+N	-1dBFS output		-85		dB
Dynamic Range	DNR	A-weighted, -60dBFS input		96		dB
Channel Separation		1kHz		90		dB
		10kHz		85		
Power Supply Rejection Ratio (SYSVDD)	PSRR	100mV(peak-peak) 1kHz		TBD		dB
		100mV(peak-peak) 20kHz		TBD		
Channel Level Matching				+/-0.1		dB
Channel Phase Deviation				+/-0.1		degrees
Microphone Bias Output (MICBIAS2)						
Output voltage	$V_{MICBIAS2}$	VrefEn = 1h		1.65		V
		VrefEn = 4h		2.64		
Power Supply Rejection Ratio (SYSVDD)	PSRR			TBD		dB
Bias Current					3	mA
Output noise spectral density				20		nV/√Hz

Test Conditions

SYSVDD = SPKVDD1 = SPKVDD2 = 5.0V. DBVDD1 = 3.3V. DBVDD2 = 3.3V.
T_A = +25°C, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Microphone Inputs (DMICDAT1 to ADC1, DMICDAT2 to ADC2)						
Input HIGH Level	V_{IH}		0.7 × DBVDD1			V
Input LOW Level	V_{IL}				0.3 × DBVDD1	V
Input capacitance	C_{IN}			10		pF
Input leakage			-0.9		0.9	µA
Programmable Gain			-12		32	dB
Programmable Gain Step Size		Guaranteed monotonic		0.5		dB
DMICCLK frequency		44.1kHz sample rate		2.8224		MHz
		48kHz, 96kHz sample rate		3.072		
S/PDIF Transmitter (SPDIF Out)						
Output HIGH Level	V_{OH}	I_{OH}=1mA	0.9 × DBVDD1			V
Output LOW Level	V_{OL}	I_{OL}=-1mA			0.1 × DBVDD1	V
Output Source/Sink Current					3	mA

Test Conditions

SYSVDD = SPKVDD1 = SPKVDD2 = 5.0V. DBVDD1 = 3.3V. DBVDD2 = 3.3V.

T_A = +25°C, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Headphone Playback Path (DAC1 to HPOUTL, HPOUTR) - 10kΩ line load						
Signal to Noise Ratio	SNR	A-weighted		105		dB
Total Harmonic Distortion	THD	$1V_{RMS}$ output		TBD		dB
Total Harmonic Distortion Plus Noise	THD+N	$1V_{RMS}$ output		-90		dB
Dynamic Range	DNR	A-weighted, -60dBFS input		105		dB
Channel Separation		1kHz		90		dB
		10kHz		90		
Power Supply Rejection Ratio (SYSVDD)	PSRR	100mV(peak-peak) 1kHz		TBD		dB
		100mV(peak-peak) 20kHz		TBD		
DC offset at load					+/-1	mV
Headphone Playback Path (DAC1 to HPOUTL, HPOUTR) - 32Ω headphone load						
Signal to Noise Ratio	SNR	A-weighted		100		dB
Total Harmonic Distortion	THD	20mW output		TBD		dB
Total Harmonic Distortion Plus Noise	THD+N	20mW output		-80		dB
Dynamic Range	DNR	A-weighted, -60dBFS input		100		dB
Channel Separation		1kHz		90		dB
		10kHz		87		
Power Supply Rejection Ratio (SYSVDD)	PSRR	100mV(peak-peak) 1kHz		TBD		dB
		100mV(peak-peak) 20kHz		TBD		
DC offset at load					+/-1	
Headphone Outputs (HPOUTL, HPOUTR)						
Full-scale Output signal level		Full-scale input, R_L=10kΩ		2		V_{RMS}
Output power	P_O	0.1% THD+N, R_L=16Ω		40		mW
Minimum load resistance	R_L			16		Ω
Load resistance	R_L	Automatic headset detect function enabled	12.8		300	Ω
Maximum load capacitance	C_L			220		pF

Test Conditions

SYSVDD = SPKVDD1 = SPKVDD2 = 5.0V. DBVDD1 = 3.3V. DBVDD2 = 3.3V.
T_A = +25°C, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Speaker Playback Path (DAC2 to SPKOUTLP, SPKOUTLN, SPKOUTRP, SPKOUTRN) - 8Ω BTL load						
Signal to Noise Ratio	SNR	A-weighted		100		dB
Total Harmonic Distortion	THD	500mW output		TBD		dB
Total Harmonic Distortion Plus Noise	THD+N	500mW output		-70		dB
Dynamic Range	DNR	A-weighted, -60dBFS input		100		dB
Channel Separation		1kHz		70		dB
		10kHz		TBD		
PSRR (SPKVDD)	PSRR	100mV(peak-peak) 1kHz		TBD		dB
		100mV(peak-peak) 20kHz		TBD		
DC offset at load						
Speaker Playback Path (DAC2 to SPKOUTLP, SPKOUTLN, SPKOUTRP, SPKOUTRN) - 4Ω BTL load						
Signal to Noise Ratio	SNR	A-weighted		100		dB
Total Harmonic Distortion	THD	1W output		TBD		dB
Total Harmonic Distortion Plus Noise	THD+N	1W output		-70		dB
Dynamic Range	DNR	A-weighted, -60dBFS input		100		dB
Channel Separation		1kHz		70		dB
		10kHz		TBD		
Power Supply Rejection Ratio (SPKVDD)	PSRR	100mV(peak-peak) 1kHz		TBD		dB
		100mV(peak-peak) 20kHz		TBD		
DC offset at load						
Speaker Outputs (SPKOUTLP, SPKOUTLN, SPKOUTRP, SPKOUTRN)						
Output power	P_O	1% THD+N, R_L=8Ω		1		W
		1% THD+N, R_L=4Ω		2		
Minimum load resistance	R_L			4		Ω
Maximum load capacitance	C_L			220		pF

Test Conditions

SYSVDD = SPKVDD1 = SPKVDD2 = 5.0V. DBVDD1 = 3.3V. DBVDD2 = 3.3V.

T_A = +25°C, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Input / Output (GPIO1, GPIO2, GPIO3)						
Input HIGH Level	V_{IH}		0.7 × DBVDD1			V
Input LOW Level	V_{IL}				0.3 × DBVDD1	V
Output HIGH Level	V_{OH}	I_{OH}=1mA	0.9 × DBVDD1			V
Output LOW Level	V_{OL}	I_{OL}=-1mA			0.1 × DBVDD1	V
Input capacitance	C_{IN}			10		pF
Input leakage			-0.9		0.9	µA
Digital Input / Output (SDO, SDI, RST#, SYNC, BCLK)						
Input HIGH Level	V_{IH}		0.7 × DBVDD2			V
Input LOW Level	V_{IL}				0.3 × DBVDD2	V
Output HIGH Level	V_{OH}	I_{OH}=1mA	0.9 × DBVDD2			V
Output LOW Level	V_{OL}	I_{OL}=-1mA			0.1 × DBVDD2	V
Input capacitance	C_{IN}			10		pF
Input leakage			-0.9		0.9	µA

TERMINOLOGY

1. Signal-to-Noise Ratio (dB) – SNR is a measure of the difference in level between the maximum full scale output signal and the output with no input signal applied. (Note that this is measured without any mute function enabled.)
2. Total Harmonic Distortion (dB) – THD is the level of the rms value of the sum of harmonic distortion products in the specified bandwidth (see note below) relative to the amplitude of the measured output signal.
3. Total Harmonic Distortion plus Noise (dB) – THD+N is the level of the rms value of the sum of harmonic distortion products plus noise in the specified bandwidth (see note below) relative to the amplitude of the measured output signal.
4. Channel Separation (L/R) (dB) – left-to-right and right-to-left channel separation is the measured signal level in the idle channel at the test signal frequency relative to the signal level at the output of the active channel. The active channel is configured and supplied with an appropriate input signal to drive a full scale output, with signal measured at the output of the associated idle channel.
5. Dynamic range (dB) - DNR is a measure of the difference between the maximum full scale output signal level and the sum of all harmonic distortion products plus noise with a low level input signal applied. Typically, an input signal level 60dB below full scale is used.
6. Mute Attenuation (dB) – This is a measure of the difference in level between the full scale output signal and the output with mute applied.
7. All performance measurements are specified with 20kHz low pass filter and, where noted, an A-weighted filter. Failure to use such a filter will result in higher THD and lower SNR readings than are found in the Electrical Characteristics. The low pass filter removes out of band noise; although it is not audible, it may affect dynamic specification values.

INTRODUCTION

The WM8862 is a high performance PC audio subsystem. It offers full compatibility with the Intel High Definition Audio (HDA) specification revision 1.0, allowing seamless integration with industry-standard HDA controllers.

The WM8862 has two high-performance stereo ADCs to provide hi-fi quality analogue line-in and microphone input digitisation. A low noise microphone bias with programmable output voltage is provided, ideally suited as a bias current source for ECM microphones. Additionally, the CODEC contains a digital microphone interface capable of supporting up to four independent digital microphones, allowing high quality microphone array implementations to be realised.

The WM8862 has two high-performance stereo DACs, matched with output drivers for direct connection to stereo headphone and stereo speakers. The headphone output driver incorporates advanced charge pump and DC servo technology to provide ground-referenced output, minimising system cost and PCB space without compromise on audio quality. The Class D speaker drivers support up to 2W/channel power output, with speakers driven in differential (BTL) configuration.

Advanced digital signal processing is incorporated in the speaker path, enabling loudspeaker compensation to be realised using Wolfson's ReTune™ feature. Programmable compression / loudness control is also possible using the Dynamic Range Controller (DRC). This can be used at a hardware level to prevent very loud signals being applied to the speakers, avoiding distortion and damage.

A S/PDIF transmitter is provided, fully compatible with IEC-60958-3. A beep generator, GPIO pins and jack detect capability are also integrated on the WM8862. The WM8862 supports up to 4 jack detect logic inputs, and can also perform impedance sensing. Impedance sensing provides support for microphone/headphone combi-jacks, by enabling detection of different types of external accessories.

This datasheet assumes familiarity with the High Definition Audio Specification Revision 1.0, available from http://www.intel.com/standards/hdaudio/. For those verbs implemented in the WM8862 which are as defined in the High Definition Audio Specification Revision 1.0 there is no detailed text describing their use in this datasheet. However, detailed text describing the function of of vendor-specific verbs is provided. Additionally, a full list of each node and each verb implemented in the WM8862 is provided at the rear of the document.

APPLICATIONS INFORMATION

RECOMMENDED EXTERNAL COMPONENTS

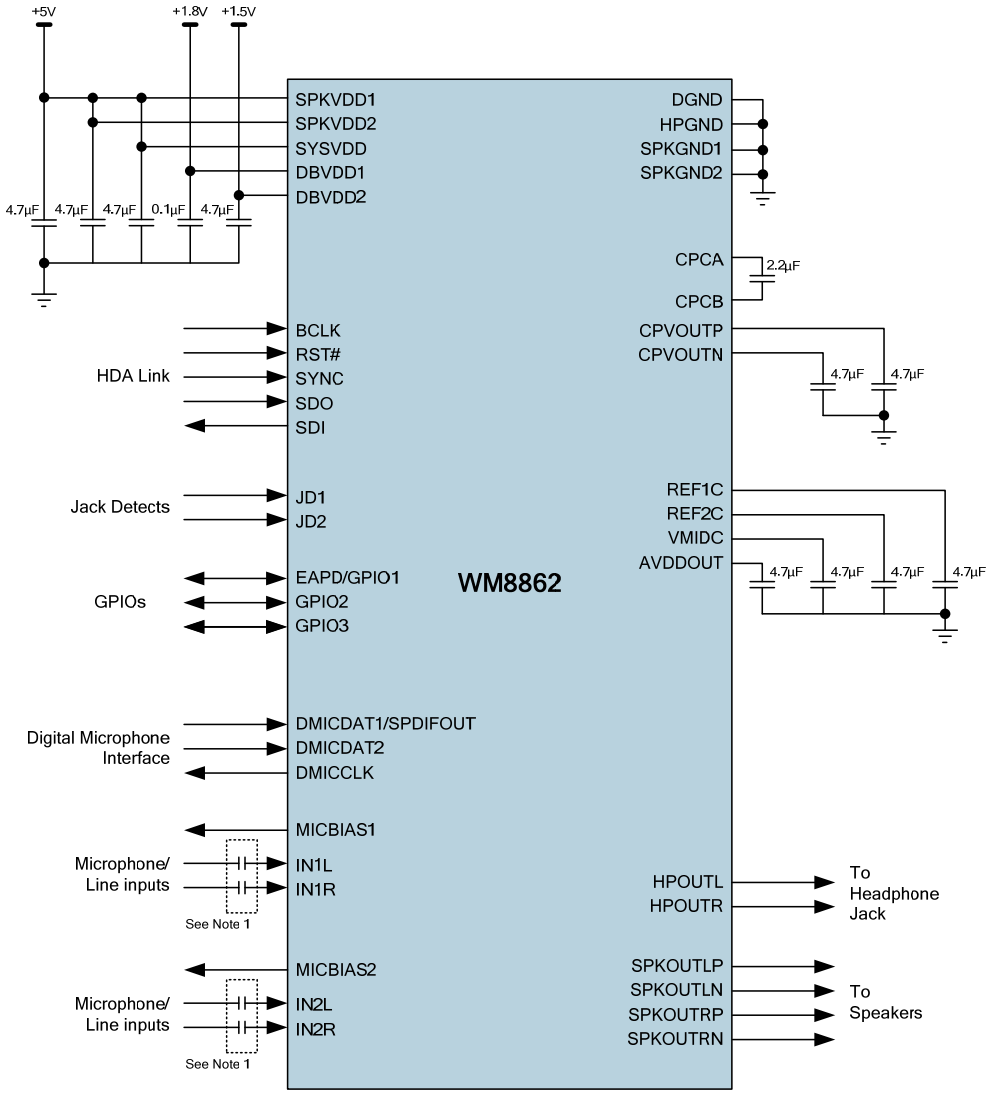


Figure 1 Recommended External Components

Notes:

1. The choice of AC-coupling input capacitors may depend on the application requirements. Typical values in the range 1µF to 10µF are recommended. See also Note 5.
2. When MICBIAS1 or MICBIAS2 is used to provide bias to an electret condenser microphone (ECM), a bias resistor is required between MICBIAS and the microphone. The choice of microphone bias resistor may depend on the microphone. A typical value is 2.2kΩ. See also Note 5.
3. The capacitor between CPCA and CPCB must be placed as close as possible to the WM8862.
4. The decoupling capacitors on CPVOUTP and CPVOUTN must also be placed as close as possible to the WM8862.
5. If the Headset Detect function is used, specific component requirements are applicable.

JACK DETECT EXTERNAL COMPONENTS

The WM8862 supports Jack Detect functions on 6 different input/output ports. This is implemented in accordance with the High Definition Audio Specification Revision 1.0, Section 7.4.2, and requires the external components shown in Figure 2.

Note that the required tolerance on the resistors is 1% or better.

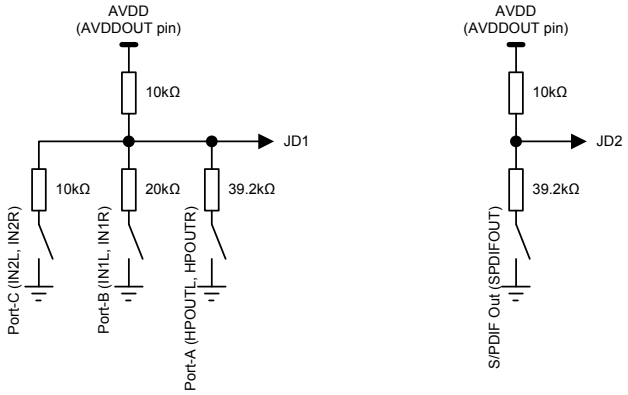
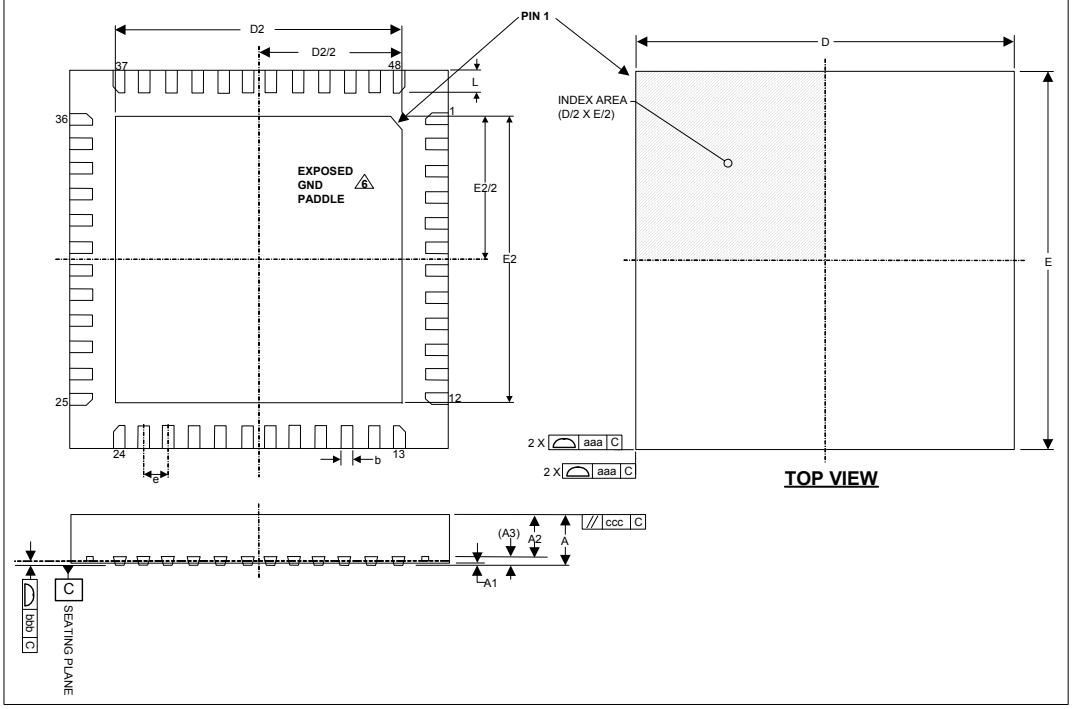


Figure 2 Jack Detect External Components

PACKAGE DIMENSIONS

FL: 48 PIN QFN PLASTIC PACKAGE 7 x 7 x 0.75 mm BODY, 0.50 mm LEAD PITCH **DM079.A**



Symbols	Dimensions (mm)			
	MIN	NOM	MAX	NOTE
A	0.7	0.75	0.8	
A1	0	0.035	0.05	
A2	-	0.55	0.57	
A3		0.203 REF		
b	0.20	0.25	0.30	1
D		7.00 BSC		
D2	5.55	5.65	5.75	
E		7.00 BSC		
E2	5.55	5.65	5.75	
e		0.5 BSC		
L	0.35	0.4	0.45	
Tolerances of Form and Position				
aaa	0.10			
bbb	0.08			
ccc	0.10			
REF	JEDEC, MO-220			

NOTES:
1. DIMENSION b APPLIED TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 mm AND 0.30 mm FROM TERMINAL TIP.
2. ALL DIMENSIONS ARE IN MILLIMETRES
3. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-002.
4. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
5. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
6. REFER TO APPLICATIONS NOTE WAN_0118 FOR FURTHER INFORMATION.

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REVISION HISTORY

DATE	REV	ORIGINATOR	CHANGES
20/10/11	2.0	JMacD/NB	First Release
13/12/11	2.1	JMacD	Order codes corrected to show - WM8862GEFL/V and WM8862GEFL/RV.