

## Multi-Channel High Definition Audio CODEC

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### DESCRIPTION

The WM8860 is a high performance multi-channel audio CODEC designed for high performance portable PC audio systems. The device offers full compatibility with the Intel High Definition Audio (HDA) specification revision 1.0, allowing seamless integration with industry-standard HDA controllers.

The WM8860 has two high performance stereo DACs to enable four channels of high definition audio. A high-performance ground-referenced stereo headphone amplifier utilises advanced charge pump and DC servo technology to minimise system cost and space without compromise on audio quality. A balanced line output, which can provide a differential connection to an external speaker amplifier, is also provided and enables common mode noise rejection when these traces are routed across a PCB.

The WM8860 also has two high performance stereo ADCs to provide Hi-Fi quality analogue line-in and microphone input digitisation. A low noise microphone bias with programmable output voltage is provided. Additionally, the CODEC contains a digital microphone interface capable of supporting up to four independent digital microphones. One differential stereo input is provided for line level signals, while one pseudo-differential stereo input with integrated microphone preamplifier is provided.

The WM8860 also contains a S/PDIF transmitter which is fully compatible with IEC-60958-3. Two dedicated GPIO pins are provided, enabling control of external amplifiers or other additional system components.

The WM8860 is supplied in a small 48-pin QFN package.

### FEATURES

- Multi-channel High Definition Audio CODEC
- Fully compatible with Intel High Definition Audio Revision 1.0
- 4-Channel DAC, 4-channel ADC
- DAC sampling frequency 8kHz - 192kHz
- ADC sampling frequency 8kHz - 96kHz
- DAC Performance:
  - SNR 108 dB ('A' weighted)
  - SNR 105dB (non weighted)
  - THD -96dB (at 0dBFS)
- ADC Performance:
  - SNR 105 dB ('A' weighted)
  - SNR 102dB (non weighted)
  - THD -95dB (at -1dBFS)
- Ground-referenced stereo headphone driver
- Differential line inputs/outputs
- Stereo microphone interface with integrated pre-amp
- Multi-channel digital microphone interface
- IEC-60958-3 compatible S/PDIF transmitter
- Jack detect and load impedance sensing
- Beep generator
- GPIO functionality
- IEEE-754 Single precision 32-bit floating point support
- Power supplies
  - Digital core: 1.62V – 1.98V
  - Digital buffer: 2.97V – 3.63V
  - Analogue: 4.5V – 5.5V
  - Charge pump: 4.5V – 5.5V
- 48-pin 7mm x 7mm QFN package

### APPLICATIONS

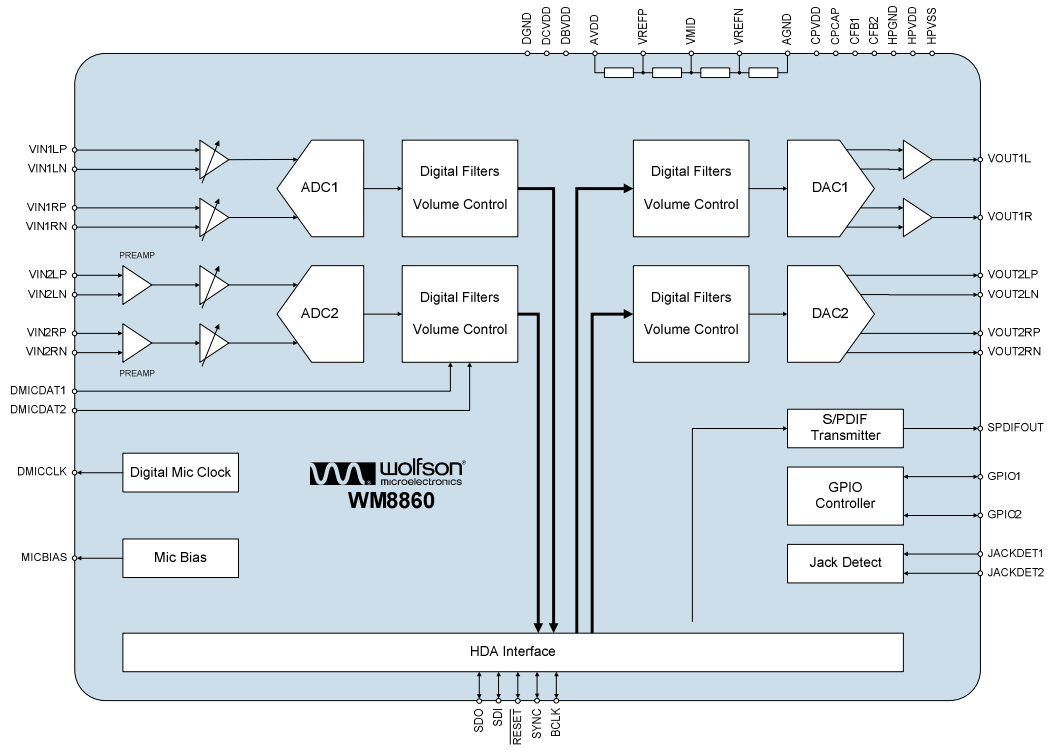
- High performance PC audio
- All-in-one desktop PC
- Notebook PC

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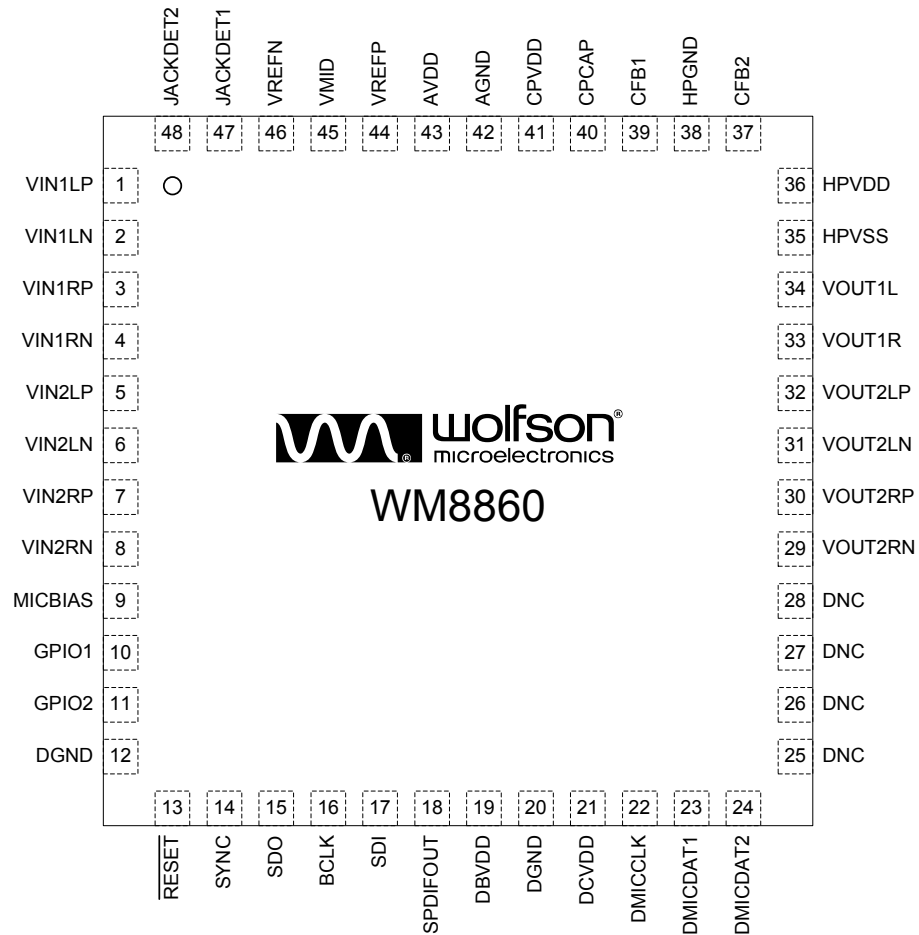
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**BLOCK DIAGRAM**



**PIN CONFIGURATION**



**ORDERING INFORMATION**

ORDER CODE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM8860GEFL/V	-40°C to +85°C	48-pin QFN (Pb-free)	MSL3	260°C
WM8860GEFL/RV	-40°C to +85°C	48-pin QFN (Pb-free, tape and reel)	MSL3	260°C

**Note:**

Reel quantity = 2200

**PIN DESCRIPTION**

PIN NO	NAME	TYPE	DESCRIPTION
1	VIN1LP	Analogue input	Left channel 1 positive input
2	VIN1LN	Analogue input	Left channel 1 negative input
3	VIN1RP	Analogue input	Right channel 1 positive input
4	VIN1RN	Analogue input	Right channel 1 negative input
5	VIN2LP	Analogue input	Left channel 2 positive input
6	VIN2LN	Analogue input	Left channel 2 negative input
7	VIN2RP	Analogue input	Right channel 2 positive input
8	VIN2RN	Analogue input	Right channel 2 negative input
9	MICBIAS	Analogue output	Microphone bias output
10	GPIO1	Digital input / output	General purpose digital input/output 1
11	GPIO2	Digital input / output	General purpose digital input/output 2
12	DGND	Supply input	Digital ground (return for DBVDD and DCVDD)
13	/RESET	Digital input	Global reset (active low)
14	SYNC	Digital input	HDA frame sync, 48kHz
15	SDO	Digital input	Serial data output from HDA controller
16	BCLK	Digital input	HDA Link bit clock, 24MHz
17	SDI	Digital input / output	Serial data input to HDA controller
18	SPDIFOUT	Digital output	S/PDIF output
19	DBVDD	Supply input	Digital buffer supply input
20	DGND	Supply input	Digital ground (return for DBVDD and DCVDD)
21	DCVDD	Supply input	Digital core supply input
22	DMICCLK	Digital output	Digital microphone clock output
23	DMICDAT1	Digital input	Digital microphone data input 1
24	DMICDAT2	Digital input / output	Digital microphone data input 2
25	DNC		Reserved - Do not connect
26	DNC		Reserved - Do not connect
27	DNC		Reserved - Do not connect
28	DNC		Reserved - Do not connect
29	VOUT2RN	Analogue output	Right channel 2 negative output
30	VOUT2RP	Analogue output	Right channel 2 positive output
31	VOUT2LN	Analogue output	Left channel 2 negative output
32	VOUT2LP	Analogue output	Left channel 2 positive output
33	VOUT1R	Analogue output	Right channel 1 output
34	VOUT1L	Analogue output	Left channel 1 output
35	HPVSS	Supply output	Charge pump negative supply decoupling point
36	HPVDD	Supply output	Charge pump positive supply decoupling point
37	CFB2	Analogue output	Charge pump flyback capacitor pin 2
38	HPGND	Supply input	Charge pump ground (return path for HPVDD and HPVSS)
39	CFB1	Analogue output	Charge pump flyback capacitor pin 1
40	CPCAP	Supply output	Internally generated regulated charge pump supply decoupling point
41	CPVDD	Supply input	Charge pump supply input
42	AGND	Supply input	Analogue ground (return path for AVDD and CPVDD)
43	AVDD	Supply input	Analogue supply input
44	VREFP	Analogue output	Analogue positive reference decoupling point
45	VMID	Analogue output	Midrail voltage decoupling point
46	VREFN	Analogue output	Analogue negative reference decoupling point
47	JACKDET1	Analogue output	Jack detect sense 1
48	JACKDET2	Analogue output	Jack detect sense 2

## ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.



ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.

MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
Analogue supply voltage (AVDD)	-0.3V	+7V
Charge pump supply voltage (CPVDD)	-0.3V	+7V
Digital core supply voltage (DCVDD)	-0.3V	+2.5V
Digital buffer supply voltage (DBVDD)	-0.3V	+7V
Voltage range digital inputs	DGND -0.3V	DBVDD +0.3V
Voltage range analogue inputs	AGND -0.3V	AVDD +0.3V
Operating temperature range, T <sub>A</sub>	-40°C	+85°C
Junction temperature, T <sub>JMAX</sub>	-40°C	+150°C
Storage temperature after soldering	-65°C	+150°C

## RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
<b>CODEC Power Supplies</b>					
Digital core supply range	DCVDD	1.62	1.8	1.98	V
Digital buffer supply range	DBVDD	2.97	3.3	3.63	V
Analogue supply range	AVDD	4.5	5.0	5.5	V
Charge pump supply range	CPVDD	4.5	5.0	5.5	V
Ground	DGND, AGND, HPGND		0		V

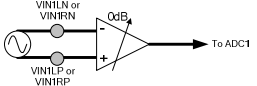
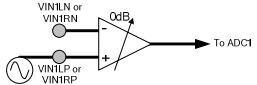
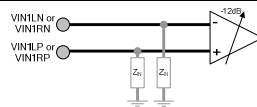
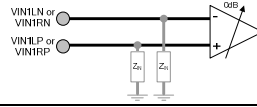
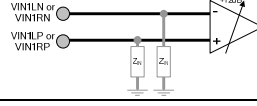
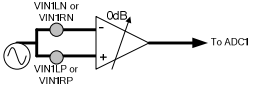
### Notes:

- Analogue and digital grounds must always be within 0.3V of each other.
- All digital and analogue supplies are completely independent from each other (i.e. not internally connected).

## ELECTRICAL CHARACTERISTICS

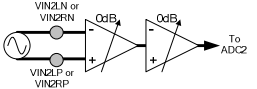
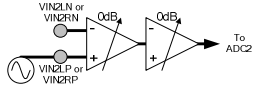
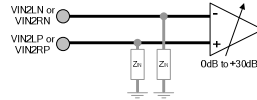
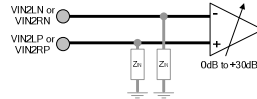
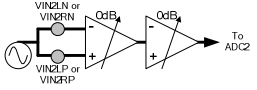
### Test Conditions

AVDD = CPVDD = 5V, DBVDD = 3.3V, DCVDD = 1.8V,  $T_A = +25^\circ\text{C}$ , 1kHz signal,  $f_s = 48\text{kHz}$ , 24-bit data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>Analogue Input 1 (VIN1LP, VIN1LN, VIN1RP, VIN1RN)</b>						
Maximum Differential Input Signal Level	$V_{INDIFF(max)}$	0dB gain 		2.25 x AVDD/5		$V_{RMS}$
Maximum Single-ended Input Signal Level	$V_{INSE(max)}$	0dB gain 		1.6 x AVDD/5		$V_{RMS}$
Input impedance	$Z_{IN}$	-12dB gain 		42		k $\Omega$
		0dB gain 		27		k $\Omega$
		+12dB gain 		9		k $\Omega$
Common Mode Rejection Ratio	CMRR	20Hz to 20kHz 		55		dB
Minimum PGA Gain Setting				-12		dB
Maximum PGA Gain Setting				+12		dB
PGA Gain Step Size		Guaranteed monotonic		0.5		dB

**Test Conditions**

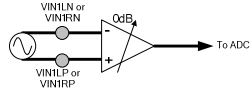
AVDD = CPVDD = 5V, DBVDD = 3.3V, DCVDD = 1.8V, T<sub>A</sub> = +25°C, 1kHz signal, f<sub>s</sub> = 48kHz, 24-bit data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>Analogue Input 2 (VIN2LP, VIN2LN, VIN2RP, VIN2RN)</b>						
Maximum Differential Input Signal Level	V <sub>INDIFF(max)</sub>	0dB gain 		2.25 x AVDD/5		V <sub>RMS</sub>
Maximum Single-ended Input Signal Level	V <sub>INSE(max)</sub>	0dB gain 		1.1 x AVDD/5		V <sub>RMS</sub>
Input impedance	Z <sub>IN</sub>	Single-ended or Differential (Inverting) 		10		kΩ
		Differential (Non-inverting) 		120		kΩ
Common Mode Rejection Ratio	CMRR	20Hz to 20kHz 		65		dB
Microphone Preamp Gain Options				0 10 20 30		dB
Minimum PGA Gain Setting				-12		dB
Maximum PGA Gain Setting				+12		dB
PGA Gain Step Size		Guaranteed monotonic		0.5		dB



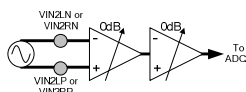
**Test Conditions**AVDD = CPVDD = 5V, DBVDD = 3.3V, DCVDD = 1.8V, T<sub>A</sub> = +25°C, 1kHz signal, fs = 48kHz, 24-bit data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>ADC1 Performance</b>						
Signal to Noise Ratio	SNR	Unweighted		102		dB
		A-weighted	100	105		dB
		A-weighted fs=96kHz		105		dB
Dynamic Range	DNR	A-weighted -60dBFS		105		dB
Total Harmonic Distortion	THD	-1dBFS		-95	-90	dB
		-1dBFS fs=96kHz		-95		dB
Channel Separation		1kHz		86		dB
		20Hz to 20kHz		86		dB
Channel Level Matching		0dBFS		0.1		dB
Channel Phase Deviation				0.01		°
Power Supply Rejection Ratio	PSRR	1kHz, 100mVpp on AVDD		90		dB
		20Hz to 20kHz, 100mVpp on AVDD		70		dB



**Test Conditions**AVDD = CPVDD = 5V, DBVDD = 3.3V, DCVDD = 1.8V, T<sub>A</sub> = +25°C, 1kHz signal, fs = 48kHz, 24-bit data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>ADC2 Performance</b>						
Signal to Noise Ratio	SNR	Unweighted		100		dB
		A-weighted		95	103	dB
		A-weighted fs=96kHz			103	
Dynamic Range	DNR	A-weighted -60dBFS		103		dB
Total Harmonic Distortion	THD	-1dBFS		-95	-90	dB
Channel Separation		1kHz		87		dB
		20Hz to 20kHz		84		dB
Channel Level Matching		0dBFS		0.1		dB
Channel Phase Deviation				0.01		°
Power Supply Rejection Ratio	PSRR	1kHz, 100mVpp on AVDD		90		dB
		20Hz to 20kHz, 100mVpp on AVDD		70		dB

**Test Conditions**AVDD = CPVDD = 5V, DBVDD = 3.3V, DCVDD = 1.8V, T<sub>A</sub> = +25°C, 1kHz signal, fs = 48kHz, 24-bit data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>Microphone Bias Generator</b>						
Output Voltage		VRefEn[2:0] = 001		0.5x AVDD		V
		VRefEn[2:0] = 100		0.8x AVDD		V
Current Source Capability					2.5	mA
Power Supply Rejection Ratio	PSRR	1kHz, 100mVpp on AVDD		100		dB
		20Hz to 20kHz, 100mVpp on AVDD		88		dB

**Test Conditions**

AVDD = CPVDD = 5V, DBVDD = 3.3V, DCVDD = 1.8V, T<sub>A</sub> = +25°C, 1kHz signal, fs = 48kHz, 24-bit data unless otherwise stated.

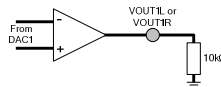
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>Digital Microphone Interface</b>						
Digital Microphone Clock Frequencies				1.024 1.4112 2.048 2.8224 3.072		MHz
Signal to Noise Ratio	SNR			96		dB
Minimum Digital Gain Setting				-12		dB
Maximum Digital Gain Setting				+32		dB
Digital Gain Step Size				0.5		dB

**Test Conditions**AVDD = CPVDD = 5V, DBVDD = 3.3V, DCVDD = 1.8V,  $T_A = +25^\circ\text{C}$ , 1kHz signal,  $f_s = 48\text{kHz}$ , 24-bit data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>Analogue Output 1 (VOUT1L, VOUT1R)</b>						
Full Scale Output Signal Level	$V_{OUT}$	$R_L = 1\text{k}\Omega$ to $47\text{k}\Omega$ H-Phn Enable = 0			$2 \times$ AVDD/5	$V_{RMS}$
		$R_L = 16\Omega$ to $1\text{k}\Omega$ H-Phn Enable = 1			$0.8 \times$ AVDD/5	$V_{RMS}$
Maximum Rated Output Power	$P_{OUT(max)}$	$R_L = 16\Omega$			40	mW
Load Impedance	$R_L$		16		47k	$\Omega$
Load Capacitance	$C_L$				1	nF
DC Offset		Measured between VOUT1L/R and AGND with path fully enabled but no signal playing	-1	0	+1	mV
<b>Analogue Output 2 (VOUT2L, VOUT2LN, VOUT2RP, VOUT2RN)</b>						
Differential Full Scale Output Signal Level	$V_{OUT}$	$R_L = 5\text{k}\Omega$ to $47\text{k}\Omega$			$2 \times$ AVDD/5	$V_{RMS}$
Single-ended Full Scale Output Signal Level	$V_{OUT}$	$R_L = 5\text{k}\Omega$ to $47\text{k}\Omega$			$1 \times$ AVDD/5	$V_{RMS}$
Load Impedance	$R_L$		5		47	k $\Omega$
Load Capacitance	$C_L$				1	nF

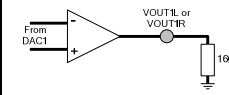
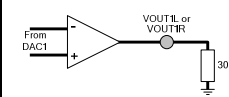
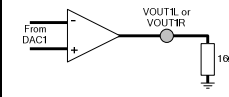
**Test Conditions**AVDD = CPVDD = 5V, DBVDD = 3.3V, DCVDD = 1.8V,  $T_A = +25^\circ\text{C}$ , 1kHz signal,  $f_s = 48\text{kHz}$ , 24-bit data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>DAC1 Path Performance (VOUT1L and VOUT1R into 10k<math>\Omega</math> Line Load)</b>						
Signal to Noise Ratio	SNR	Unweighted		105		dB
		A-weighted	100	108		dB
		A-weighted $f_s=96\text{kHz}$		108		dB
Out of Band Signal to Noise Ratio (0.6 $f_s$ to 150kHz)	OBSNR	$F_s > 11.025\text{kHz}$		80		dB
		$F_s \leq 11.025\text{kHz}$		75		dB
Dynamic Range	DNR	A-weighted -60dBFS		108		dB
Total Harmonic Distortion	THD	0dBFS		-96	-85	dB
		0dBFS $f_s=96\text{kHz}$		-96	-85	dB
Channel Separation		1kHz		115		dB
		20Hz to 20kHz		110		dB
Channel Level Matching		0dBFS		0.1		dB
Channel Phase Deviation				0.01		$^\circ$
AVDD Power Supply Rejection Ratio	AVDD PSRR	1kHz, 100mVpp on AVDD		51		dB
		20Hz to 20kHz, 100mVpp on AVDD		50		dB
CPVDD Power Supply Rejection Ratio	CPVDD PSRR	1kHz, 100mVpp on CPVDD		86		dB
		20Hz to 20kHz, 100mVpp on CPVDD		75		dB



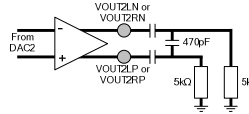
**Test Conditions**

AVDD = CPVDD = 5V, DBVDD = 3.3V, DCVDD = 1.8V, T<sub>A</sub> = +25°C, 1kHz signal, f<sub>s</sub> = 48kHz, 24-bit data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>DAC1 Path Performance (VOUT1L and VOUT1R into 16Ω Headphone Load)</b>						
Total Harmonic Distortion	THD	$P_{OUT} = 30mW$ $R_L = 16\Omega$ 		-80	-73	dB
				0.01		%
		$P_{OUT} = 10mW$ $R_L = 300\Omega$ 		-80		dB
				0.01		%
Idle Channel Noise		$R_L = 16\Omega$ A-weighted 	90	98		dBV
				12.26		$\mu V_{rms}$
Channel Separation		$R_L = 16\Omega$ 1kHz		85		dB
		$R_L = 16\Omega$ 20Hz to 20kHz		72		dB

**Test Conditions**AVDD = CPVDD = 5V, DBVDD = 3.3V, DCVDD = 1.8V,  $T_A = +25^\circ\text{C}$ , 1kHz signal,  $f_s = 48\text{kHz}$ , 24-bit data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>DAC2 Path Performance (VOUT2LP, VOUT2LN, VOUT2RP and VOUT2N into 10k<math>\Omega</math> Line Load)</b>						
Signal to Noise Ratio	SNR	Unweighted		103		dB
		A-weighted	100	106		dB
		A-weighted $f_s=96\text{kHz}$		106		dB
Out of Band Signal to Noise Ratio (0.6fs to 150kHz)	OBSNR	$F_s > 11.025\text{kHz}$		80		dB
		$F_s \leq 11.025\text{kHz}$		75		dB
Dynamic Range	DNR	A-weighted -60dBFS		106		dB
		0dBFS		-92		dB
		0dBFS $f_s=96\text{kHz}$		-92		dB
Channel Separation		20Hz to 20kHz		102		dB
Channel Level Matching		0dBFS		0.1		dB
Channel Phase Deviation				0.01		$^\circ$
AVDD Power Supply Rejection Ratio	AVDD PSRR	1kHz, 100mVpp on AVDD		75		dB
		20Hz to 20kHz, 100mVpp on AVDD	55			dB



**Test Conditions**AVDD = CPVDD = 5V, DBVDD = 3.3V, DCVDD = 1.8V, T<sub>A</sub> = +25°C, 1kHz signal, fs = 48kHz, 24-bit data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>S/PDIF Transmitter Specification</b>						
Output Signal Logic High	V <sub>OH(S/PDIF)</sub>		0.9 * DBVDD			V
Output Signal Logic Low	V <sub>OL(S/PDIF)</sub>				0.1 * DBVDD	V
Output Current Source/Sink Capability		DBVDD = 1.8V	7			mA
		DBVDD = 3.63V	15			mA
Output Sample Rate Tolerance		Includes maximum reference clock error of ±0.025% as allowed by HDA Specification			1000	ppm
			-0.1		+0.1	%
Output Sample Rate Support				32 44.1 48 88.2 96 176.4 192		kHz



**Test Conditions**AVDD = CPVDD = 5V, DBVDD = 3.3V, DCVDD = 1.8V, T<sub>A</sub> = +25°C, 1kHz signal, fs = 48kHz, 24-bit data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>Analogue References</b>						
Positive Voltage Reference	VREFP			0.9 * AVDD		V
Negative Voltage Reference	VREFN			0.1 * AVDD		V
Midrail Voltage Reference	VMID			0.5 * AVDD		V
Charge Pump Cap Level	CPCAP			3.15		V
Midrail Voltage Resistance	R <sub>VMID</sub>	AVDD to VMID or VMID to AGND VMID_SEL[1:0]=00		12.5		kΩ
		AVDD to VMID or VMID to AGND VMID_SEL[1:0]=01		75		kΩ
		AVDD to VMID or VMID to AGND VMID_SEL[1:0]=10		37.5		kΩ
		AVDD to VMID or VMID to AGND VMID_SEL[1:0]=11		375		kΩ
<b>Digital Input / Output</b>						
Input High Level	V <sub>IH</sub>		0.65 * DBVDD			V
Input Low Level	V <sub>IL</sub>				0.35 * DBVDD	V
Output High Level	V <sub>OH</sub>		0.9 * DBVDD			V
Output Low Level	V <sub>OL</sub>				0.1 * DBVDD	V
Input Capacitance					7.5	pF
Input Leakage			-0.1		+0.1	μA

## TERMINOLOGY

1. Signal-to-Noise Ratio (dB) – SNR is a measure of the difference in level between the full scale output signal and the output with no input signal applied.
2. Total Harmonic Distortion (dB) – THD is the level of the rms value of the sum of harmonic distortion products relative to the amplitude of the applied input signal.
3. Total Harmonic Distortion plus Noise (dB) – THD+N is the level of the rms value of the sum of harmonic distortion products plus noise in the specified bandwidth relative to the amplitude of the applied input signal.
4. Crosstalk (L/R) (dB) – left-to-right and right-to-left channel crosstalk is the measured signal level in the idle channel at the test signal frequency relative to the signal level at the output of the active channel. The active channel is configured and supplied with an appropriate input signal to drive a full scale output, with signal measured at the output of the associated idle channel. For example, measured signal level on the output of the idle right channel with a full scale signal level at the output of the active left channel.
5. Multi-Path Channel Separation (dB) – is the measured signal level in the idle path at the test signal frequency relative to the signal level at the output of the active path. The active path is configured and supplied with an appropriate input signal to drive a full scale output, with signal measured at the output of the specified idle path.
6. All performance measurements carried out with 20kHz low pass filter, and where noted an A-weighted filter. Failure to use such a filter will result in higher THD and lower SNR readings than are found in the Electrical Characteristics. The low pass filter removes out of band noise; although it is not audible it may affect dynamic specification values.
7. Mute Attenuation – This is a measure of the difference in level between the full scale output signal and the output with mute applied.
8. Channel Level Matching (dB) – the difference in output level between channels in a stereo pair.
9. Channel Phase Deviation (Degrees) – the difference in phase between channels in a stereo pair.
10. Idle Channel Noise (dBV) – absolute rms measurement of the noise floor over the 20Hz to 20kHz band.

## INTRODUCTION

The WM8860 is a high performance multi-channel audio CODEC designed for high performance portable PC audio systems. The device offers full compatibility with the Intel High Definition Audio (HDA) specification revision 1.0, allowing seamless integration with industry-standard HDA controllers.

The WM8860 has two high performance stereo DACs to enable four channels of high definition audio. A high-performance ground-referenced stereo headphone amplifier utilises advanced charge pump and DC servo technology to minimise system cost and space without compromise on audio quality. A stereo balanced line output is also provided. These line outputs may be used connected to external speaker drivers in a notebook or netbook application.

The WM8860 also has two high performance stereo ADCs to provide Hi-Fi quality analogue line-in and microphone input digitisation. A low noise microphone bias with programmable output voltage is provided, ideally suited as a bias current source for ECM microphones. Additionally, the CODEC contains a digital microphone interface capable of supporting up to four independent digital microphones, allowing high quality microphone array implementations to be realised. One differential stereo input is provided for line level signals, while one pseudo-differential stereo input with integrated microphone preamplifier is provided.

The WM8860 also contains a S/PDIF transmitter which is fully compatible with IEC-60958-3.

The WM8860 includes an integrated beep generator allowing system beeps to be played back through the output paths.

This datasheet assumes familiarity with the High Definition Audio Specification Revision 1.0, available from <http://www.intel.com/standards/hdaudio/>. For those verbs implemented in the WM8860 which are as defined in the High Definition Audio Specification Revision 1.0 there is no detailed text describing their use in this datasheet. However, detailed text describing the function of of vendor-specific verbs is provided. Additionally, a full list of each node and each verb implemented in the WM8860 is provided at the rear of the document.

APPLICATIONS INFORMATION

RECOMMENDED EXTERNAL COMPONENTS

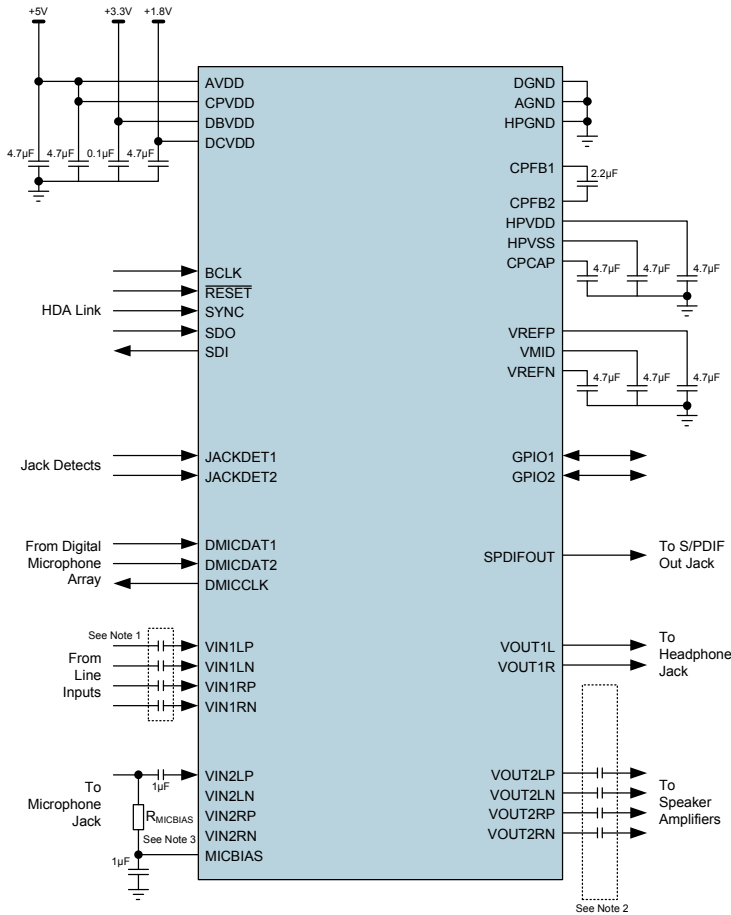
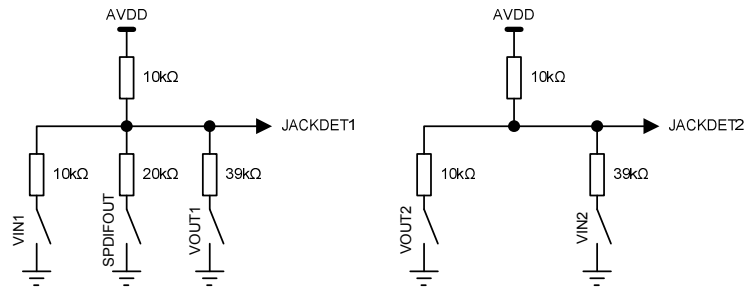


Figure 1 Recommended External Components

Notes:

1. AC-coupling capacitors for inputs may depend on circuitry used prior to WM8860. Typical values between 1µF and 10µF are common – consult any documentation for the exact circuit used
2. AC-coupling capacitors for outputs may depend in circuitry used after WM8860. Typical values between 1µF and 10µF are common – consult any documentation for the exact circuit used
3. A single-ended mono microphone input is shown, but other configurations are equally valid. The value of the microphone bias resistor will vary with the microphone used – a typical value is 2.2kΩ
4. The capacitor between CFB1 and CFB2 must be placed as close as possible to the device pins
5. The decoupling capacitor on CPCAP must also be placed as close as possible to the device pins
6. The decoupling capacitor on CPVDD is next important – it too should be placed as close as possible to the device pins
7. The decoupling capacitors on VREFP, VREFN and VMID are next important, in that order
8. All remaining decoupling capacitors should then be placed as close as possible

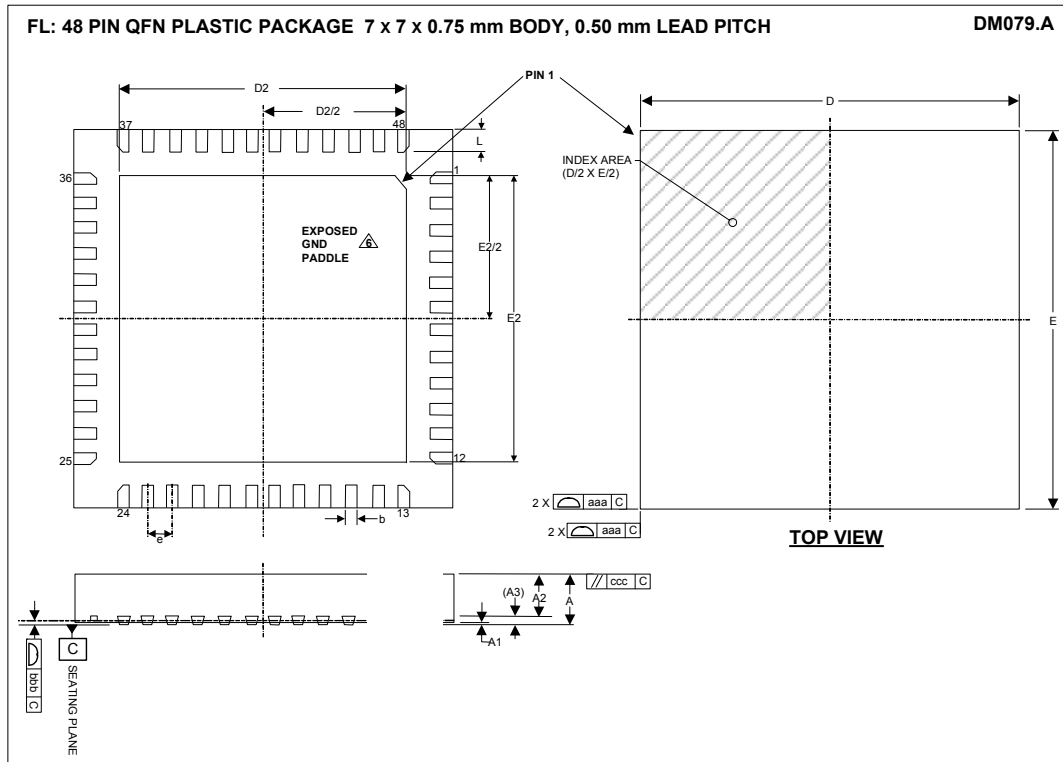
## REQUIRED JACK DETECT COMPONENTS



**Figure 2** Required Jack Detect Components

The WM8860 supports jack detect on all analogue input and output ports, as well as on the S/PDIF output. This is implemented as per the High Definition Audio Specification Revision 1.0, section 7.4.2 and as such requires the resistor values shown in Figure 2 above. Note that, as per the High Definition Audio Specification, it is a requirement that the tolerance on these resistors is 1% or better.

**PACKAGE DIMENSIONS**



Symbols	Dimensions (mm)			
	MIN	NOM	MAX	NOTE
<b>A</b>	0.7	0.75	0.8	
<b>A1</b>	0	0.035	0.05	
<b>A2</b>	-	0.55	0.57	
<b>A3</b>		0.203 REF		
<b>b</b>	0.20	0.25	0.30	1
<b>D</b>		7.00 BSC		
<b>D2</b>	5.55	5.65	5.75	
<b>E</b>		7.00 BSC		
<b>E2</b>	5.55	5.65	5.75	
<b>e</b>		0.5 BSC		
<b>L</b>	0.35	0.4	0.45	
<b>Tolerances of Form and Position</b>				
<b>aaa</b>	0.10			
<b>bbb</b>	0.08			
<b>ccc</b>	0.10			
<b>REF</b>	JEDEC, MO-220			

- NOTES:
1. DIMENSION  $b$  APPLIED TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 mm AND 0.30 mm FROM TERMINAL TIP.
  2. ALL DIMENSIONS ARE IN MILLIMETRES
  3. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-002.
  4. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
  5. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
  6. REFER TO APPLICATIONS NOTE WAN\_0118 FOR FURTHER INFORMATION.

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