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WM8803

Digital Audio Interface Receiver

DESCRIPTION

The WM8803 is a digital audio interface receiver conforming to IEC 60958/61937 and EIAJ CP-1201. It supports input audio data rates up to 192kHz and a maximum output data length of 24 bits.

The WM8803 has a flexible digital output port that allows the user access to channel status pre-emphasis information, input signal sampling frequency, sub-code Q data with the associated CRC flags and other status data.

The WM8803 can output an externally input clock signal that can be used as an ADC converter clock when the PLL is unlocked. It also maintains the continuity of the output clock when the clock is switched.

The WM8803 includes a built-in oscillator and serial data input circuits and allows the system micro-controller to read the sub-code Q data and the channel status. It provides several low-power modes, thus supporting applications that require long battery life, such as portable audio devices and PDAs.

The device is available in a 24-pin TSSOP package.

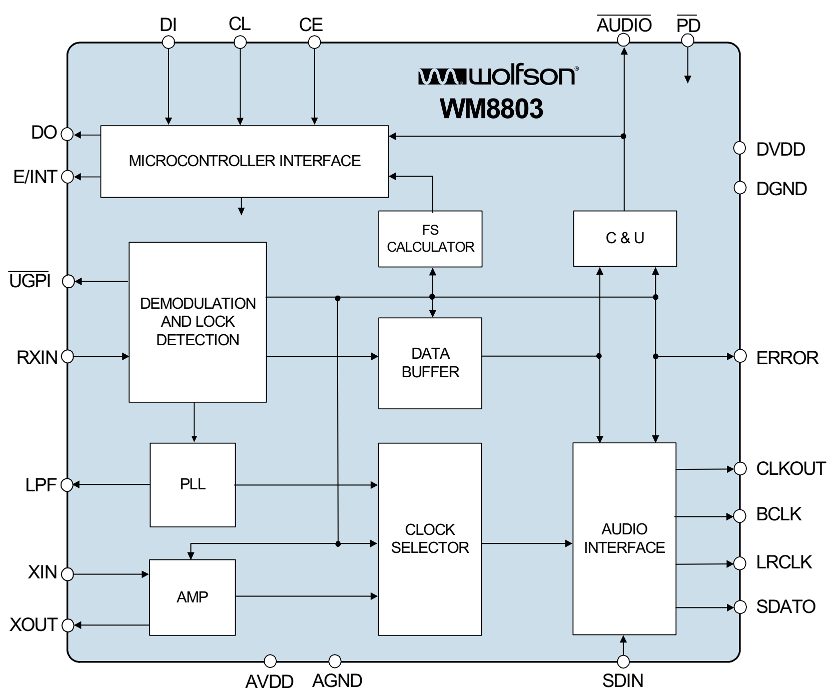
FEATURES

- PLL circuit for synchronization with transferred input bi-phase mark signal.
- Input sampling frequency: 32kHz to 192kHz
- Outputs clocks: fs, 64fs, and one of 128fs, 256fs, 384fs, and 512fs.
- 4-Wire CCB MPU Serial Control or Hardware Default Interface
- Master Clocking Mode
- Programmable Audio Data Interface Modes
  - I^2S, Left, Right Justified
  - 16/20/24/32 bit Word Lengths
- 3.3V Digital supply Operation
- 5V tolerant digital input ports

APPLICATIONS

- DVD Receivers
- DVD-R/W Players
- Audio Video Receivers
- Portable Music Players

BLOCK DIAGRAM



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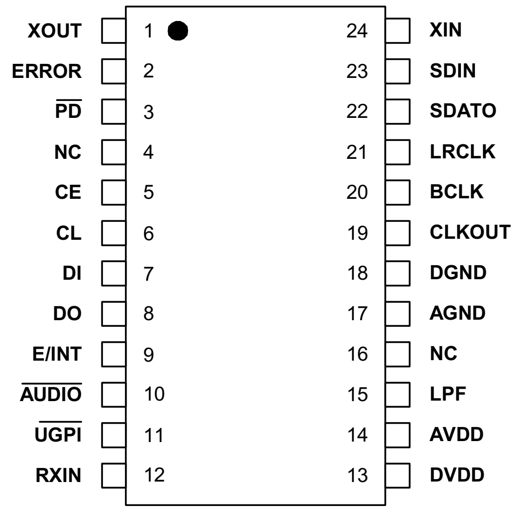
PIN CONFIGURATION



ORDERING INFORMATION

DEVICE	TEMP. RANGE	PACKAGE
WM8803SCDT/V	-30 to +70^{o}C	24-pin TSSOP

PIN DESCRIPTION

PIN	NAME	TYPE	DESCRIPTION
1	XOUT	Analogue Output	Oscillation amplifier circuit output pin
2	ERROR	Digital Output	PLL lock error and data error output pin
3	$\overline{\text{PD}}$ [5]	Digital Input	System reset and low power mode control input pin (5V tolerant)
4	NC	Digital Input	Non connection
5	CE[5]	Digital Input	Micro-controller interface: chip enable input pin (5V tolerant)
6	CL[5]	Digital Input	Micro-controller interface: serial clock input pin (5V tolerant)
7	DI[5]	Digital Input	Micro-controller interface: write data input pin (5V tolerant)
8	DO	Digital Output	Micro-controller interface: read data output pin
9	E / INT	Digital Output	Pre-emphasis detection or micro-controller interface interrupt output pin
10	$\overline{\text{AUDIO}}$	Digital Output	Channel status bit 1 non-PCM data detection output pin
11	$\overline{\text{UGPI}}$	Digital Output	User general purpose interface output pin[1]
12	RXIN[5]	Digital Input	Digital data input pin (5V tolerant)
13	DVDD	Supply	Digital system power supply
14	AVDD	Supply	Analog system power supply
15	LPF	Analogue Output	PLL loop filter connection pin
16	NC		No connection
17	AGND	Supply	Analog system ground
18	DGND	Supply	Digital system ground
19	CLKOUT	Digital Output	System clock output pin[2]
20	BCLK	Digital Output	64fs clock output pin
21	LRCLK	Digital Output	Fs clock output pin[3]
22	SDATO	Digital Output	Demodulated data output pin
23	SDIN	Digital Input	Serial digital data input pin (5V tolerant)
24	XIN	Digital Input	Oscillation amplifier element connection or external clock input pin

Notes:

1. Micro-controller register output or clock switching transition period signal.
2. 128fs, 256fs, 384fs, 512fs, or oscillator amplifier outputs
3. Other than I^2S mode; Low: right channel, High: left channel
   I^2S mode; Low: left channel, High: right channel
4. I/O voltage handling: I or O pins: –0.3 to +3.6V, except annotated pins: –0.3 to +5.5V
5. To prevent logic circuit latch-up, all power supply levels must be applied or removed simultaneously.

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Ele Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically suscept damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage device.

CONDITION	SYMBOL	CONDITIONS	MIN - MAX
Maximum supply voltage	$AVDD_{max}$	1	–0.3 to 4.6V
Maximum supply voltage	$DVDD_{max}$	2	–0.3 to 4.6V
Input voltage 1	V_{IN1}	3	–0.3 to VDD + 0.3V
Input voltage 2	V_{IN2}	4	–0.3 to 5.8V
Storage temperature	T_{stg}		–55 to 125°C
Operating temperature	T_{opg}		–30 to 70°C
Maximum output current	I_i, I_o	5	±20 mA

Notes:

1. AVDD pin
2. DVDD pin
3. XIN pin
4. RXIN, SDIN, PD, CE, CL, and DI pins
5. Per single input or output pin

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply voltage 1	AVDD, DVDD	1	2.7	3.3	3.6	V
Supply voltage 2	AVDD, DVDD	2	3.0	3.3	3.6	V
Input voltage range 1	V_{IN1}	3	0	3.3	3.6	V
Input voltage range 2	V_{IN2}	4	0	3.3	5.5	V
Operating temperature	T_{opg}		–30	—	70	°C

Notes:

1. PLLCK [1:0] = “00” or PLLCK [1:0] = “01”
2. PLLCK [1:0] = “10” or PLLCK [1:0] = “11”
3. XIN pin
4. RXIN, SDIN, $\overline{PD}$, CE, CL, and DI pins

ELECTRICAL CHARACTERISTICS

INPUT AND OUTPUT PIN CAPACITANCE

Test Conditions

AVDD = DVDD = V_{IN1} = V_{IN2} = 0 V, Ta = 25°C, f = 1MHz

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input and Output Pin Capacitance						
Input pins	C_{IN}	1	—	—	10	pF
Output pins	C_{OUT}	1	—	—	10	pF

Notes:

1. AVDD = DVDD = V_{IN1} = V_{IN2} = 0 V, Ta = 25°C, f = 1MHz

DC CHARACTERISTICS

Test Conditions

Ta = 25°C, AVDD = DVDD = 3.3V, AGND = DGND = 0V

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC Characteristics						
High-level input voltage	V_{IH}	1	0.7DVDD	—	—	V
Low-level input voltage	V_{IL}	1	—	—	0.2DVDD	V
High-level input voltage	V_{IH}	2	2.0	—	5.8	V
Low-level input voltage	V_{IL}	2	–0.3	—	0.8	V
High-level output voltage	V_{OH}	3	DVDD – 0.8	—	—	V
Low-level output voltage	V_{OL}	3	—	—	0.4	V
High-level output voltage	V_{OH}	4	DVDD – 0.8	—	—	V
Low-level output voltage	V_{OL}	4	—	—	0.4	V
High-level output voltage	V_{OH}	5	DVDD – 0.8	—	—	V
Low-level output voltage	V_{OL}	5	—	—	0.4	V
Current drain	I_{DD1}	6	—	6.5	13	mA
Current drain	I_{DD2}	7	—	—	0.1	μA
Current drain	I_{DD3}	8	—	4.5	9	mA
Current drain	I_{DD4}	9	—	5	10	mA

Notes:

1. CMOS level pins: XIN pin
2. TTL level pins: Input pins other than those listed above.
3. I_{OH} = –8mA, I_{OL} = 6mA: CLKOUT pin
4. I_{OH} = –2mA, I_{OL} = 2mA: BCLK, LRCLK, SDATO, and DO pins
5. I_{OH} = –1mA, I_{OL} = 1mA: Output pins other than those listed above.
6. Operating mode: *PLLSEL* = “0”, *AMPOPR* = “0”, f_S = 44.1kHz, C_L = 30pF
7. Low power mode condition 1) : $\overline{PD}$ = low
8. Low power mode condition 2) *PDOWN [1:0]* = “01”, XIN = 11.2896MHz, C_L = 30pF
9. Low power mode condition 3) : *PDOWN [1:0]* = “10”, XIN = 11.2896MHz, C_L = 30pF

SYSTEM TIMING REQUIREMENTS

Test Conditions

Ta = 25°C, AVDD = DVDD = 3.3V, AGND = DGND = 0V

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
System Timing Information						
RXIN sampling frequency	f_{FS1}	1	30	—	195	kHz
RXIN sampling frequency	f_{FS2}	2	30	—	108	kHz
XIN clock frequency	f_{XF1}	3	—	11.2896	—	MHz
XIN clock frequency	f_{XF2}	4	—	12.2880	—	MHz
XIN clock frequency	f_{XF3}	5	—	16.9344	—	MHz
XIN clock frequency	f_{XF4}	6	—	22.5792	—	MHz
XIN clock frequency	f_{XF5}	7	—	24.5760	—	MHz
XIN clock frequency	f_{XF6}	8	—	33.8688	—	MHz
CLKOUT clock frequency	F_{MCK}		2	—	100	MHz
CLKOUT clock jitter	t_j		—	200	—	ps

Notes:

1. *PLLCK [1:0]* = “00”
2. Settings other than *PLLCK [1:0]* = “00”.
3. *XISEL [3:0]* = “0000”
4. *XISEL [3:0]* = “0001”
5. *XISEL [3:0]* = “0010”
6. *XISEL [3:0]* = “0100”
7. *XISEL [3:0]* = “0101”
8. *XISEL [3:0]* = “0110”

SERIAL INTERFACE TIMING REQUIREMENTS

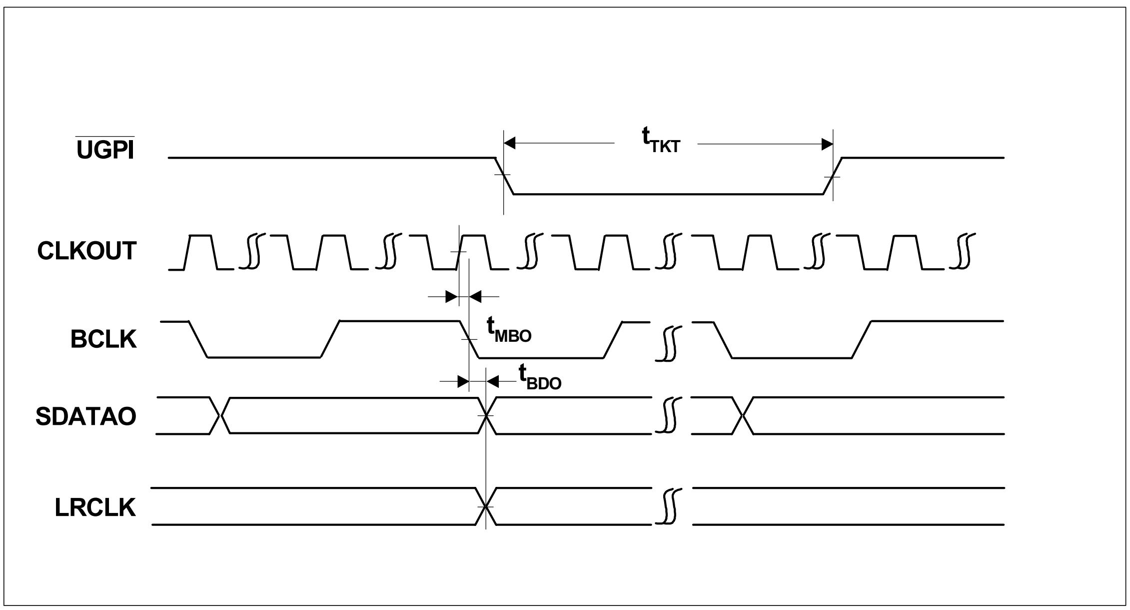


Figure 1 Serial Interface Timing Requirements

Test Conditions

Ta = 25°C, AVDD = DVDD = 3.3V, AGND = DGND = 0V

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
CLKOUT to BCLK delay	t_{MBO}		—	—	10	ns
BCLK to SDATO delay	t_{BDO}		—	—	5	ns
UGPI low-level pulse width	t_{TKT}	1	—	—	100	ms

Notes:

1. When setting the clock switching transition period signal output

MICRO-CONTROLLER INTERFACE TIMING REQUIREMENTS

Test Conditions

Ta = -30~70°C, AVDD = DVDD = 3.3V, AGND = DGND = 0V

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Micro-controller Interface Timing Information						
$\overline{PD}$ low-level pulse width	T_{PDdw}		200	—	—	μs
E/INT high-level pulse width	T_{INTuw}	1	5	1/fs	63	μs
CL low-level pulse width	T_{CLdw}		100	—	—	ns
CL high-level pulse width	T_{CLuw}		100	—	—	ns
CL to CE setup time	$t_{CEsetup}$		50	—	—	ns
CL to CE hold time	T_{CEhold}		50	—	—	ns
CL to DI setup time	$T_{DIsetup}$		50	—	—	ns
CL to DI hold time	T_{DIhold}		50	—	—	ns
CL to CE hold time	T_{CLhold}		50	—	—	ns
CL to DO delay time	t_{CLtoDO}		—	—	20	ns
CE to DO delay time	t_{CEtoDO}		—	—	20	ns

Notes:

1. *INTOPF* = “1”, *INTSEL* = “1”, and *fs* is the input sampling frequency.

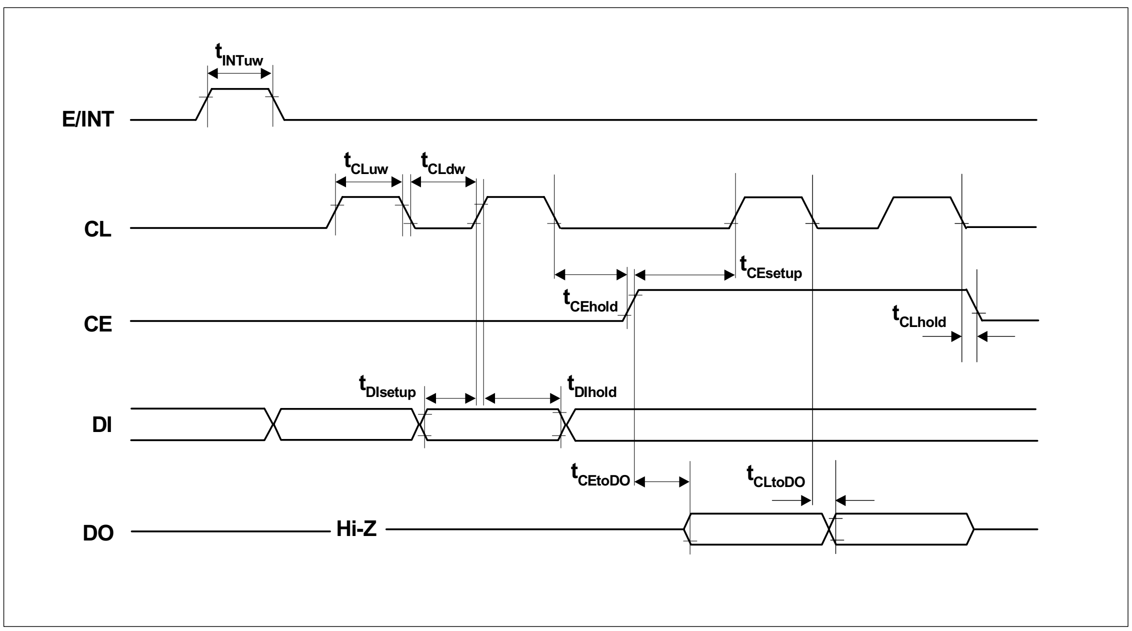


Figure 2 Micro-controller Interface Timing Requirements

DEVICE DESCRIPTION

SYSTEM RESET (PD)

The system operates normally when PD is set to high level after applying a supply voltage of 2.7V(3.0V) or higher. Following power ON, the system is reset by setting PD to low level again. System reset is enabled by setting PDB at power on.

If a crystal oscillator is used, after setting PD low level and then high level, at least 10ms should be allowed before starting normal operation until the oscillator element is stable.

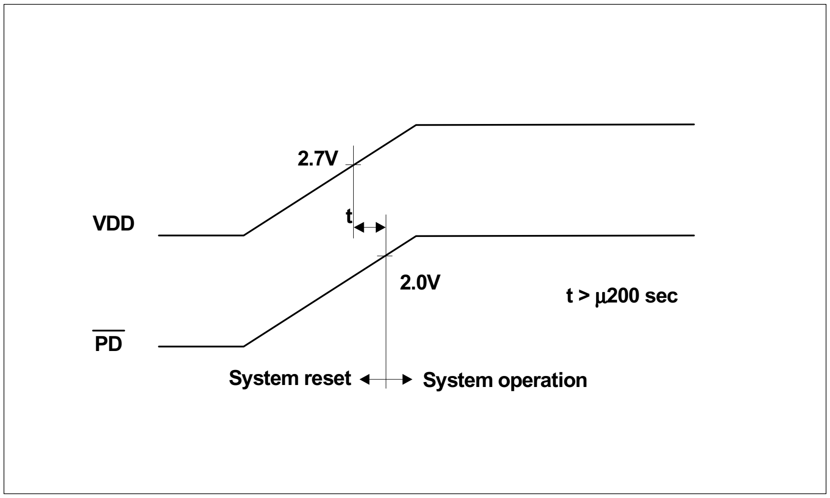


Figure 3 PD Pin Levels at Power On

LOW POWER MODES

The WM8803 not only supports a total system power down mode controlled with the PD pin but also provides low-power modes in which only certain functions operate. These low power modes are controlled by *PDOWN[1:0]*.

The "power down" mode controlled by the PD pin applies to all circuits in the WM8803. All clocks are stopped and the registers are initialized.

The XIN and XOUT pins continue to operate in the *PDOWN[1:0]* controlled low power mode, which stops all circuits other than the oscillator amplifier. The XOUT signal can be used as the master clock for a DSP or other circuits.

The CLKOUT, BCLK, LRCLK, SDATO, SDIN, XIN and XOUT pins continue to operate in the *PDOWN[1:0]* controlled low power mode, which stops all circuits other than the oscillator amplifier and the divider circuit . This mode can be used to minimize power consumption during analogue data reception.

In a low power mode set with the *PDOWN[1:0]* and with the oscillator amplifier stopped by setting *AMPOPR*, it will not be possible for the WM8803 to provide a clock output. The *AMPOPR* overrides all other oscillator settings. Note that the *PLLOPR* setting is invalid and the PLL circuit will be stopped.

When a low power mode is set up with the *PDOWN[1:0]*, it is possible to write to the micro-controller registers. However, all the sub-code Q and channel status data will read out as zeros.

The low power modes are listed in Table 1.

MODE	PDB	*AMPOPR*	*PLLOPR*	*PDOWN1*	*PDOWN0*	FUNCTION
(1)	L	×	×	×	×	Reset (stand-by)
(2)	H	0	0	0	0	Normal operation
(3)		0	1	0	0	VCO stopped.
(4)		0	×	0	1	All circuits except the oscillator amplifier stopped.
(5)		0	×	1	0	All circuits except the oscillator amplifier and divider circuit stopped.
(6)		1	0	0	0	Oscillator amplifier stopped.
(7)		1	1	×	×	All circuits stopped.

Table 1 Low Power Modes

The table below lists the output pin states in the above modes.

OUTPUT PIN	MODE (1)	MODE (2)	MODE (3)	MODE (4)	MODE (5)	MODE (6)	MODE (7)
AUDIOB	L	Output	L	L	L	Output	L
UGPIB	H	Output	Output	Output	Output	Output	Output
CLKOUT	L	Output	Output	Output	Output	Output	L
BCLK	L	Output	Output	L	Output	Output	L or H
LRCLK	L	Output	Output	L	Output	Output	L or H
SDATO	L	Output	Output	L	Output	Output	L
XOUT	H	Output	Output	Output	Output	H	H
ERROR	H	Output	H	H	H	Output	H
E/INT	L	Output	L	L	L	Output	L

Table 2 Output Pin States in Modes (1) to (7)

Notes:

1. In modes (3), (4), and (5), the clock supplied to XIN is used as the source.
2. Mode (3) applies in the state where an external clock other than CLKOUT is supplied to XIN. If XIN and CLKOUT are connected, no clock signals are output in this mode.
3. Mode (6) applies when the PLL circuit is locked. When the PLL circuit is unlocked, all circuits will go to the stopped state since no clock signal is supplied to XIN.
4. In mode (7), the states immediately prior to entering mode (7) will be retained.

CLOCKS

PLL (LPF)

The WM8803 includes a VCO (voltage controlled oscillator) that can synchronize with data corresponding to sampling frequencies from 30k to 195kHz.

The locking frequency is selected by setting *PLLCK[1:0]*.

The VCO circuit can be stopped by setting *PLLOPR*.

The range of input data that can be received depends upon the settings of the *PLLCK[1:0]*.

The (512/2)fs entry for the *PLLCK[1:0]* = "11" in Table 3 is a state where the PLL itself is synchronized with the 512fs clock, but the clock signal output from CLKOUT is a frequency 1/2 that of the PLL locked frequency i.e.256fs. This (512/2)fs lock frequency has the same functions as the 256fs setting from CLKOUT and can be convenient for certain applications. Refer to the output clocks section for details.

It is recommended that the 256fs setting of *PLLCK[1:0]* = "00" is used to reduce the system power consumption, especially in portable equipment.

For best performance, it is recommended that the 512fs setting of *PLLCK[1:0]* = "10" or the (512/2)fs of *PLLCK[1:0]* = "11" is used.

PLLCK1	PLLCK0	PLL LOCK FREQUENCY	INPUT DATA RECEPTION RANGE
0	0	256fs	30k to 195kHz
0	1	384fs	30k to 108kHz
1	0	512fs	30k to 108kHz
1	1	(512/2)fs	30k to 108kHz

Table 3 Input Data Reception Ranges by PLL Lock Frequency Setting

The LPF is the PLL loop filter connection. Use capacitor and resistor components of the recommended values as listed in the table below according to the *PLLCK[1:0]* settings used.

PLLCK1	PLLCK0	R0	C0	C1
0	0	150Ω	0.047µF	0.0068µF
0	1			
1	0	150Ω	0.068µF	0.0047µF
1	1			

Table 4 Loop Filter Component Values

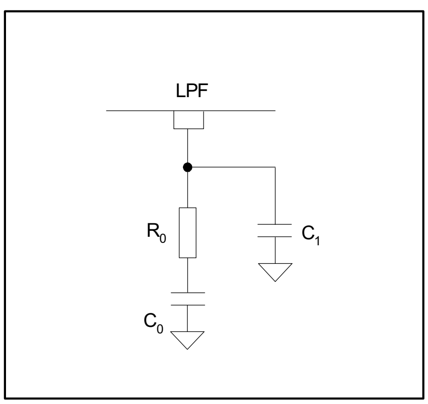


Figure 4 Loop Filter Structure

OSCILLATOR AMPLIFIER (XIN AND XOUT)

The following methods can be used to supply a clock signal to the internal oscillator amplifier.

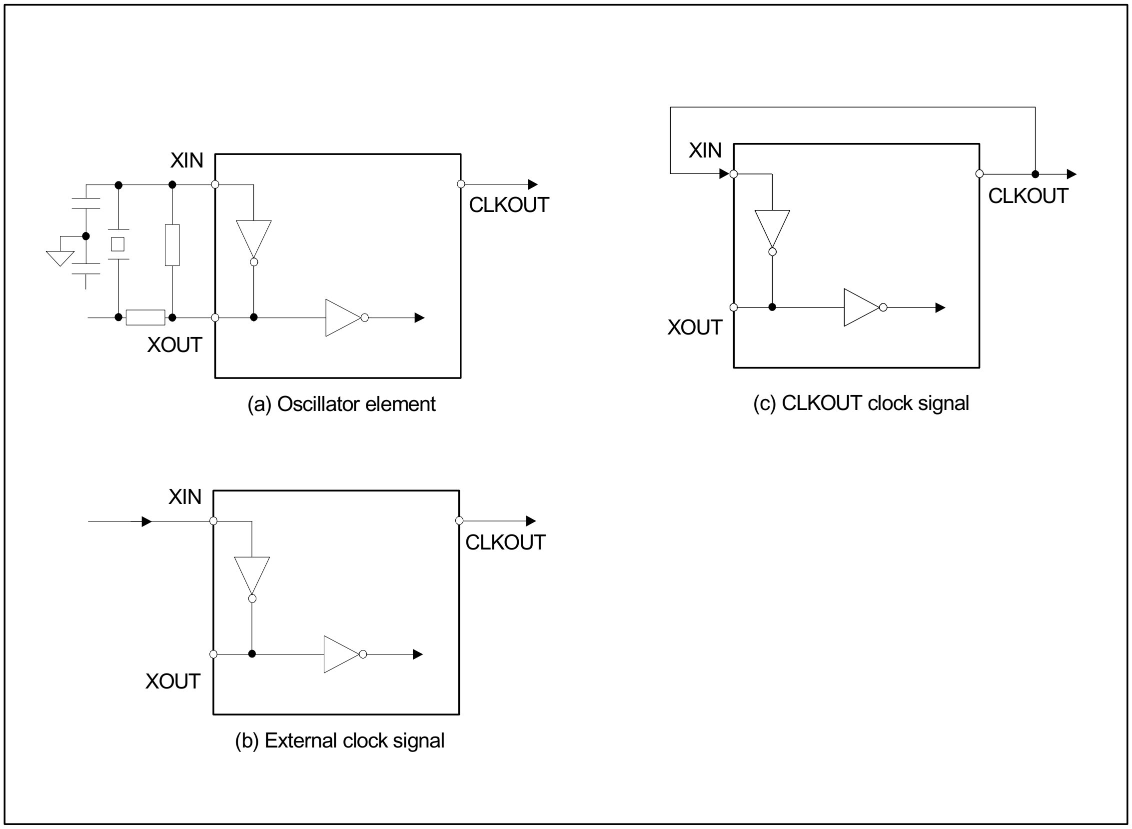


Figure 5 XIN and XOUT Circuit Structures

If an oscillator element is used, it is recommended that it provides the desired system operating frequency as its fundamental frequency. Since the load capacitance depends on the oscillator element characteristics, the circuit must be designed for the crystal used.

In normal operation, the clock signal to the XIN pin should be supplied at all times.

An externally supplied clock is used when the PLL circuit is unlocked and when XIN is the clock source. A clock source input to XIN is also required when calculating the input data sampling frequency.

A clock of frequency 11.2896, 12.288, 16.9344, 22.5792, 24.576, or 33.8688MHz that matches the setting of the *XISEL[2:0]* should be applied. Digital data should only be input after the *XISEL[2:0]* has been set to match the oscillator or external clock input frequency. The WM8803 may malfunction if data is input when the input frequency and *XISEL[2:0]* frequency do not match.

The WM8803 will operate even when the frequency set with the *XISEL[2:0]* and the frequency supplied to XIN differ. However, maintenance of continuity of clock switching and the input fs calculation are not guaranteed.

The WM8803 supports an application in which CLKOUT is connected to XIN and *XISEL3* is set, thus requiring no oscillator element. However, since only the VCO is used as the source clock, when the PLL is not in the locked state the VCO free-running frequency (10M to 16MHz) will be output from CLKOUT. Furthermore, input fs calculation and limitation are not possible with this technique. Additionally, since no clock is supplied to the oscillator amplifier circuit when the VCO is set to the stopped state, the whole system will go to the stopped state. This function limits settings to *PLLCK[1:0]* = “00”.

The oscillator amplifier normally stops automatically when the PLL is locked, but continuous operation can be set by *AMPCNT*. Setting the WM8803 to continuous operation mode makes it possible to calculate the input sampling frequency when the PLL is locked. However, since both the oscillator amplifier clock and the PLL clock signals will be present, users must determined whether or not this adversely affects audio quality.

The oscillator amplifier can be stopped when not required by setting the *AMPOPR*. When returning from stopped mode to operating mode the application must maintain its state for at least 10ms until the oscillator stabilizes and normal operation resumes.

OUTPUT CLOCKS (CLKOUT, BCLK, LRCLK)

The clock source for the clock outputs CLKOUT, BCLK, and LRCLK can be selected from two master clocks: the PLL circuit and the XIN pin.

Normally, when the PLL circuit is locked master clock is switched to the PLL source. When the PLL circuit is unlocked, master clock automatically switches to the XIN source. The clock source can be forcibly selected by setting *OCKSEL*. Clock continuity is maintained when the clock source is switched due to the locked/unlocked state of the PLL circuit or by setting *OCKSEL*.

Clock switching depends on the PLL circuit locked/unlocked state at the time OCKSEL is set. If the PLL source is selected by *OCKSEL* when the PLL circuit is unlocked, the switch will occur automatically after the PLL circuit locks.

When VCO operation is stopped by setting *PLLOPR*, XIN becomes the clock source. However, clock continuity cannot be maintained if the stopped state is set with the *PLLOPR* while the PLL circuit is locked. Continuity cannot be maintained when switching from the PLL locked state with low power mode set.

OCKSEL	**0**		**1**	
PLL state	Locked	Unlocked	Locked	Unlocked
Clock source	PLL	XIN	XIN	XIN

Table 5 Command Settings, PLL States, and the Clock Source

Either the PLL clock or the XIN clock is output from CLKOUT. The CLKOUT clock signal is divided to create the signals output from BCLK and LRCLK.

The frequency when the PLL circuit is locked is set with the *PLLCK[1:0]*. When switching from the 512fs setting, (*PLLCK[1:0]* = “10”) to the (512/2)fs setting (*PLLCK[1:0]* = “11”) in the PLL locked state, it is possible to maintain clock continuity without losing the PLL lock. This is also true when changing the frequency is the opposite direction..

Using the procedure shown in Figure 6 to switch between 512fs and (512/2)fs, the BCLK and LRCLK output clock will maintain continuity and allow the CLKOUT output clock frequency to be held within a narrow band.

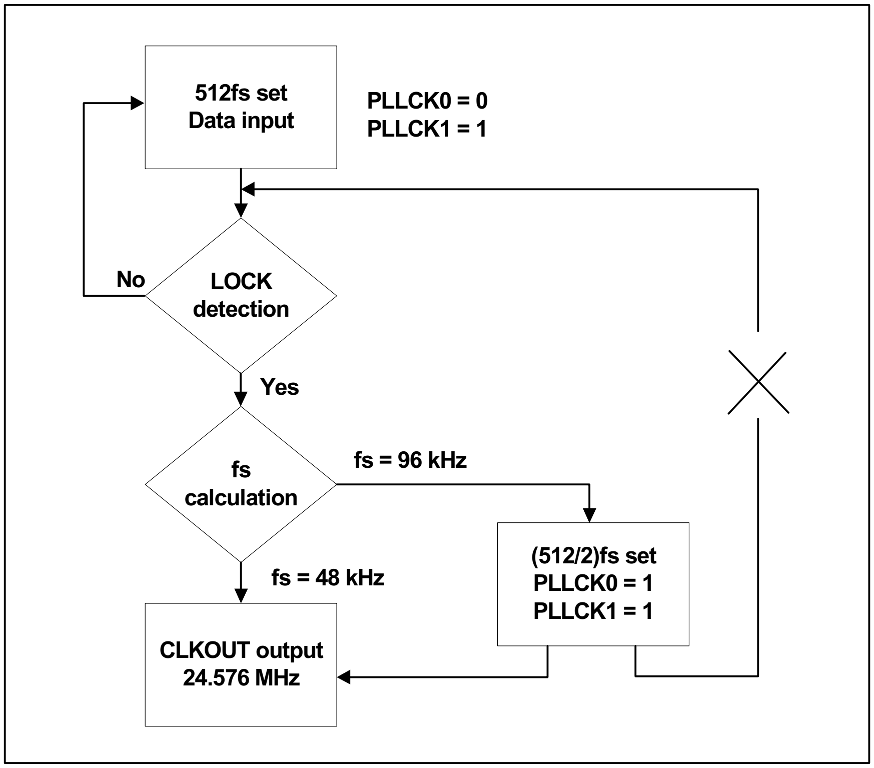


Figure 6 Flowchart for CLKOUT Output Clock Narrow Band Operation

The tables below show the output clocks in XIN and PLL clock source modes.

PLLCK1	PLLCK0	XISEL1	XISEL0	CLKOUT	BCLK	LRCLK
0	0	0	0	11.2896MHz	2.8224MHz	44.1kHz
0	0	0	1	12.2880MHz	3.0720MHz	48kHz
0	0	1	0	16.9344MHz	4.2336MHz	66.15kHz
0	1	0	0	11.2896MHz	1.8816MHz	29.4kHz
0	1	0	1	12.2880MHz	2.0480MHz	32kHz
0	1	1	0	16.9344MHz	2.8224MHz	44.1kHz
1	0	0	0	11.2896MHz	2.8224MHz	44.1kHz
1	0	0	1	12.2880MHz	3.0720MHz	48kHz
1	0	1	0	16.9344MHz	4.2336MHz	66.15kHz
1	1	0	0	11.2896MHz	2.8224MHz	44.1kHz
1	1	0	1	12.2880MHz	3.0720MHz	48kHz
1	1	1	0	16.9344MHz	4.2336MHz	66.15kHz

Table 6 XIN Clock Source Mode Output Clocks

Note:

1. *XISEL2* = 0, PLL unlocked state or forced setting

PLLCK1	PLLCK0	XISEL1	XISEL0	CLKOUT	BCLK	LRCLK
0	0	0	0	22.5792MHz	5.6448MHz	88.2kHz
0	0	0	1	24.5760MHz	6.1440MHz	96kHz
0	0	1	0	33.8688MHz	8.4672MHz	132.3kHz
0	1	0	0	22.5792MHz	3.7632MHz	58.8kHz
0	1	0	1	24.5760MHz	4.0960MHz	64kHz
0	1	1	0	33.8688MHz	5.6448MHz	88.2kHz
1	0	0	0	22.5792MHz	5.6448MHz	88.2kHz
1	0	0	1	24.5760MHz	6.1440MHz	96kHz
1	0	1	0	33.8688MHz	8.4672MHz	132.3kHz
1	1	0	0	22.5792MHz	5.6448MHz	88.2kHz
1	1	0	1	24.5760MHz	6.1440MHz	96kHz
1	1	1	0	33.8688MHz	8.4672MHz	132.3kHz

Table 7 XIN Clock Source Mode Output Clocks

Note:

1. *XISEL2* = 1, PLL unlocked state or forced setting

PLLCK1	PLLCK0	CLKOUT	BCLK	LRCLK
0	0	256 s	64fs	Fs
0	1	384fs	64fs	Fs
1	0	512fs	64fs	Fs
1	1	256fs	64fs	Fs

Table 8 PLL Clock Source Mode Output Clocks (PLL Locked State)

The CLKOUT output clock frequency can be set to 1/2 its normal value by *MCKHFO*, regardless of the PLL locked/unlocked state. Clock switching using *MCKHFO* can also be performed in the PLL locked state without losing that locked state, but clock continuity is not maintained.

If the audio output format is set to bi-phase data output, the BCLK output clock frequency will be doubled to 128fs when the PLL circuit is locked. However, when unlocked, the BCLK frequencies from Table 8 will be output. Note that the clock continuity is not maintained when this output format is set.

CLOCK SYSTEM DIAGRAM

This section presents the relationship between the two master clock types and the switching and clock dividing functions.

The items in square brackets near the switch and function blocks are the names of write commands.

The Lock/Unlock switch is switched automatically according to the locked/unlocked state of the PLL circuit.

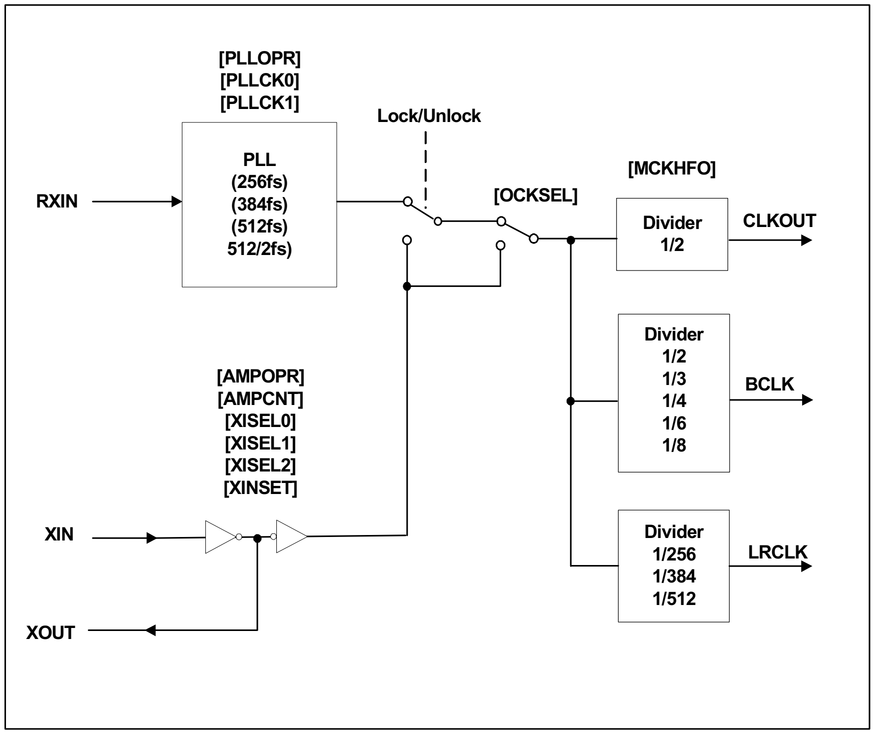


Figure 7 Master Clock System Diagram

NOTES ON CLOCK SOURCE SWITCHING

In states where the input fs calculation result is restricted by *FLIMIT*, if the WM8803 is switched by *OCKSEL* from the PLL locked state (oscillator amplifier stopped) to the XIN source clock state, clock continuity is maintained. However, ERROR will temporarily output a high level indicating an error. This is because the oscillator amplifier will switch to the operating state at the same time as the WM8803 switches to XIN source operation, and the input fs calculation will be restarted. The fs calculated value prior to this time will be reset and when that is compared to the newly calculated fs value, the transition will be handled as a change in fs.

With these settings, the oscillator amplifier must be set to continuous operation mode by *AMPCNT* so that the clock source can be switched by *OCKSEL* while maintaining the ERROR state.

Note that when switching from the oscillator amplifier stopped state to XIN (the clock source while the PLL circuit is locked), clocks which use XIN as the source will be output only after the oscillator amplifier has started operating. Inversely, switching from XIN to the PLL circuit in the locked state allows clocks to be output immediately. In both cases, clock continuity is maintained.

When neither an oscillator element nor an external clock is used, but the CLKOUT clock is supplied to XIN. The VCO free-running frequency is output from CLKOUT; when the PLL is unlocked this frequency will be in the range 10 to 16MHz. Clock signals created by dividing CLKOUT are output from BCLK and LRCLK. However, these BCLK and LRCLK clocks will differ with the WM8803 sample rate set and will vary with the supply voltage and operating environment. **Care is required when using the CLKOUT, BCLK, and LRCLK clocks when the PLL circuit is unlocked**.

DATA INPUT AND OUTPUT

BI-PHASE MARK MODULATED DIGITAL DATA INPUT (RXIN)

The bi-phase mark modulated digital data is input through the RXIN pin.

The RXIN pin supports TTL levels. This allows a 5V optical reception module to be connected directly.

BI-PHASE MARK MODULATED INPUT DATA RECEPTION RANGE SETTING

The WM8803 can restrict the upper limit of the input data sampling frequency received and only receive input data at selected sampling frequencies.

The input frequency is set by selecting *FLIMIT* = 1 and selecting the required sampling rate with *FSSEL[3:0],* Table 9.

FSSEL3	FSSEL2	FSSEL1	FSSEL0	INPUT DATA RECEPTION RANGE
0	0	0	0	32kHz to 96kHz
0	0	0	1	32kHz only
0	0	1	0	44.1kHz only
0	0	1	1	48kHz only
0	1	0	0	88.2kHz only
0	1	0	1	96kHz only
0	1	1	0	44.1kHz or 88.2kHz only
0	1	1	1	48kHz or 96kHz only
1	0	0	0	32kHz or 44.1kHz or 48kHz
1 …. 1	0 ….. 1	0 ….. 1	1 ….. 1	Reserved

Table 9 Input Data Reception Range (*FS4XIN* = 0)

Note:

The notation 32kHz to 96kHz means 32k, 44.1k, 48k, 64k, 88.2k, or 96kHz.

The table above only applies when the input fs calculation mode *FS4XIN* = 0. When *FS4XIN* = 1, fs data at twice the shown values is supported.

Input data that exceeds the set range is handled as an error, and the XIN source clock is output. At this time, the SDATO output data is determined by the *RDTSEL* setting.

When the PLL is following a source with a changing fs, such as a CD player with a variable pitch control, if the oscillator amplifier is stopped with the PLL in the locked state the fs calculation is not performed. As a result, an input frequency outside the set range will not result in an error. The oscillator amplifier must be set to continuous operation mode to handle sources such as this.

In systems that connect CLKOUT to XIN and thus do not require an oscillator element, it is not possible to perform the fs calculation. In this mode the reception range cannot be limited.

OUTPUT DATA FORMATS: NORMAL MODE (SDATO)

The output format of audio data is set up after recovery. In Normal Mode the SDATO audio data range can be of the input data format only.

The output format is set with the *OFSEL[2:0]*. The BCLK, LRCLK, and SDATO synchronize to the rising edge of CLKOUT. SDATO is synchronized to the falling edge of BCLK and is clocked on the rising edge.

After an error is detected and ERROR goes output low, the output data is synchronized with the LRCLK edge immediately following the Error signal.

The ERROR low signal is output for the signal outside the effective bit length of the output data.

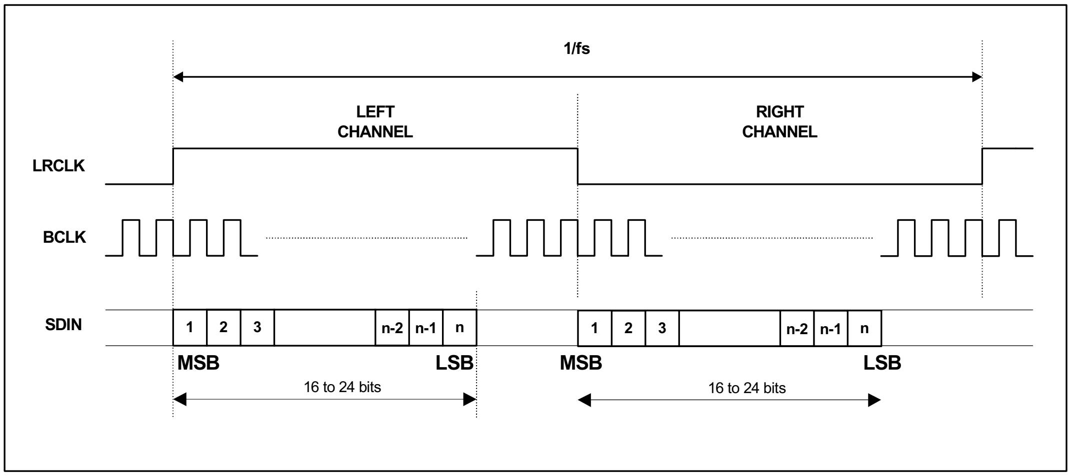


Figure 8 MSB First Left-justified Data Output (OFSEL [2:0] = 000)

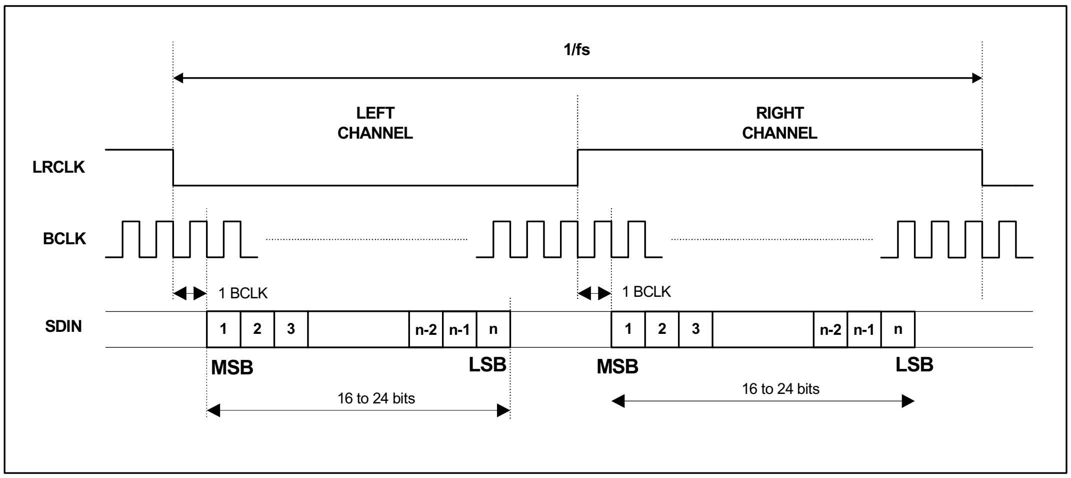


Figure 9 I^{2}S Data Output (OFSEL [2:0] = 001)

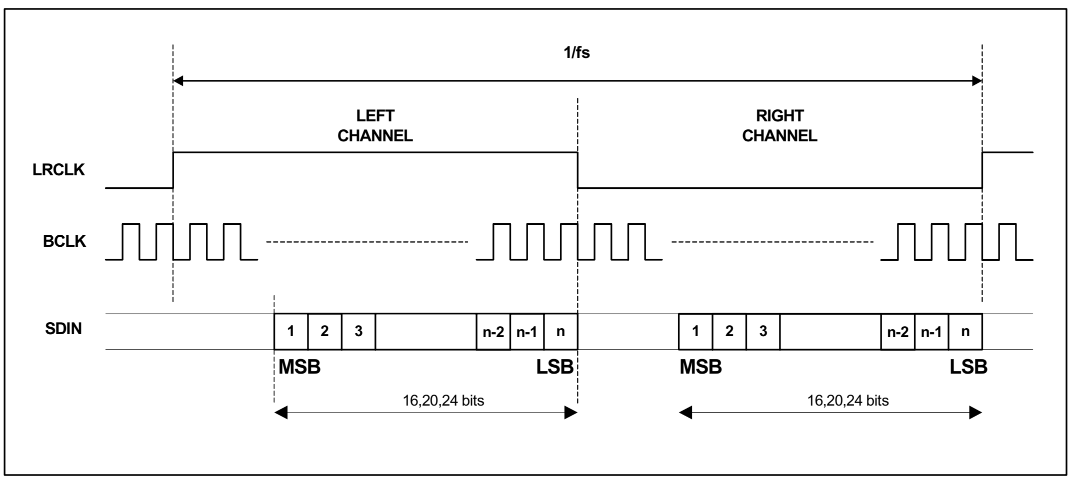


Figure 10 MSB First Right-justified Data Output (OFSEL [2:0] = 010,011, or 100)

OUTPUT DATA FORMATS: SPECIAL MODE (SDATO)

The output format of the audio data is set up after recovery In Special Mode the SDATO audio data range does not necessarily have to match the input data format.

The output format is set with the *OFSEL[2:0]* bit. The BCLK, LRCLK, and SDATO synchronize to the rising edge of CLKOUT. SDATO is synchronizes to the falling edge of BCLK and is clocked on the rising edge.

After an error is detected and ERROR goes output low, the output data is synchronized with the LRCLK edge immediately following the error signal.

Bi-phase data output synchronizes to LRCLK and the fs clock of the 128fs clock. However, when the PLL is unlocked the BCLK changes to the 64fs clock, Figure 8.

The NRZ 28bits data output contains 4 bits validity (V), user data (U), channel status (C), preamble B (indicated by Z) and 24bit LSB left justified base audio data. When preamble B is confirmed Z-bit outputs high in that frame, Figures 9 and 10.

A ERROR low signal is output for a signal outside the effective bit length of the NRZ data output.

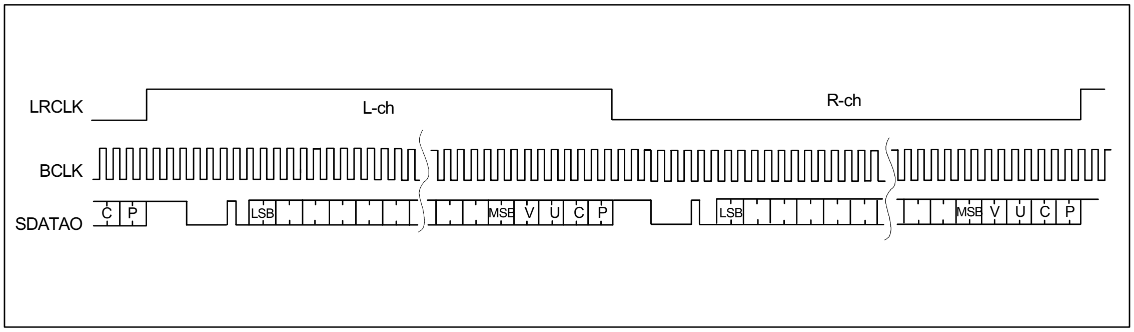


Figure 11 Data Output Timing – Biphase Data Output

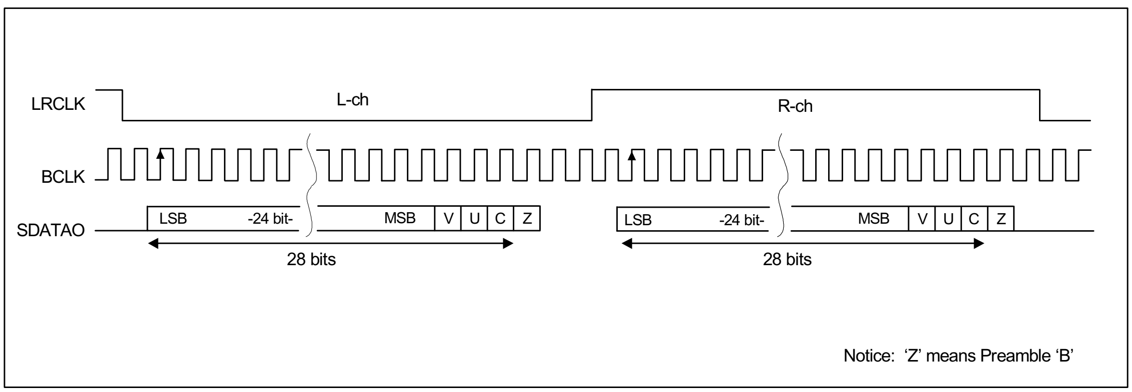


Figure 12 Data Output Timing – NRZ Data I²S Output

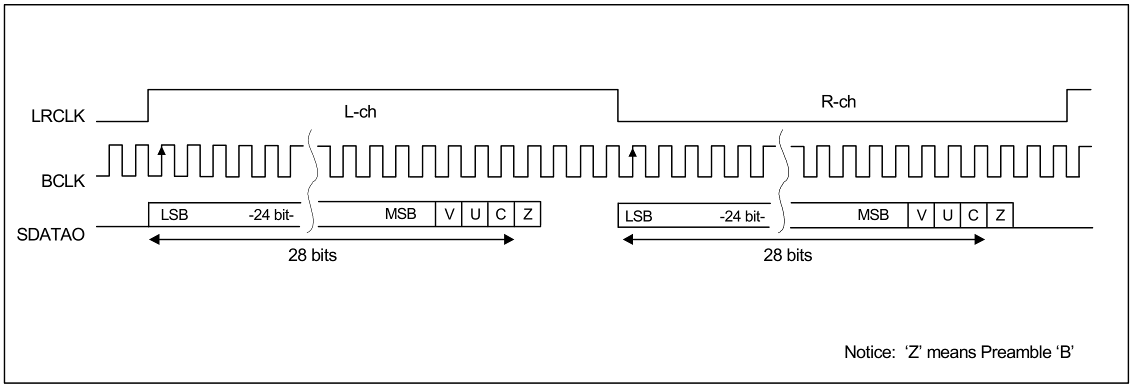


Figure 13 Data Output Timing – NRZ Data LSB First Left-justified Output

SERIAL AUDIO DATA INPUT FORMAT (SDIN)

The SDIN pin is a serial digital audio data input that can accept 24bit data data from sources such as an A/D converter output.

When the data input to the SDIN is output from the SDATO, a clock signal synchronized with the SDIN input data must be output from the BCLK and LRCLK to produce useable signals. Except for the Special Mode setting, the SDIN input must have the same format as the required output data format.

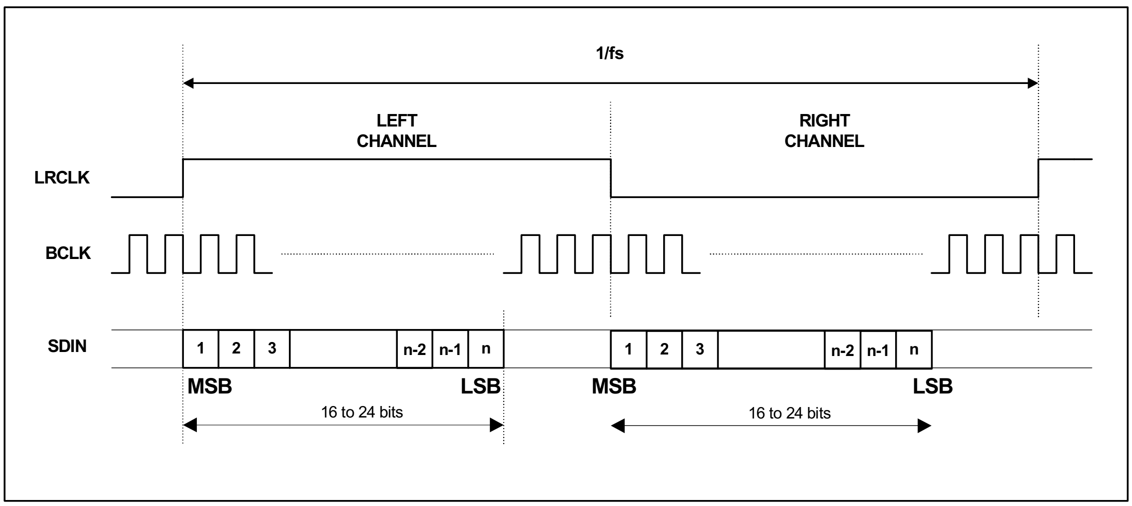


Figure 14 MSB First Left-justified Data Input

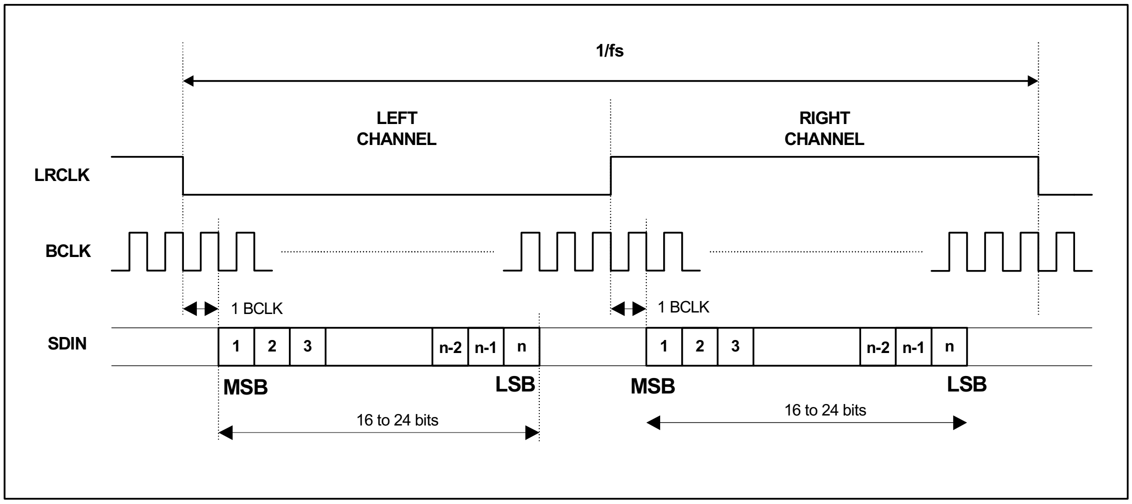


Figure 15 I²S Data Input

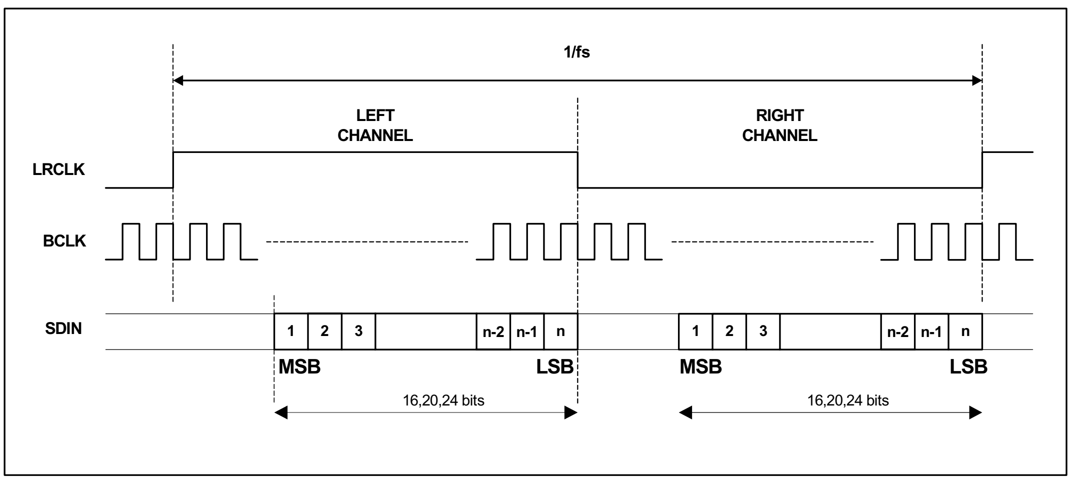


Figure 16 MSB First Right-justified Data Input

OUTPUT DATA SWITCHING (SDIN, SDATO)

The SDATO pin outputs the demodulated data when the PLL circuit is locked and the SDIN input data when the PLL circuit is unlocked. Switching between SDIN and SDATO is performed automatically according to the locked/unlocked state of the PLL circuit. When XIN is the clock source, input data synchronized with the CLKOUT, BCLK, and LRCLK clocks as the SDIN input data.

The SDIN input data can be output from SDATO by setting *RDTSTA* regardless of the PLL circuit locked/unlocked state. In this case, the CLKOUT, BCLK, and LRCLK clocks will also be switched to the XIN clock source. The switch occurs in synchronization with the LRCLK edge that follows the setting of the *RDTSTA*.

The SDATO output data can be forcibly muted by setting *RDTMUT*. The muting processing is started in synchronization with the LRCLK edge that follows the setting of the *RDTMUT*.

The SDATO output can be muted in the PLL locked state by setting *RDTSEL*.

These settings have the following priority order: *RDTSEL* < *RDTSTA* < *RDTMUT*.

When XIN is set to be the clock source with *OCKSEL*, the PLL circuit will operate as long as PLL operation is not stopped by *PDOWN[1:0]* or *PLLOPR*. In this mode the state of the PLL circuit is always output from the ERROR pin. Regardless of the PLL state information processed can be read out over the micro-controller interface.

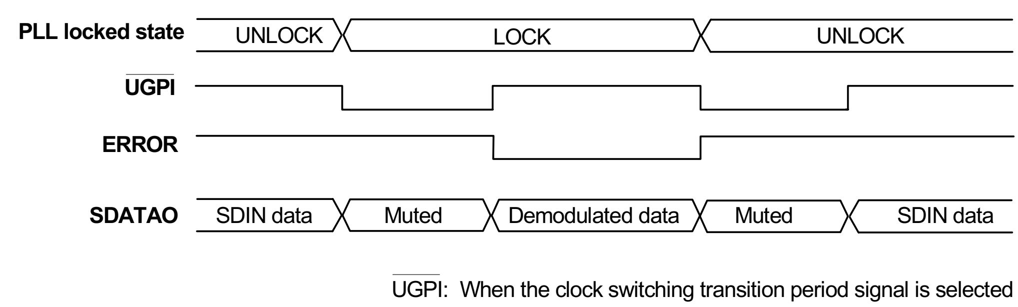


Figure 17 SDATO Output Data Switching Timing Chart (when RDTSEL is set to "0")

INPUT DATA SAMPLING FREQUENCY CALCULATION

This function calculates the input data sampling frequency using the XIN clock.

In modes where the oscillator amplifier is automatically stopped due to PLL circuit lock, the fs calculation is performed and ERROR indicates the error state. Calculation completes at the same time the oscillator amplifier is stopped and the fs value is retained. After calculation is confirmed, the value does not change until the PLL circuit goes to the unlocked state. In continuous operation mode, the oscillator amplifier continuously repeats the frequency calculation. Even when sampling the input data during which the channel status sampled information does not change within the PLL capture range, it will still be possible to read out a calculated result that follows the input data.

The calculated result can be read out from CCB address 0xEC or output registers DO4 to DO6. Note, however, that when the PLL synchronizes with data that corresponds to 32k to 192kHz. The fs calculation mode can be selected from two modes; a 32k to 96kHz calculation mode and a 64k to 192kHz calculation mode and is switched by *FS4XIN*. It is not possible to monitor an fs calculation result for the whole 32k to 192kHz range at the same time.

In systems that connect CLKOUT to XIN and thus do not require an oscillator element, the fs calculation result will always be "out of range".

ERROR OUTPUT AND PROCESSING (ERROR)

LOCK ERROR AND DATA ERROR OUTPUT

The ERROR pin outputs a high level when the PLL is in the unlocked state or an error occurs in the transmitted data.

PLL LOCK ERROR

The PLL circuit will go to the unlocked state for input data that does not conform to the bi-phase modulation rules and for input data in which the preamble B, M, and W cannot be detected.

The ERROR output goes to the high level when a PLL lock error occurs and is held high until data modulation has returned to normal for 15 to 50ms.

The rise and fall of the ERROR output is synchronized with LRCLK.

INPUT DATA TRANSMISSION ERROR

Odd input parity errors are detected from the parity bits in the input data.

When input parity errors occur for 9 or more consecutive cycles, the ERROR output goes high. The high level is held until the PLL is in a locked state for 15 to 50ms, then ERROR returns low.

When 8 or fewer consecutive input parity errors occur, an error will only be output for intervals between sub-frames for errors that occurred only when non-PCM data is recognized by the channel status data delimiter bit 1. In this case, the parity error flag used for data recognized as PCM data will not be output.

OTHER ERRORS

Even when ERROR has gone low, the WM8803 always acquires bits 24 to 27 (sampling frequency) of the channel status and compares the current data with that of the previous block. If any differences are found, ERROR is immediately set to the high level and the state is handled as a PLL lock error.

Similarly, when *FLIMIT* is set to restrict fs input range and the input fs calculation results are reflected in the error flags, fs calculation results are compared continuously. If a disparity occurs in the data, ERROR will immediately go high, and the state will be handled as a PLL lock error.

ERROR OCCURRENCE PROCESSING

This section describes the data processing performed when an error occurs. When up to 8 consecutive input parity errors occur and if the transmitted data is PCM audio data, the data is replaced with the corresponding left and right channel data from the immediately preceding frame. If the transmitted data is non-PCM data, the error data is output without modification. Non-PCM data is based on data that was detected before the input parity error that occurred, and is data for which the channel status bit 1 non-PCM data detection bit is “1”.

The output data is muted when 9 or more consecutive parity errors, or a PLL lock error, occur.

For the channel status output when a parity error occurs, the data for the previous block is retained.

DATA AND DETECTION FLAGS	PLL LOCK ERROR	INPUT PARITY ERROR (A)	INPUT PARITY ERROR (B)	INPUT PARITY ERROR (C)
SDATO output pin	L	L	Previous data	Output
Input fs calculation	L	L	Output	Output
Channel status data	L	L	Previous data	Previous data
Sub-code Q data	L	L	Output	—

Table 10 Data Processing when Errors Occur

Notes:

1. Input parity error (A): When 9 or more consecutive parity errors occur
2. Input parity error (B): When up to 8 consecutive parity errors occur in audio data
3. Input parity error (C): When up to 8 consecutive parity errors occur in non-PCM burst data

The figure below presents an example of the data processing performed when a parity error occurs.

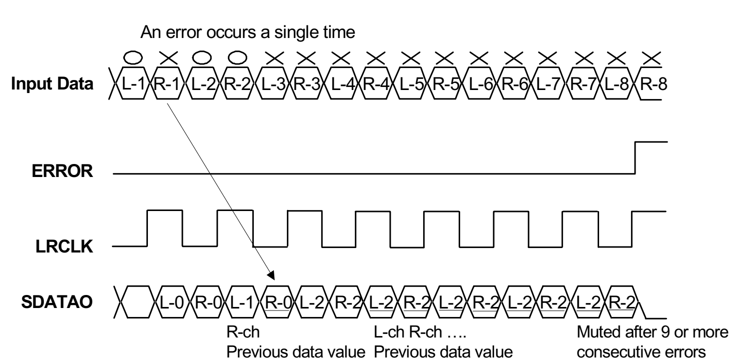


Figure 18 Data Processing Example Following a Parity Error (When PCM data is received)

ERROR RECOVERY PROCESSING

When the preamble B, M, and W are detected, the PLL circuit goes to the locked state and data demodulation starts. The SDATO output data starts on the first LRCLK edge after ERROR goes low.

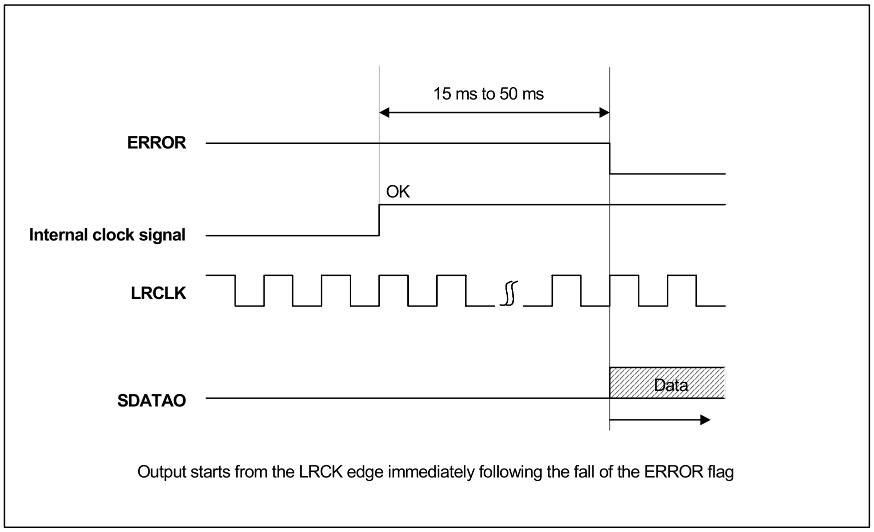


Figure 19 Data Processing at the Start of Data Demodulation

CHANNEL STATUS DATA

DATA DELIMITER BIT 1 OUTPUT ($\overline{\text{AUDIO}}$)

$\overline{\text{AUDIO}}$ outputs the channel status bit 1, which indicates whether or not the input bi-phase data is PCM audio data.

$\overline{\text{AUDIO}}$	OUTPUT CONDITIONS
L	PCM audio data (CS bit 1 = low)
R	Non-PCM data (CS bit 1 = high)

Table 11 $\overline{\text{AUDIO}}$ Output

EMPHASIS INFORMATION OUTPUT (E/INT)

E/INT has a shared function as a micro-controller interface interrupt output or, in the initial settings state, it outputs the presence or absence of emphasis of the input signal. This emphasis has a time constant of 50/15µs for use in consumer products or broadcast studios.

E/INT	OUTPUT CONDITIONS
L	No pre-emphasis
R	50/15µs pre-emphasis

Table 12 E/INT Output

USER GENERAL PURPOSE INTERFACE OUTPUT PORT ($\overline{\text{UGPI}}$)

$\overline{\text{UGPI}}$ is a user-settable output port that supports the following functions.

— Micro-controller interface register output

— Clock switching transition period signal output

GPISEL selects between these functions. In the initial settings, the micro-controller interface register *GPIDAT* is allocated to this pin. The initial setting of the *GPIDAT* register is 1, so a high level will be output from $\overline{\text{UGPI}}$.

MICRO-CONTROLLER INTERFACE REGISTER OUTPUT (OPTICAL RECEIVER MODULE POWER DOWN EXAMPLE)

This section describes an example in which $\overline{\text{UGPI}}$ outputs a micro-controller interface register, and how that signal is used as the power supply control signal for an optical receiver module.

1. Connect the $\overline{\text{UGPI}}$ output to the optical receiver module power supply control switch.
2. After clearing a reset due to $\overline{\text{PD}}$, the micro-controller interface register output will be selected as the initial setting for $\overline{\text{UGPI}}$. As a result, the *GPIDAT* set value will be output.
3. After a reset is cleared, the initial value of *GPIDAT* = 1, and so $\overline{\text{UGPI}}$ will be output high. The control switch will be in the off state, and data will not be supplied from the optical receiver module.
4. Setting *GPIDAT* = 0 will activate the optical receiver module supply data. Controlling the $\overline{\text{UGPI}}$ output with *GPIDAT* will allow current drain to be minimized when the optical receiver module is not used.

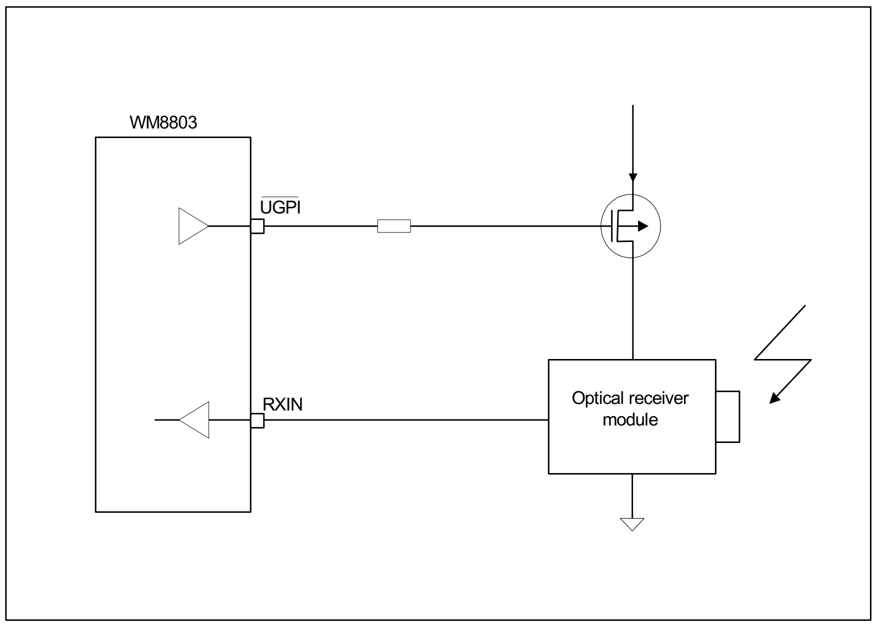


Figure 20 $\overline{\text{UGPI}}$ Output Example (Optical Receiver Module Power Supply Control)

MICRO-CONTROLLER INTERFACE REGISTER OUTPUT (DIGITAL DATA INPUT SWITCH CONTROL SIGNAL EXAMPLE)

$\overline{\text{UGPI}}$, when used as a micro-controller interface register output, can be used as a control signal that switches the digital data input.

If more than one type of data input is required an input selector circuit and a control signal will be required. It is possible to implement two digital data inputs without having to provide a control signal from the micro-controller by using the $\overline{\text{UGPI}}$ output.

Note that after a reset is cleared, the initial value of *GPIDAT* will be 1, and as a result, $\overline{\text{UGPI}}$ will output a high level.

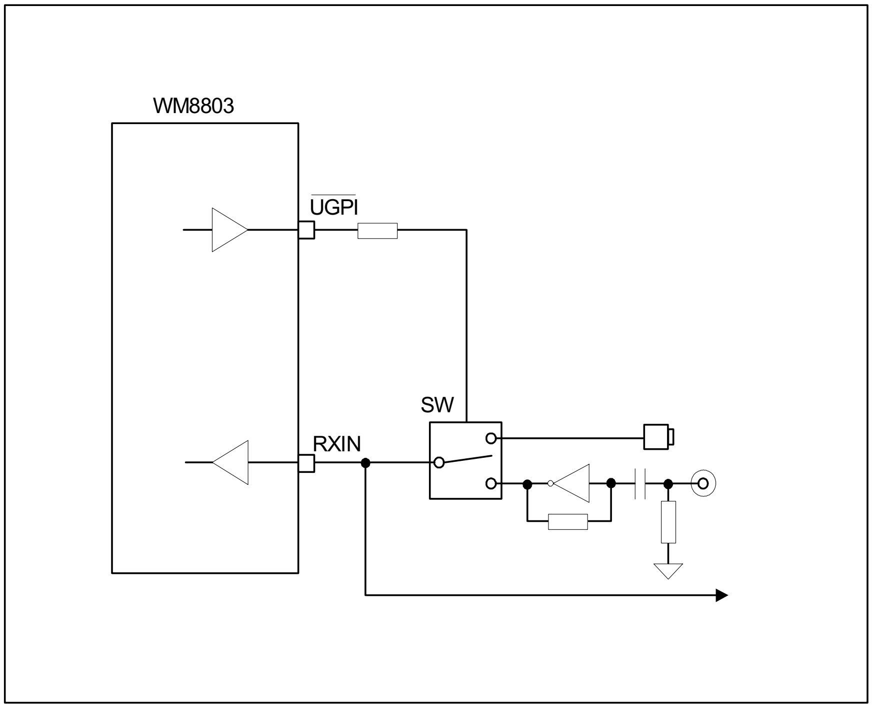


Figure 21 $\overline{\text{UGPI}}$ Output Usage Example (Data Input Switching Example)

CLOCK SWITCHING TRANSITION PERIOD SIGNAL OUTPUT

This section describes operation when $\overline{\text{UGPI}}$ is selected as the clock switching transition period signal.

When there are changes to the PLL circuit locked/unlocked state, the clock switching transition period signal reports to external circuits the output clock state switching transitions. This signal allows the application to grasp the PLL lock state transitions and the timing of changes in the clock signals. *GPISEL* is used to select this function.

After setting *GPISEL*, $\overline{\text{UGPI}}$ will initially output a high level. This is followed by output low level pulses when the output clock changes due to changes in the PLL circuit locked/unlocked state.

In the lock pull-in process, the $\overline{\text{UGPI}}$ falling edge is triggered by the word clock generated by the XIN clock after input data is detected and the PLL circuit locks, and by $\overline{\text{UGPI}}$ rising with the same timing as ERROR after a fixed period has elapsed.

In the process where the PLL lock state is lost, the $\overline{\text{UGPI}}$ low level pulse is formed by $\overline{\text{UGPI}}$ falling with the same timing as the PLL lock detection signal ERROR and by $\overline{\text{UGPI}}$ rising after a fixed number of counts of the word clock generated from XIN.

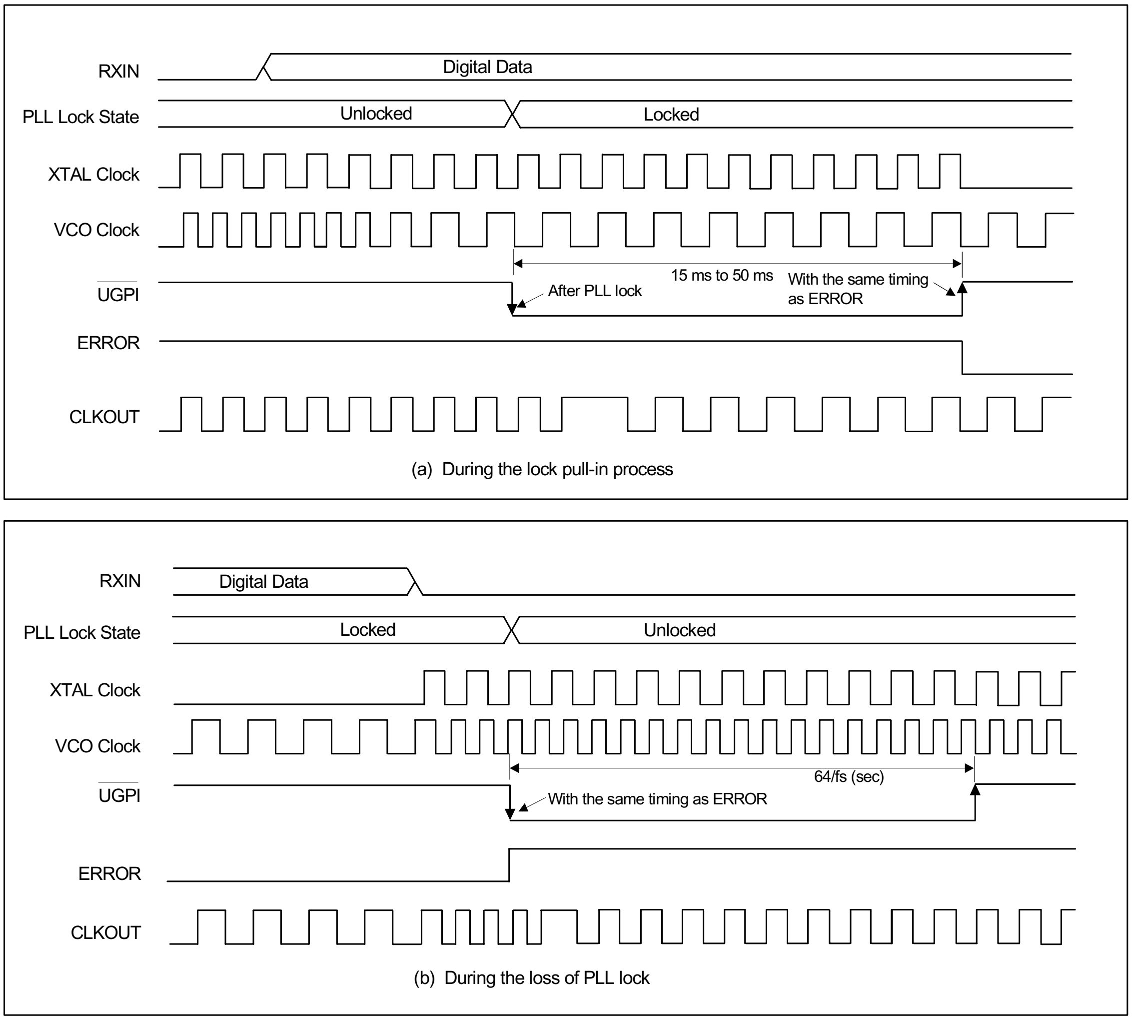


Figure 22 Clock Switching Timing

MICRO-CONTROLLER INTERFACE (E/INT, CE, CL, DI, DO)

INTERRUPT OUTPUT (E/INT)

The E/INT pin can be set to function as the micro-controller interface interrupt output using *INTSEL*.

An interrupt is issued when a change occurs in the PLL lock state, the output data information or other aspects of WM8803 operation.

The interrupt output function consists of registers for selecting interrupts, the E/INT pin to output those state transitions, and the registers that store interrupt related data.

The E/INT pin normally outputs a low level, but outputs a high level when an interrupt occurs. After outputting a high level, it returns to the low level according to the *INTOPF* setting.

INTOPF selects whether the E/INT pin holds the high level for a fixed period and then is cleared (returning to the low level), or is cleared at the same time as the output register is read.

The interrupts can be selected from the items listed in Table 13. More than one of these items can be set to be interrupts at the same by setting the contents of CCB address 0xEA. The interrupt signal is issued whenever any one of the interrupt events occurs.

E/INT output = (selected interrupt 1) + (selected interrupt 2) + ... + (selected interrupt n)

NO.	COMMAND	DESCRIPTION
1	INTERR	Output when the state of the ERROR pin changes.
2	INTPCM	Output when the state of the $\overline{\text{AUDIO}}$ pin changes.
3	INTEMP	Output when the state of the pre-emphasis information changes.
4	INTVFL	Output when the state of the validity flag changes.
5	INTFSC	Output when the input fs calculation result changes.
6	INTCSF	Output when the first 48 bits of the channel status data is updated.
7	INTSQY	Output when the sub-code Q data can be read out.

Table 13 Interrupt Event Settings

When an interrupt event occurs the content of the selected interrupt events is stored in the CCB address 0xEB output registers DO1 to DO7. The read registers for event items 1 through 4 read out the current state of those events regardless of the E/INT output. For event items 5 through 7, the state is stored when the event occurs.

To monitor interrupt event item 5 in the PLL locked state, the oscillator amplifier must be set to continuous operation mode, since the oscillator amplifier clock is used.

When E/INT is set to output a high-level pulse when interrupt event occurs, the pulse width for each interrupt event will be between 1/2 fs and 3/2 fs.

When the WM8803 is set so that E/INT is cleared after the output register is read, the clear operation is performed immediately after output register 0xEB is reset. The data for interrupt events 6 and 7 is updated within the periods shown in Table 14, the corresponding read registers should be read as soon as possible after the event is detected.

DATA	UPDATE INTERVAL
Channel status and preamble B	2ms to 6ms
Sub-code Q data	13.3ms (fs = 44.1kHz), 6.65ms (2x speed)

Table 14 Data Update Intervals (Input fs = 32k to 96kHz)

CCB ADDRESSES

The address locations in Table 15 are those used to set the parameters, write data values and to read data values from the WM8803 over the micro-controller interface.

The micro-controller interface data format conforms to that of the Sanyo-developed CCB serial bus format. However, a three state circuit is adopted for the data output instead of the open drain circuit used in CCB.

Data is input or output after input of the CCB address. See the I/O timing chart for details on the data input and output timing.

REGISTER CONTENT	R/W	CCB ADDRESS	B0	B1	B2	B3	A0	A1	A2	A3
Function settings data 1	Write	0xE8	0	0	0	1	0	1	1	1
Function settings data 2	Write	0xE9	1	0	0	1	0	1	1	1
Function settings data 3	Write	0xEA	0	1	0	1	0	1	1	1
Interrupt data output	Read	0xEB	1	1	0	1	0	1	1	1
Fs value, CS data output	Read	0xEC	0	0	1	1	0	1	1	1
Sub-code Q data output	Read	0xED	1	0	1	1	0	1	1	1

Table 15 Register I/O Content and CCB Addresses

DATA WRITE PROCEDURE

The data input bit length is 16 bits.

After inputting data to one of the CCB addresses 0xE8 to 0xEA, set CE to the high level.

Input data is acquired on the rising edge of CL.

The bits marked “0” in the table are reserved bits. A value of 0 must be written to these bits.

DATA READ PROCEDURE

Read data is output from DO and goes to the high-impedance state when CE is low. Output starts on the CE rising edge following the establishment of the output address by the CCB command on the DI pin. After operation the DO pin is returned to the high-impedance state by setting CE low.

The number of data bits read out differs with the type of data read. Interrupt data has 8bits, the channel status related data (0xEC) has 56bits, and the sub-code Q data (0xED) has 88bits. However, it is not necessary to read out all the data. During readout it is possible to read data up to the point when the CL clock is stopped and the CE pin is set low. For example, when reading the sub-code Q data, if the CRC flags are read and the data is seen to be corrupted, there is no need to read the data following.

I/O TIMING

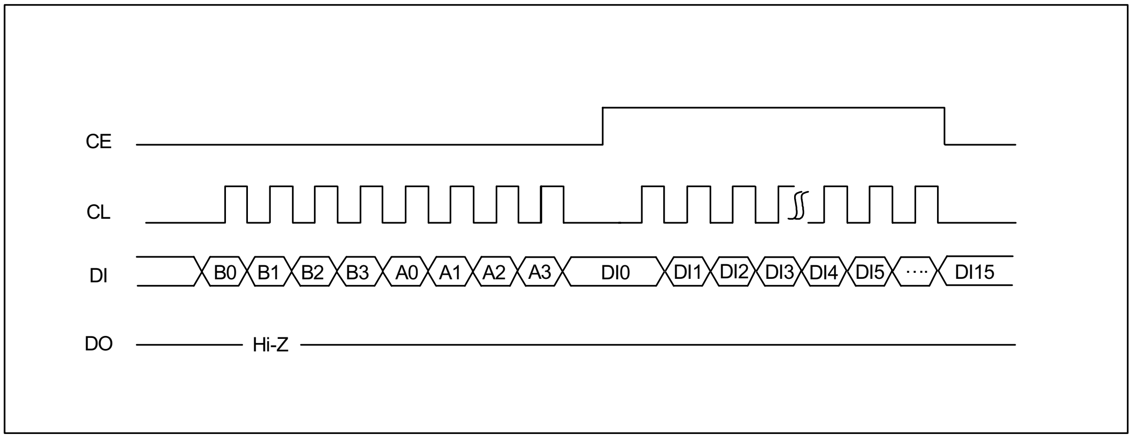


Figure 23 Input Timing Chart (Normal, Low Clock)

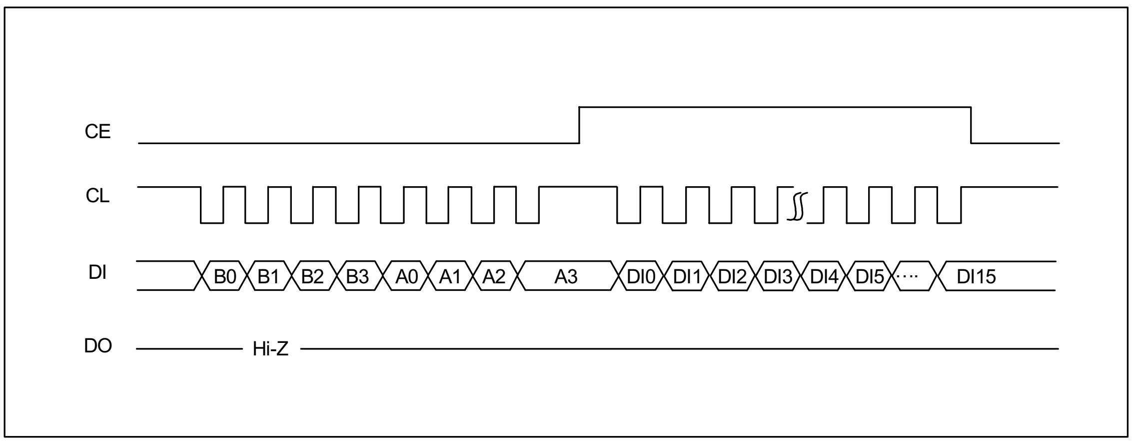


Figure 24 Input Timing Chart (Normal, High Clock)

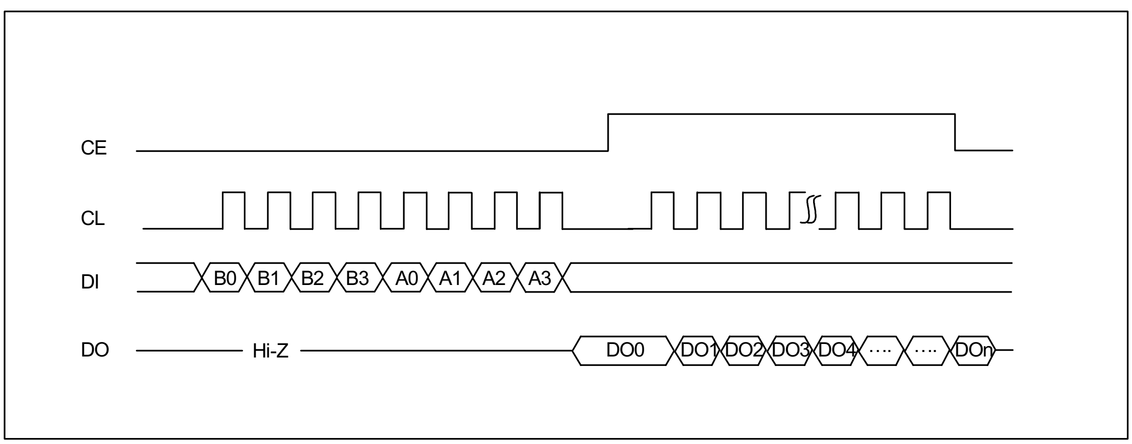


Figure 25 Output Timing Chart (Normal, Low Clock)

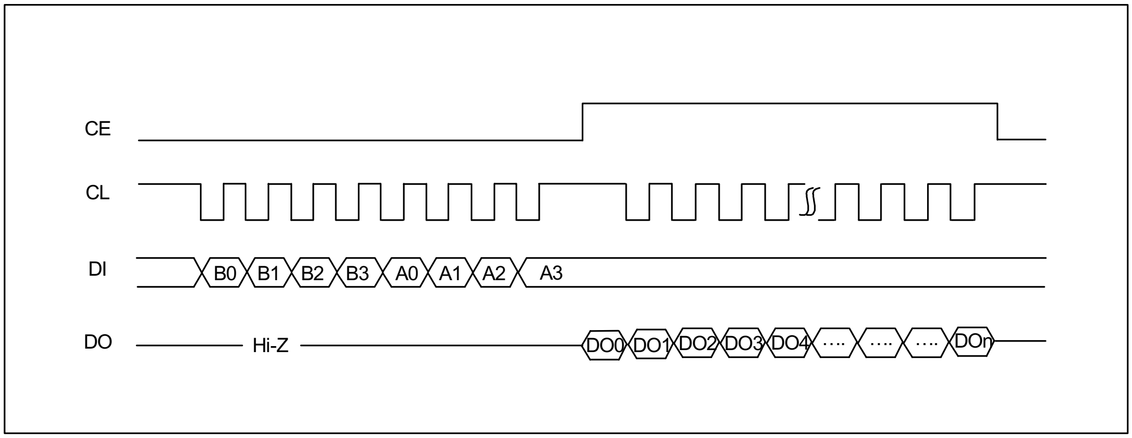


Figure 26 Output Timing Chart (Normal, High Clock)

Note:

1. It is necessary to read DO0 with a separate port from DI.

WRITE REGISTER TABLE

The table below lists the write registers.

INPUT REGISTER	0XE8	0XE9	0XEA
DI0	SYSRST	GPISEL	INTOPF
DI1	0	GPIDAT	0
DI2	PDOWN0	FLIMIT	0
DI3	PDOWN1	FS4XIN	0
DI4	PLLOPR	FSSEL0	0
DI5	PLLCK0	FSSEL1	0
DI6	PLLCK1	FSSEL2	0
DI7	MCKHFO	FSSEL3	0
DI8	0	OFSEL0	INTSEL
DI9	AMPOPR	OFSEL1	INTERR
DI10	AMPCNT	OFSEL2	INTPCM
DI11	OCKSEL	0	INTEMP
DI12	XISEL0	RDTSEL	INTVFL
DI13	XISEL1	RDTSTA	INTFSC
DI14	XISEL2	RDTMUT	INTCSF
DI15	XISEL3	0	INTSQY

Table 16 List of Write Registers

The shaded areas are reserved bits. Only a value of 0 may be written to these bits.

WRITE DATA DETAILED DOCUMENTATION

DI7	**DI6**	**DI5**	**DI4**	**DI3**	**DI2**	**DI1**	**DI0**
MCKHFO	PLLCK1	PLLCK0	PLLOPR	PDOWN1	PDOWN0	0	SYSRST
DI15	**DI14**	**DI13**	**DI12**	**DI11**	**DI10**	**DI9**	**DI8**
XISEL3	XISEL2	XISEL1	XISEL0	OCKSEL	AMPCNT	AMPOPR	0

Table 17 Input Register Function Settings 1: System Settings (0xE8)

SYSRST: **System reset**

0: No reset performed (initial value)

1: Reset all circuits other than the command registers.

PDOWN[1:0]: **Low power mode settings** (Allows the operation of specific functions only)

00: Normal operation (initial value)

01: Only the oscillator amplifier operates.

10: Only the oscillator amplifier and the output clock divider operate.

11: Reserved

PLLOPR: **PLL (VCO) operate/stop setting**

0: Operate (initial value)

1: Stop

PLLCK[1:0]: **PLL locked state clock frequency setting**

00: 256fs (initial value)

01: 384fs

10: 512fs

11: (512/2)fs = 256fs

MCKHFO: **CLKOUT output clock frequency setting**

0: 1/1 output (initial value)

1: 1/2 output

In the PLL locked state when switching from the 512fs setting with the *PLLCK[1:0]* = “10” to the (512/2)fs setting with the *PLLCK[1:0]* = “11” it is possible to maintain clock continuity without entering the PLL lock error state..This is also the case when switching in the reverse direction.

For systems such as portable equipment power consumption can be minimized,by setting *PLLCK[1:0]* = “00” (256fs). Systems such as AV amplifiers that required best performance, the *PLLCK[1:0]* = “10” (512fs) or the *PLLCK[1:0]* = “11” (512/2fs) setting is recommended.

AMPOPR:	**Oscillator amplifier operate/stop setting** 0: Operate (initial value) 1: Stop
AMPCNT:	**Oscillator amplifier state setting** 0: Automatically stop in the PLL locked state (initial value) 1: Always operate
OCKSEL:	**Clock source setting** 0: Use the XIN clock as the source when the PLL is unlocked (initial value) 1: Use the XIN clock as the source regardless of the PLL state.
XISEL[3:0]:	**XIN input frequency setting** 0000: 11.2896MHz (initial value) 0001: 12.288MHz 0010: 16.9344MHz 0011: Reserved 0001: 22.5792MHz 0010: 24.576MHz 0010: 33.8688MHz 0011: Reserved 1xxx: Setting used when the CLKOUT pin and the XIN pin are connected.

DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
FSSEL3	FSSEL2	FSSEL1	FSSEL0	FS4XIN	FLIMIT	GPIDAT	GPISEL
DI15	**DI14**	**DI13**	**DI12**	**DI11**	**DI10**	**DI9**	**DI8**
0	RDTMUT	RDTSTA	RDTSEL	0	OFSEL2	OFSEL1	OFSEL1

Table 18 Input Register Function Settings 1: I/O Data Settings (0xE9)

GPISEL: **$\overline{\text{UGPI}}$ pin setting**

0: Outputs the micro-controller interface register state. (initial value)

1: Outputs the clock switching transition period signal.

GPIDAT: **$\overline{\text{UGPI}}$ pin setting** (Only valid when register output mode is set up)

0: Outputs the low level.

1: Outputs the high level. (initial value)

FLIMIT: **Input data reception limitation setting**

0: No reception limitation. All data within the PLL locking range can be received. (initial value)

1: Reception is limited. The input fs calculation result is reflected in the error flag according to the *FSSEL[3:0]* setting.

FS4XIN: **Input fs calculation range setting**

0: Perform fs calculation for input data in the range 32k to 96 kHz. (initial value)

1: Perform fs calculation for input data in the range 64k to 192 kHz.

FSSEL[3:0]: **Input data reception range setting** (When *FLIMIT* = “1” and *FS4XIN* = “0”)

0000: 32k, 44.1k, 48k, 64k, 88.2k, or 96kHz (initial value)

0001: 32kHz only

0010: 44.1kHz only

0011: 48kHz

0100: 88.2kHz only

0101: 96kHz only

0110: 44.1k or 88.2kHz only

0111: 48k or 96kHz only

1000: 32k or 44.1k or 48kHz

1001-1111:Reserved

FSSEL[3:0]: **Input data reception range setting** (When *FLIMIT* = “1” and *FS4XIN* = “1”)

0000: 64k, 88.2k, 96k 128k, 176.4k, or 192kHz (initial value)

0001: 64kHz only

0010: 88.2kHz only

0011: 96kHz only

0100: 176.4kHz only

0101: 192kHz only

0110: 88.2k or 176.4kHz only

0111: 96k or 192kHz only

1000: 64k or 88.2k or 96kHz only

1001-1111: Reserved

OFSEL[2:0]: **Serial audio data output format setting**

000: 24-bit MSB first left-justified data output (initial value)

001: 24-bit I^2S data output

010: 24-bit MSB first right-justified data output

011: 20-bit MSB first right-justified data output

100: 16-bit MSB first right-justified data output

101-100: Reserved

101: Bi-phase data output

110: 28-bit I^2S data output (NRZ data output)

111: 28-bit LSB first left-justified data output (NRZ data output)

RDTSEL: **SDATO output setting in the PLL unlocked state**

0: Output the SDIN data in the PLL unlocked state. (initial value)

1: Mute the output in the PLL unlocked state.

RDTSTA: **SDATO output setting**

0: Observe the *RDTSEL* setting. (initial value)

1: Output the SDIN data regardless of the PLL state.

RDTMUT: **SDATO mute setting**

0: Output the data selected by *RDTSEL*. (initial value)

1: Mute the output.

DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
0	0	0	0	0	0	0	INTOPF
DI15	**DI14**	**DI13**	**DI12**	**DI11**	**DI10**	**DI9**	**DI8**
INTQSY	INTCSF	INTFSC	INTVFL	INTEMP	INTPCM	INTERR	INTSEL

Table 19 Input Register Function Settings 1: Interrupt Settings (0xEA)

INTOPF: **E/INT output setting** (Only valid when the interrupt output function is selected.)

0: Output a high level when an interrupt occurs. (initial value)

1: Output a high level pulse when an interrupt occurs.

INTSEL: **E/INT pin setting**

0: Output the channel status emphasis information. (initial value)

1: Output the micro-controller interface interrupt signal.

INTERR: **ERROR signal output setting**

0: Do not output this signal. (initial value)

1: Output changes to the ERROR pin state.

INTPCM: **$\overline{\text{AUDIO}}$ signal output setting**

0: Do not output this signal. (initial value)

1: Output changes to the $\overline{\text{AUDIO}}$ pin state.

INTEMP: **Channel status emphasis detection flag output setting**

0: Do not output this flag. (initial value)

1: Output the emphasis detection flag.

INTVFL: **Parity flag detection flag output setting**

0: Do not output this flag. (initial value)

1: Output the parity flag.

INTFSC: **PLL lock frequency calculation result update flag output setting**

0: Do not output this flag. (initial value)

1: Output the PLL lock frequency calculation result update flag.

INTCSF: **First 48 bits of channel status data update flag output setting**

0: Do not output this flag. (initial value)

1: Output the first 48 bits of channel status data update flag.

INTQSY: **Sub-code Q data readout load signal detection flag output setting**

0: Do not output this flag. (initial value)

1: Output the flag that indicates updates to the 80 bits of sub-code Q data including the CRC.

If E/INT is set up for high level output when an interrupts are generated with *INTOPF*, the high-level state will be maintained until the interrupt event output (address 0xEB) is read out. When that data has been read, the E/INT output will return to the normal low level.

The channel status update flag is computed by comparing the current data with the first 48bits of the previous block, and determining the channel status to have been updated if the data is the same.

READ REGISTER TABLE

The table below lists the read registers.

OUTPUT REGISTER	0XEB	0XEC	0XED
DO0	0	0	CRC
DO1	OUTERR	OUTERR	CRC
DO2	OUTPCM	OUTPCM	0
DO3	OUTEMP	0	0
DO4	OUTVFL	FSCAL0	0
DO5	OUTFSC	FSCAL1	0
DO6	OUTCSF	FSCAL2	0
DO7	OUTSQY	0	0
DO8	0	Bit 0	Control
DO9	0	Bit 1	Control
DO10	0	Bit 2	Control
DO11	0	Bit 3	Control
DO12	0	Bit 4	Address
DO13	0	Bit 5	Address
DO14	0	Bit 6	Address
DO15	0	Bit 7	Address
DO16	0	Bit 8	Track
DO17	0	Bit 9	Track
DO18	0	Bit 10	Track
DO19	0	Bit 11	Track
DO20	0	Bit 12	Track
DO21	0	Bit 13	Track
DO22	0	Bit 14	Track
DO23	0	Bit 15	Track
DO24	0	Bit 16	Index
…..	0	…..	…..
DO54	0	Bit 46	Frame
DO55	0	Bit 47	Frame
DO56	0	0	zero
…..	0	0	…..
DO86	0	0	abs frame
DO87	0	0	abs frame

Table 20 List of Read Registers

READ DATA DETAILED DOCUMENTATION

DO7	DO6	DO5	DO4	DO3	DO2	DO1	DO0
OUTSQY	OUTCSF	OUTFSC	OUTVFL	OUTEMP	OUTPCM	OUTERR	0

Table 21 Output Register: Interrupt Data Output (0xEB)

OUTERR: **ERROR output** (Outputs the state when read)

0: No transmission error and the PLL circuit is in the PLL locked state.

1: Either a transmission error occurred or the PLL circuit is in the unlocked state.

OUTPCM: **$\overline{\text{AUDIO}}$ output** (Outputs the state when read)

0: Non-PCM signal not detected.

1: Non-PCM signal detected.

OUTEMP: **Channel status emphasis detection** (Outputs the state when read)

0: No pre-emphasis.

1: 50/15µs pre-emphasis was applied.

OUTVFL: **Parity flag detection** (Outputs the state when read)

0: No error.

1: Parity error detected.

OUTFSC: **Input fs calculation result** (Cleared after read)

0: No input fs calculation result update.

1: The fs calculation result was updated.

OUTCSF: **First 48 bits of the channel status update result** (Cleared after read)

0: This data was not updated.

1: The data has been updated.

OUTQSY: **Sub-code Q data readout load signal detection** (Cleared after read)

0: Not detected.

1: Detected.

	DO7	DO6	DO5	DO4	DO3	DO2	DO1	DO0
0	*0*	*FSCAL2*	*FSCAL1*	*FSCAL0*	*0*	*OUTPCM*	*OUTERR*	*0*
8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
16	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
24	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
32	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
40	Bit 39	Bit 38	Bit 37	Bit 36	Bit 35	Bit 34	Bit 33	Bit 32
48	Bit 47	Bit 46	Bit 45	Bit 44	Bit 43	Bit 42	Bit 41	Bit 40

Table 22 Output Register: Input fs Calculation Result and Channel Status Data (0xEC)

Error information, non-PCM information, input fs calculation result, and channel status data can be read from this register. Note that the error information and the non-PCM data information are the same as those read from 0xEB.

OUTERR: **ERROR output** (Outputs the state when read)

0: No transmission error and the PLL circuit is in the PLL locked state

1: Either a transmission error occurred or the PLL circuit is in the unlocked state.

OUTPCM: $\overline{\textbf{AUDIO}}$ output (Outputs the state when read)

0: Non-PCM signal not detected.

1: Non-PCM signal detected.

The input data fs calculation result is allocated as shown in Table 23. The target calculation frequencies differ depending on the *FS4XIN* setting. The calculation range differs slightly depending on the XIN clock frequency.

FSCAL2	FSCAL1	FSCAL0	FS4XIN = 0		FS4XIN = 1	
			TARGET FS	CALCULATED RANGE	TARGET FS	CALCULATED RANGE
0	0	0	Out of range	—	Out of range	—
0	0	1	32kHz	30.9k to 33.2kHz	64kHz	62.0k to 66.4kHz
0	1	0	44.1kHz	42.5k to 45.8kHz	88.2kHz	85.5k to 91.0kHz
0	1	1	48kHz	46.3k to 49.9kHz	96kHz	92.6k to 99.0kHz
1	0	0	64kHz	62.1k to 66.4kHz	128kHz	124.0k to 132.8kHz
1	0	1	88.2kHz	85.6k to 91.0kHz	176.4kHz	171.0k to 182.2kHz
1	1	0	96kHz	92.6k to 99.0kHz	192kHz	185.1k to 198.0kHz
1	1	1	—	—	—	—

Table 23 Input fs Calculation Result (Ta = 25°C, VDD = 3.3V, XIN = 11.2896MHz)

The channel status reads out the first 48bits of the data.

Since the channel status consists of 192 frames, updated data can always be read out by reading with a period 192 times the period of the input sampling frequency.

The processing load on the micro-controller can be reduced by setting the E/INT pin to interrupt the output and using the update flag interrupt to read out the data. This flag is output when a comparison of the first 48bits of the current data and the data for the previous block indicates that they are the same.

	DO7	DO6	DO5	DO4	DO3	DO2	DO1	DO0
0	0	0	0	0	0	0	CRC	CRC
8	Address	Address	Address	Address	Control	Control	Control	Control
16	Track	Track	Track	Track	Track	Track	Track	Track
24	Index	Index	Index	Index	Index	Index	Index	Index
32	Minute	Minute	Minute	Minute	Minute	Minute	Minute	Minute
40	Second	Second	Second	Second	Second	Second	Second	Second
48	Frame	Frame	Frame	Frame	Frame	Frame	Frame	Frame
56	Zero	Zero	Zero	Zero	Zero	Zero	Zero	Zero
64	abs minute	abs minute	abs minute	abs minute	abs minute	abs minute	abs minute	abs minute
72	abs second	abs second	abs second	abs second	abs second	abs second	abs second	abs second
80	abs frame	abs frame	abs frame	abs frame	abs frame	abs frame	abs frame	abs frame

Table 24 Output Register: Sub-code Q Data with CRC Flags Output (0xED)

The cyclic redundancy code (CRC) is a set of flags that indicates the correctness of the 80bits of sub-code Q data. Note that the same data is output for both the DO0 and DO1 CRC flags.

When sub-code Q data is included in the input data, the result of the CRC calculation can be read out along with the data.

To read out the sub-code Q data, the data must be read out with INTQSY set as the E/INT interrupt output function, and the IC must be set up to output the load signal.

When sub-code Q data is detected, the E/INT signal will output a high level or a high-level pulse. The sub-code Q data is updated on each rising edge on the E/INT signal. Applications must complete readout of this data within 13.3ms (standard speed) or 6.6ms (2 × speed) of the rising edge of the E/INT signal.

CRC	OUTPUT CONDITIONS
L	Errors were found in the sub-code Q data.
H	The sub-code Q data is correct.

Table 25 CRC Flag Output

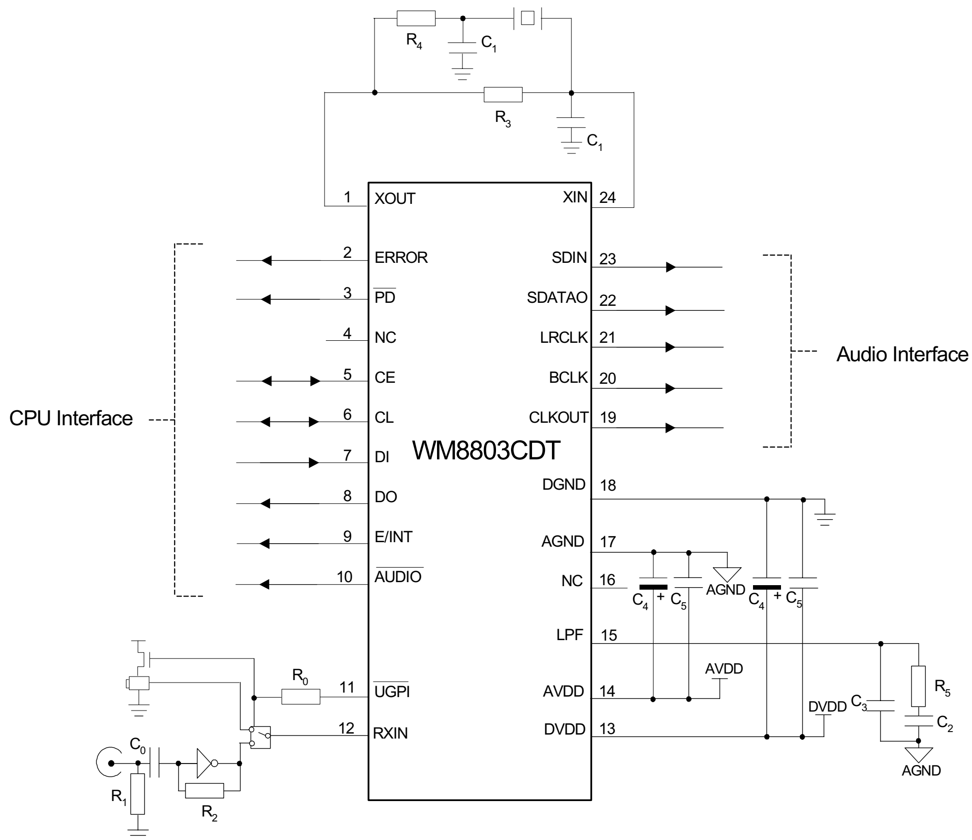
SAMPLE APPLICATION

The power supply pin de-coupling capacitors (0.1µF and 10µF) should be located as close as possible to the WM8803. Use ceramic and good quality electrolytic capacitors respectively, with good high-frequency characteristics for these components.

Use a capacitor with a minimal thermal coefficient for the PLL loop filter capacitor.

There are no constraints on the NC pin levels. IC operation will not be affected by leaving them open or by holding them fixed at particular levels.

RECOMMENDED EXTERNAL COMPONENTS



NOTES:

1. AGND and DGND should be connected as close to the WM8803 as possible.
2. C_2, C_3, C_4, and C_5 should be positioned as close to the WM8803 as possible.
3. Capacitor types should be carefully chosen. Capacitors with very low ESR are recommended for optimum performance.

RECOMMENDED EXTERNAL COMPONENTS VALUES

COMPONENT REFERENCE	SUGGESTED VALUE	USE	NOTES
R0	50 to 1kΩ	—	
R1	75Ω	Coaxial terminator	
R2	50k to 100kΩ	Input amplifier feedback	
R3	1MΩ	Oscillator amplifier feedback	
R4	150 to 330Ω	Oscillator amplifier current limited	
R5	*	PLL loop filter	Tolerance: ±5%
C0	0.01µ to 0.1µF	AC coupling	
C1	1p to 33pF	Oscillator element load	NP0 special ceramic capacitor
C2	*	PLL loop filter	Film capacitor
C3	*	PLL loop filter	Ceramic capacitor
C4	Over 1µF	Power supply de-coupling	Electrolytic capacitor
C5	0.1µF	Power supply de-coupling	Ceramic capacitor

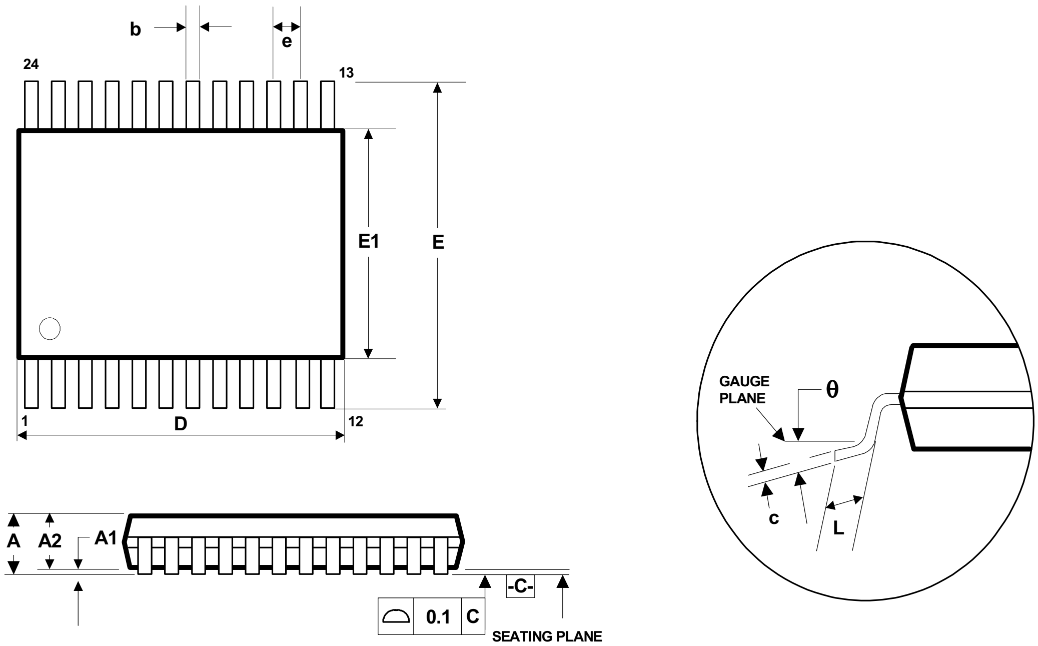
Table 26 Recommended Component Values

Note:

*** Refer Table 4**

PACKAGE DIMENSIONS

DT: 24 PIN TSSOP (6.5 x 6.4 x 1.0 mm) **DM031.B**



Symbols	Dimensions (mm)		
	MIN	**NOM**	**MAX**
A	-----	-----	1.20
A_1	0.03	0.08	0.18
A_2		1.00	
b	0.17	0.22	0.32
c	0.10	0.15	0.25
D	6.4	6.50	6.95
e		0.50 BSC	
E	6.15	6.4 BSC	6.65
E_1	4.30	4.40	4.50
L	0.30	0.50	0.70
θ	0^o	-----	10^o

NOTES:
A. ALL LINEAR DIMENSIONS ARE IN MILLIMETERS.
B. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
C. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSION.

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