PEX 8732 Highlights

- **PEX 8732 Vitals**
  - 32-lane, 8-port PCIe Gen3 switch
    - Integrated 8.0 GT/s SerDes
  - 27 x 27mm^2, 676-ball PBGA package
  - Typical Power: 5.84 Watts

- **PEX 8732 Key Features**
  - **Standards Compliant**
    - PCI Express Base Specification, r3.0 (compatible w/ PCIe r1.0a/1.1/2.0)
    - PCI Power Management Spec, r1.2
    - Microsoft Vista Compliant
    - Supports Access Control Services
    - Dynamic link-width control
    - Dynamic SerDes speed control
  - **High Performance**
    - ♦ ***performance*PAK**
      - ✓ Read Pacing (bandwidth throttling)
      - ✓ Multicast
      - ✓ Dynamic Buffer/FC Credit Pool
    - Non-blocking switch fabric
    - Full line rate on all ports
    - Packet Cut-Thru w/ 132ns max packet latency (x8 to x8)
  - **Flexible Configuration**
    - Ports configurable as x1, x4, x8, x16
    - Registers configurable with strapping pins, EEPROM, I^{2}C, or host software
    - Lane and polarity reversal
    - Compatible with PCIe 1.0a PM
  - **Multi-Host & Fail-Over Support**
    - Configurable Non-Transparent (NT) port
    - Failover with NT port
  - **Quality of Service (QoS)**
    - Eight traffic classes per port
    - Two Virtual Channels (VCs)
    - Weighted round-robin source port arbitration
  - **Reliability, Availability, Serviceability**
    - ♦ ***vision*PAK**
      - ✓ Per Port Performance Monitoring
        - Per port payload & header counters
      - ✓ SerDes Eye Capture
      - ✓ Error Injection and Loopback
    - 3 Hot-Plug Ports with native HP Signals
    - All ports Hot-Plug capable thru I^{2}C (Hot-Plug Controller on every port)
    - ECRC and Poison bit support
    - Data Path parity
    - Memory (RAM) Error Correction
    - INTA# and FATAL_ERR# signals
    - Advanced Error Reporting
    - Port Status bits and GPIO available
      - Per port error diagnostics
    - JTAG AC/DC boundary scan

Application:
Speed Bridge

PLX Products:
PEX8732 – 32-lane, 8-port PCIe Gen3 Switch

Key Benefit:
PCIe Gen 3 (8.0GT/s) speed

Release of PCIe Gen3 specification

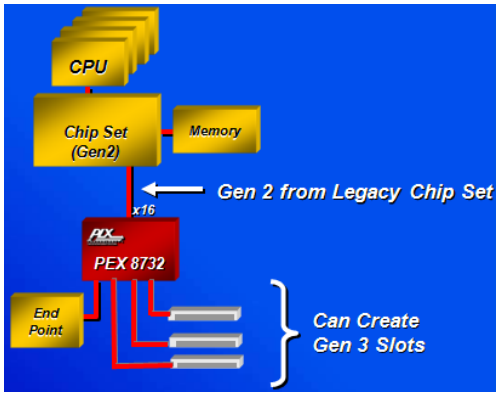
Now that the PCIe Gen3 specification has been finalized, the 8.0Gbps high speed serial interconnect will become common place in all system architecture. This comes as the widely adopted PCIe Gen2 designs continue and ramp into volume production. With the design challenges to overcome moving to the faster bandwidth, Gen3 is still months away from being embraced. However, Gen3 switches can be used to bridge the specification gap. PCIe Gen3 is required to be backwards compatible with existing PCIe implementations (ie. support the Gen2 and Gen1 specifications).

A Gen3 Switch as a Speed Bridge

The simple addition of the ExpressLane™ PEX8732 is the answer. This will allow existing Gen2 host/devices to run at the higher throughput Gen3 speeds when other Gen3 host/devices are available in the same system architecture. It is a fast and seamless way to support the new 8.0Gbps speed.

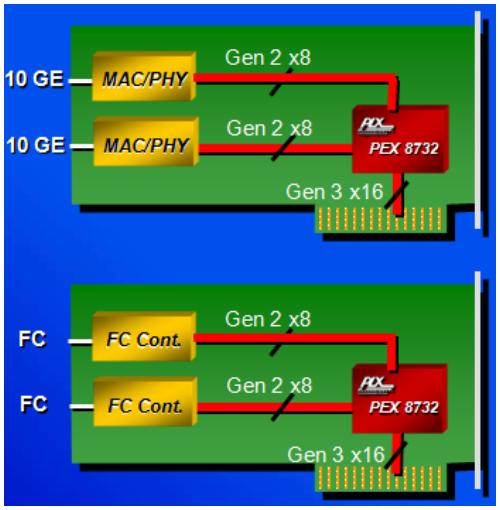
The PEX8732 is a 32-lane, 8-port PCIe Gen3 switch device built on 40nm technology. PEX8732 offers Multi-Host PCI Express switching capability that enables users to connect multiple hosts to their respective endpoints via scalable, high-bandwidth, non-blocking interconnection to a wide variety of applications including servers, storage, communications, and graphics platforms. The PEX8732 is well suited for fan-out, aggregation, and peer-to-peer traffic patterns. This is the perfect solution when supporting PCI Express.

Create Gen3 slots with a Gen2 CPU



With the delays in the Gen3 specification along with the postponed launch of host systems supporting Gen3, there is a way to upgrade existing Gen2 host systems to support the Gen3 endpoints. Especially now that the number of widely available Gen3 endpoint are dawning upon us today. Customers can still use a Gen2 CPU and use the PEX8732 to create Gen3 slots on the motherboard. Therefore, the Gen3 endpoints will be running at the faster 8.0Gbps speed when plugged into a PCIe Gen3 capable slot.

Create Gen3 devices



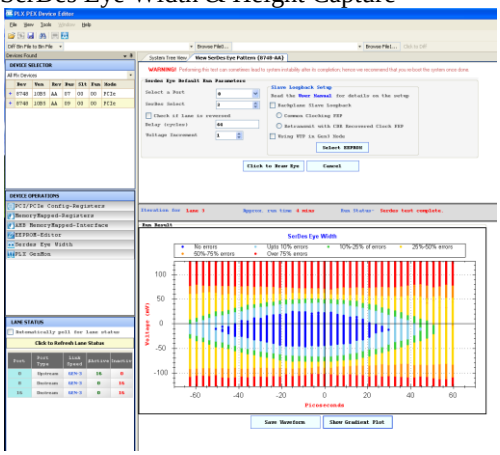
On the contrary, it is no easy task to convert a Gen2 endpoint, such as an Ethernet MAC/PHY or a Fiber Channel controller, over to a PCIe Gen3 native device. It will be a whole new design with endless testing to validate the new Gen3 protocol. However, the PEX8732 can be used once again to solve this dilemma. This quickly allows PCIe endpoints to interface with a Gen3 capable host system by simply designing in the PEX8732 on the add-in card form factor. Vendors can start shipping PCIe Gen3 endpoints today while designers work on a Gen3 solution in the interim.

PLX Gen3 Switches Available Today

PCI-SIG® Base Spec.	Device	Lanes	Ports
r3.0	PEX8748	48	12
r3.0	PEX8747	48	5
r3.0	PEX8732	32	8
r3.0	PEX8724	24	6
r3.0	PEX8716	16	4
r3.0	PEX8712	12	3

Additional PLX Advantages

- *vision*PAK
  - SerDes Eye Width & Height Capture



  - Per Port Performance Monitoring
  - Packet gernation to saturate up to a x16 wide Gen3 port
  - Error Injection in the data path to system behavior
  - Loopback at various stages of the data path
  - Access to internal parallel data path and state-machines
  - View of the PCIe hierarchy of the system
- Integrated Non-Transparent Port
- Spread Spectrum Clock Isolation

Available on PLX Website:

www.plxtech.com/8732

Product Brief, Databook, Application Notes, Technical Support
Hardware (RDK) and Software (SDK) Development Kits, Signal Integrity (SI) Kit, BSDL models, H-Spice models, OrCAD symbols, and more.