Version 1.0 2004

PEX 8111

Features

- General Features
  - Forward and Reverse bridging
  - Tiny 161 ball BGA package (10mm x 10mm)
  - Low power – 0.3 Watts maximum
  - EEPROM configuration option with SPI
  - Internal 8Kbyte shared RAM
  - 1.5 V core supply voltage
  - JTAG
  - Four (4) GPIO pins for maximum design and application flexibility
  - Extensive PME support including D0 and $D0_{Active}$, D1, D2 and $D3_{Hot}$ and $D3_{Cold}$
- Integrated PCI Express Interface
  - PCI Express Base specification 1.0a compliant
  - x1 Link, full-duplex, 2.5 Gbps
  - One virtual channel
  - Automatic LVDS polarity reversal
  - 128 byte maximum payload size
  - Link CRC
  - Link power management
  - Flow control buffering
  - PCI Express transaction queues for eight (8) outstanding TLPs
- PCI Interface
  - PCI 3.0: 32 bits at 33 MHz
  - PCI Power Management 1.1
  - Internal arbiter supports up to 4 external masters; provides REQ#/GNT# signals
  - 3.3V I/O and 5V tolerant PCI
  - Message Signal Interrupt (MSI) support
  - Provides PCI clock output
  - Four mailbox registers for messaging
  - ISA Enable and VGA Enable registers for legacy operation

PLX TECHNOLOGY
THE I/O INTERCONNECT SOLUTION

PCI Express to PCI Bridge

Reversible Bridge in a Tiny Package

The PLX Technology PEX 8111 bridge enables designers to migrate legacy PCI bus interfaces to the new advanced serial PCI Express. This is ideal when including existing PCI ICs on a PCI Express™ Adapter Board, such as the new ExpressCard™ standard. This simple bridge can also reside on either end of a PCI Express cable to connect remote functions running the PCI protocol. The PEX 8111 supports **forward and reverse bridging**. The tiny 10 mm x 10mm Plastic BGA package makes the PEX 8111 bridge ideal for use in applications where board real estate is at a premium. With its low power 0.15 micron CMOS design, the PEX 8111 consumes a maximum power of only 300 mW.

Forward and Reverse Bridging

Compliant to the PCI Express-to-PCI/PCI-X Bridge Specification 1.0, the PEX 8111 is capable of operating in either forward or reverse bridging modes. In forward mode, the bridge allows legacy PCI chips and adapters to be used with new PCI Express processor systems. Reverse bridge operation allows conventional PCI processors and chipsets to configure and control advanced PCI Express switches and endpoints. The reverse PEX 8111 not only allows complete configuration of a downstream PCI Express system from the PCI bus, but it also handles limited PCI Express **root functions** for reverse interrupt and Power Management Events.

Block Diagram

The PEX 8111 is equipped with a standard PCI Express port that operates as a single, x1 link with a maximum of 250 Megabytes per second of throughput per transmit and receive direction. With a single 2.5 Gbps integrated SerDes, the standard PCI Express signaling delivers the highest bandwidth with the lowest possible pin count using LVDS technology.

The PEX 8111 has a single parallel bus segment supporting the PCI v 3.0 protocol. With a 32-bit wide parallel data path running at 33MHz, the PCI bandwidth is 132 Megabytes per second.

While the PCI Express link accommodates the full PCI bus bandwidth, the device also supports internal queues with flow control features to optimize throughput and traffic flow.

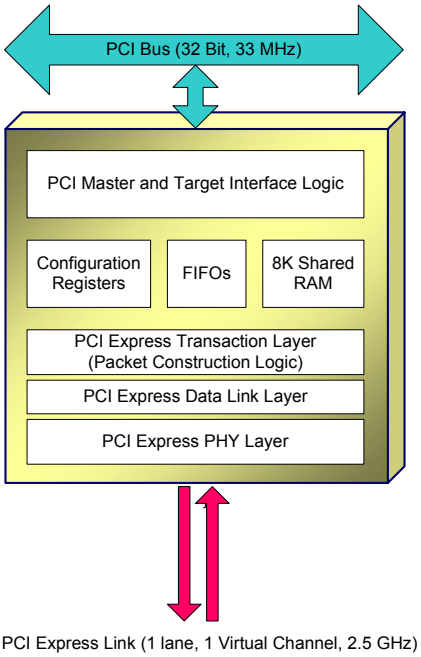

Figure 1. PEX 8111 Block Diagram

Design Applications

ExpressCard™ Adapter – Forward Bridge

The PEX 8111 can be used to quickly upgrade legacy PCI adapter board designs to be compatible with PCI Express standard interface slots. In Figure 2, an existing CardBus™ IC is converted for use on an ExpressCard™ with the addition of the single-chip PEX 8111.

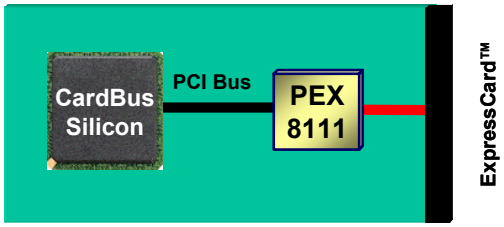

Figure 2. Forward Bridge in ExpressCard™

Embedded Platform – Reverse Bridge

The PEX 8111 supports Reverse bridging, enabling designers to utilize the latest PCI Express silicon with widely entrenched PCI host systems. Reverse bridging allows the host processor to reside out on the PCI bus; the PEX 8111 will accept configuration cycles from the PCI side and manage the local PCI Express interface as a secondary entity within the PCI software model as in Figure 3.

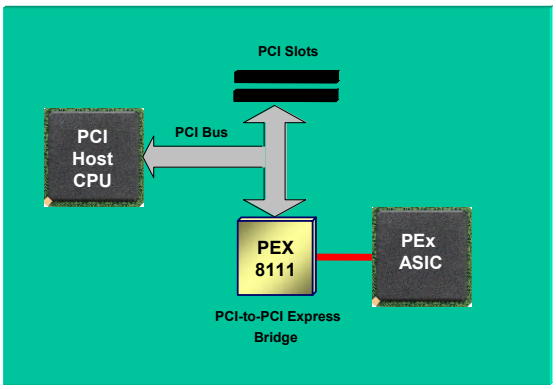

Figure 3. Reverse Bridge with PCI CPU

Standardized PCI Expansion – Forward and Reverse Bridge Modes

The PEX 8111 is the ideal bridge for facilitating remote I/O expansion in computing, communications, or data acquisition applications (see Figure 4). The PCI SIG® PCI Express cabling specification and the PEX 8111 offer a standards-based extender for the parallel PCI bus. Because the PEX 8111 supports reverse bridging operation, the PCI host system is able to configure the PCI Express link.

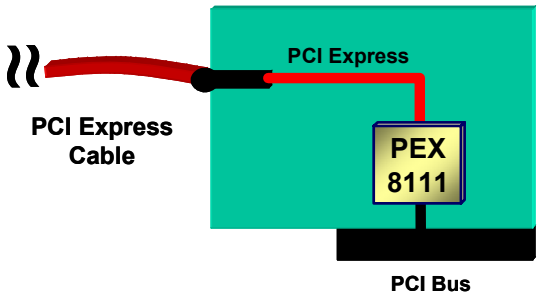

Figure 4. Remote Expansion of PCI-Based Systems

Development Tools

PEX 8111 Reference Design Kits (PEX 8111RDKs) enable rapid customer design. The Forward Bridge RDK hardware module includes the PEX 8111 with a single x1 PCI Express (card-edge) port and single PCI slot on the secondary side. The Reverse Bridge RDK includes a standard PCI edge connector (card-edge) and a standard PCI Express slot on the secondary side. Each PEX 8111RDK can be installed in a motherboard to test and validate customer software and to evaluate PEX 8111 features and benefits.

Product Ordering Information

Part Number	Description
PEX 8111-AA33BC	PCI Express to PCI Bridge
PEX 8111RDK-F	Forward Bridge Reference Design Kit
PEX 8111RDK-R	Reverse Bridge Reference Design Kit

Please visit the PLX Web site at http://www.plxtech.com or contact PLX sales at 408-774-9060 for sampling

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