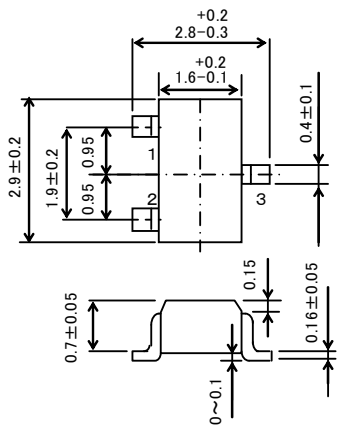
TOSHIBA Field Effect Transistor Silicon P-Channel MOS Type

SSM3J312T

High Speed Switching Applications
Power Management Switch Applications

- 1.8V drive
- Low on-resistance: R_{on} = 237mΩ (max) (@V_{GS} = −1.8 V)
  R_{on} = 142mΩ (max) (@V_{GS} = −2.5 V)
  R_{on} = 91mΩ (max) (@V_{GS} = −4.0 V)

Unit: mm



TSM

1.GATE
2.SOURCE
3.DRAIN

JEDEC	—
JEITA	—
TOSHIBA	2-3S1A

Weight: 10 mg (typ.)

Absolute Maximum Ratings (Ta = 25°C)

Characteristic		Symbol	Rating	Unit
Drain-Source voltage		V_{DS}	−12	V
Gate-Source voltage		V_{GSS}	± 8	V
Drain current	DC	I_D	−2.7	A
	Pulse	I_{DP}	−5.4	
Drain power dissipation		$P_{D\ (Note\ 1)}$	700	mW
Channel temperature		T_{ch}	150	°C
Storage temperature range		T_{stg}	−55~150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Mounted on FR4 board.
(25.4 mm × 25.4 mm × 1.6mm, Cu Pad: 645 mm^2)

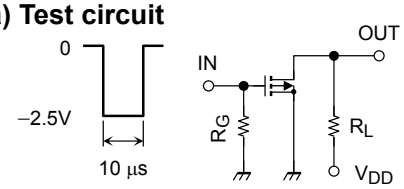
Electrical Characteristics (Ta = 25°C)

Characteristic		Symbol	Test Conditions	Min	Typ.	Max	Unit
Drain-Source breakdown voltage		$V_{(BR)\ DSS}$	I_D = −1 mA, V_{GS} = 0	−12	—	—	V
		$V_{(BR)\ DSX}$	I_D = −1 mA, V_{GS} = +8 V	−4	—	—	
Drain cut-off current		I_{DSS}	V_{DS} = −12 V, V_{GS} = 0	—	—	−10	μA
Gate leakage current		I_{GSS}	V_{GS} = ±8V, V_{DS} = 0	—	—	±1	μA
Gate threshold voltage		V_{th}	V_{DS} = −3 V, I_D = −1 mA	−0.3	—	−1.0	V
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = −3 V, I_D = − 1 A (Note2)	2.7	4.5	—	S
Drain-Source on-resistance		$R_{DS\ (ON)}$	I_D = −1.0 A, V_{GS} = −4.0 V (Note2)	—	69	91	mΩ
			I_D = −0.75 A, V_{GS} = −2.5 V (Note2)	—	97	142	
			I_D = −0.3 A, V_{GS} = −1.8 V (Note2)	—	137	237	
Input capacitance		C_{iss}	V_{DS} = −10 V, V_{GS} = 0, f = 1 MHz	—	550	—	pF
Output capacitance		C_{oss}		—	170	—	
Reverse transfer capacitance		C_{rss}		—	155	—	
Total Gate Charge		Q_g	V_{DS} = −6 V, I_{DS}= −2.7 A V_{GS} = −4 V	—	7.5	—	nC
Gate-Source Charge		Q_{gs}		—	6.0	—	
Gate-Drain Charge		Q_{gd}		—	1.5	—	
Switching time	Turn-on time	t_{on}	V_{DD} = −10 V, I_D = −0.75 A, V_{GS} = 0~−2.5 V, R_G = 4.7 Ω	—	32	—	ns
	Turn-off time	t_{off}		—	37	—	
Drain-Source forward voltage		V_{DSF}	I_D = 2.7A, V_{GS} = 0 V (Note2)	—	0.85	1.2	V

Note2: Pulse test

Switching Time Test Circuit

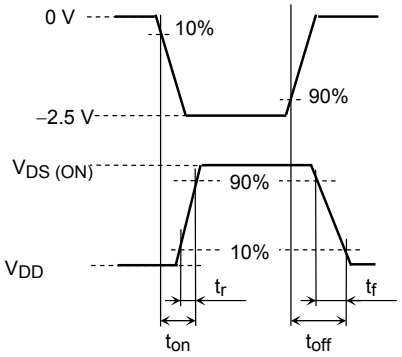
(a) Test circuit



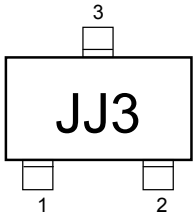
V_{DD} = -10 V
R_G = 4.7 Ω
D.U. ≦ 1%
V_{IN}: t_r, t_f < 5 ns
Common Source
Ta = 25°C

(b) V_{IN}

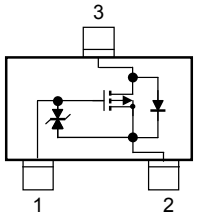
(c) V_{OUT}



Marking



Equivalent Circuit (top view)

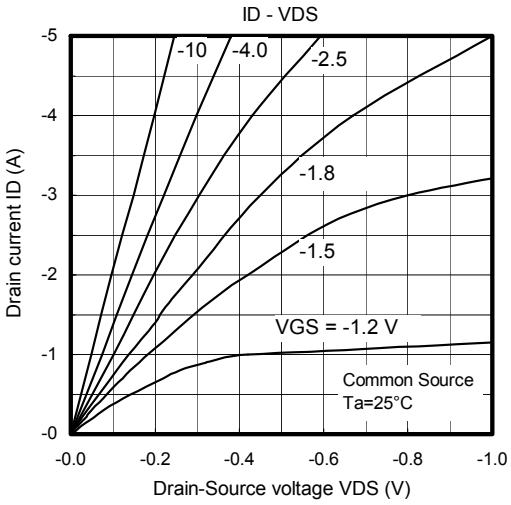


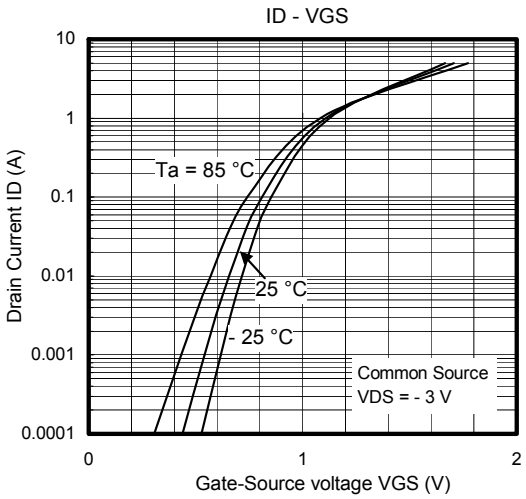
Precaution

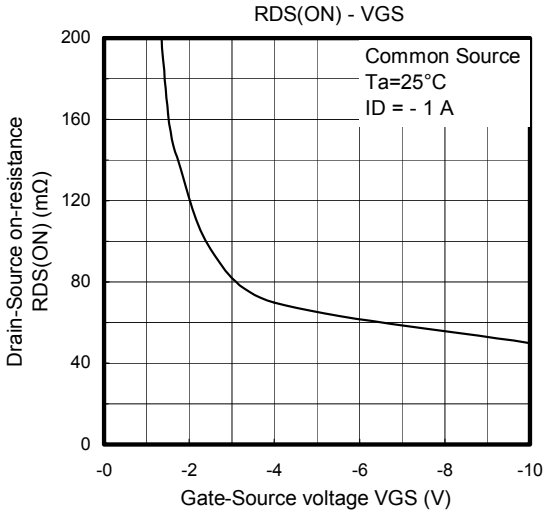
V_{th} can be expressed as the voltage between gate and source when the low operating current value is I_D=−1mA for this product. For normal switching operation, $V_{GS\ (on)}$ requires a higher voltage than V_{th}, and $V_{GS\ (off)}$ requires a lower voltage than V_{th}.
(The relationship can be established as follows: $V_{GS\ (off)} < V_{th} < V_{GS\ (on)}$)
Take this into consideration when using the device.

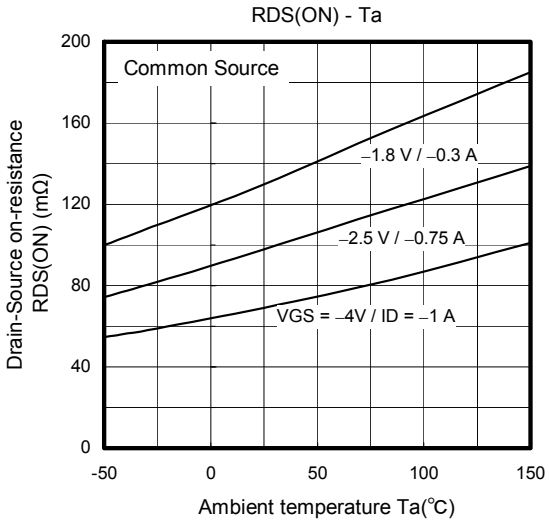
Handling Precaution

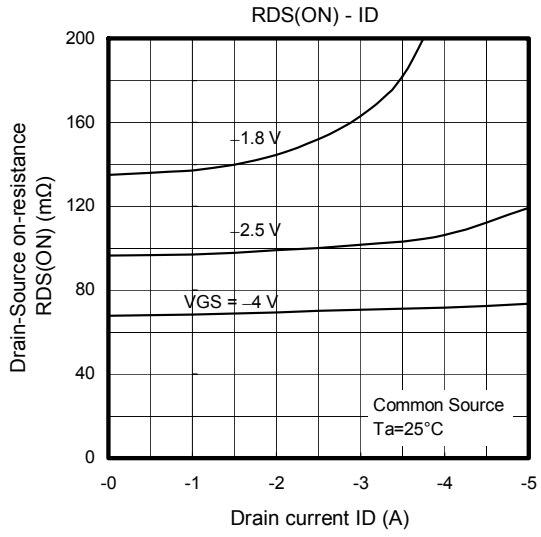
When handling individual devices which are not yet mounted on a circuit board, be sure that the environment is protected against electrostatic discharge. Operators should wear anti-static clothing, and containers and other objects that come into direct contact with devices should be made of anti-static materials.

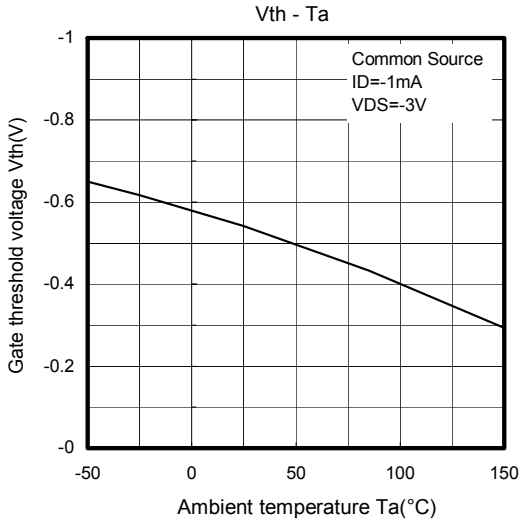


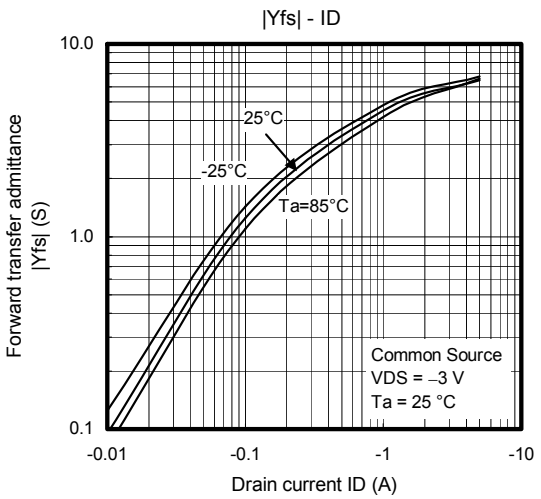


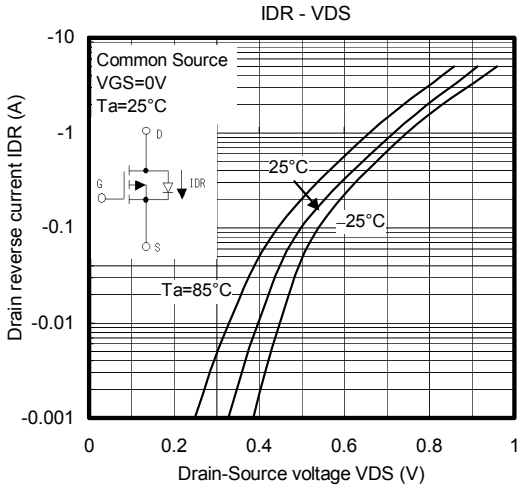


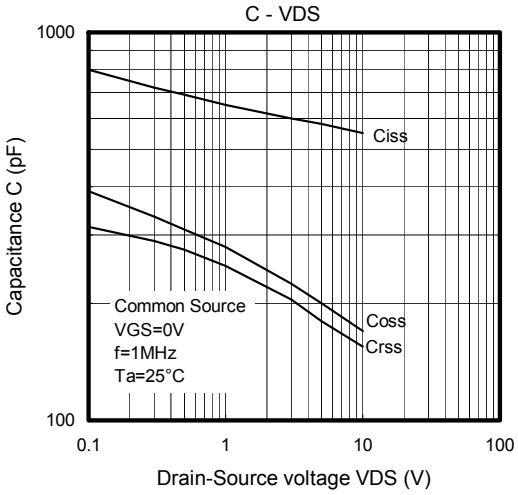


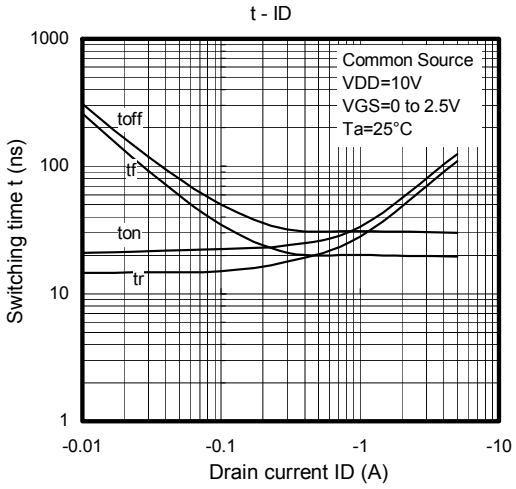


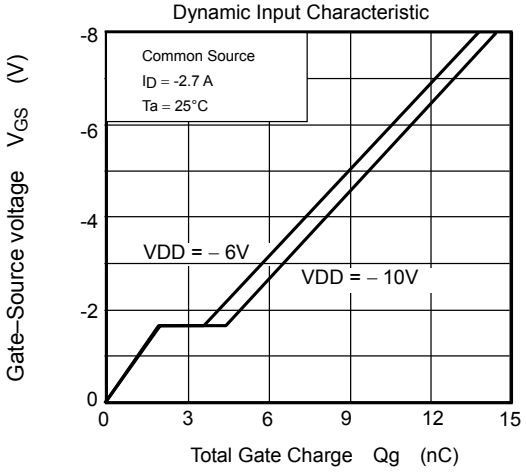


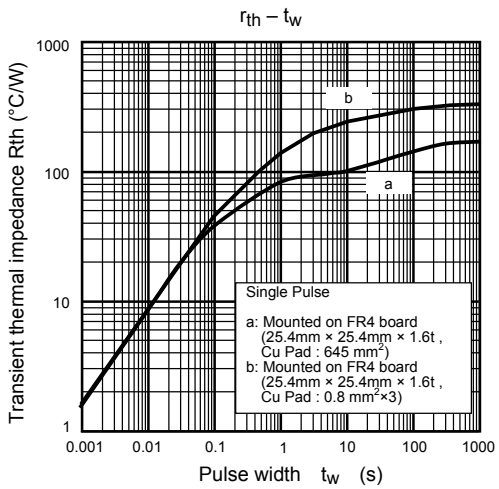


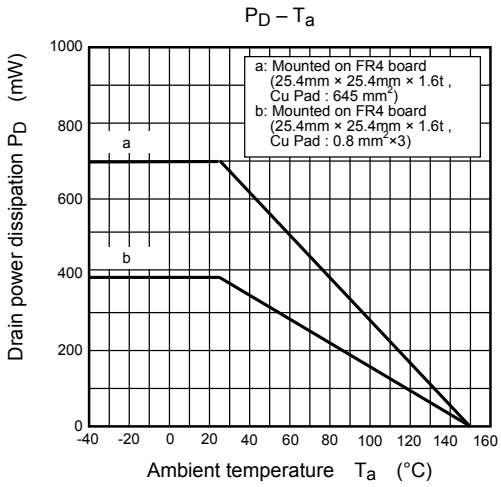












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20070701-EN GENERAL

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