

TOSHIBA Field Effect Transistor Silicon P Channel MOS Type(U-MOS VI)

## SSM6P47NU

### Power Management Switch Applications

- 1.5V drive
- Low ON-resistance:  $R_{DS(on)} = 242 \text{ m}\Omega$  (max) (@ $V_{GS} = -1.5 \text{ V}$ )  
 $R_{DS(on)} = 170 \text{ m}\Omega$  (max) (@ $V_{GS} = -1.8 \text{ V}$ )  
 $R_{DS(on)} = 125 \text{ m}\Omega$  (max) (@ $V_{GS} = -2.5 \text{ V}$ )  
 $R_{DS(on)} = 95 \text{ m}\Omega$  (max) (@ $V_{GS} = -4.5 \text{ V}$ )

### Absolute Maximum Ratings (Ta = 25°C) (Q1, Q2 Common)

Characteristics	Symbol	Rating	Unit
Drain-Source voltage	$V_{DSS}$	-20	V
Gate-Source voltage	$V_{GSS}$	±8	V
Drain current	DC	$I_D$	-4.0
	Pulse	$I_{DP}$ (Note 1)	-8.0
Power dissipation (Note 2)	$P_D$	1	W
	$t < 10\text{s}$	2	
Channel temperature	$T_{ch}$	150	°C
Storage temperature	$T_{stg}$	-55 to 125	°C

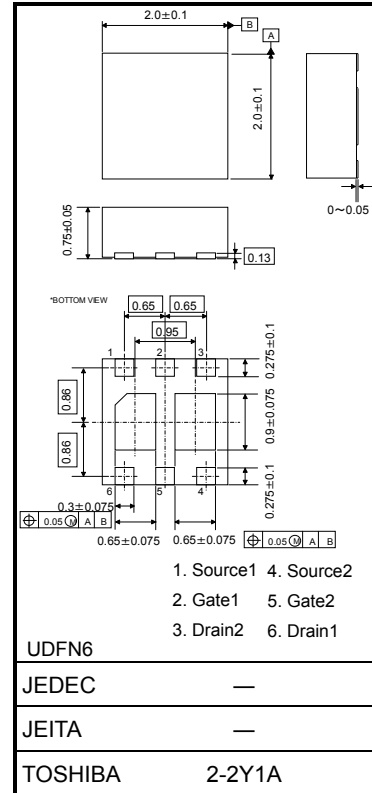
Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: The channel temperature should not exceed 150 °C during use.

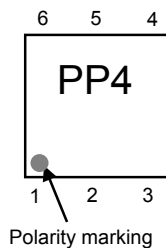
Note 2: Total rating  
 Mounted on an FR4 board.  
 (25.4 mm × 25.4 mm × 1.6 mm, Cu Pad: 645 mm<sup>2</sup>)

Unit: mm

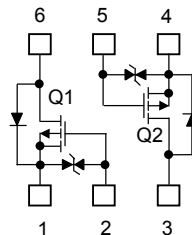


Weight: 8.5 mg (typ.)

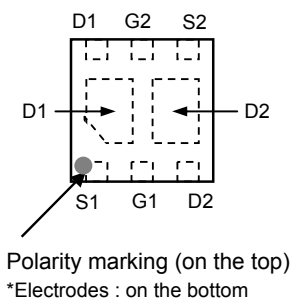
### Marking(Top View)



### Equivalent Circuit(Top View)



### Pin Condition(Top View)



## Electrical Characteristics (Ta = 25°C) (Q1, Q2 Common)

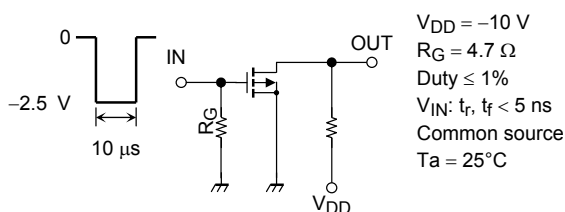
Characteristic	Symbol	Test Conditions	Min	Typ.	Max	Unit
Drain-Source breakdown voltage	V (BR) DSS	I <sub>D</sub> = -1 mA, V <sub>GS</sub> = 0 V	-20	—	—	V
	V (BR) DSX	I <sub>D</sub> = -1 mA, V <sub>GS</sub> = 5 V (Note 4)	-15	—	—	
Drain cut-off current	I <sub>DSS</sub>	V <sub>DS</sub> = -20 V, V <sub>GS</sub> = 0 V	—	—	-1	μA
Gate leakage current	I <sub>GSS</sub>	V <sub>GS</sub> = ±8 V, V <sub>DS</sub> = 0 V	—	—	±1	μA
Gate threshold voltage	V <sub>th</sub>	V <sub>DS</sub> = -3 V, I <sub>D</sub> = -1 mA	-0.3	—	-1.0	V
Forward transfer admittance	Y <sub>fs</sub>	V <sub>DS</sub> = -3 V, I <sub>D</sub> = -1.0 A (Note 3)	2.8	5.6	—	S
Drain-source ON-resistance	R <sub>DS (ON)</sub>	I <sub>D</sub> = -1.5 A, V <sub>GS</sub> = -4.5 V (Note 3)	—	80.5	95	mΩ
		I <sub>D</sub> = -1.0 A, V <sub>GS</sub> = -2.5 V (Note 3)	—	99.5	125	
		I <sub>D</sub> = -0.5 A, V <sub>GS</sub> = -1.8 V (Note 3)	—	122	170	
		I <sub>D</sub> = -0.25 A, V <sub>GS</sub> = -1.5 V (Note 3)	—	143	242	
Input capacitance	C <sub>iSS</sub>	V <sub>DS</sub> = -10 V, V <sub>GS</sub> = 0 V, f = 1 MHz	—	290	—	pF
Output capacitance	C <sub>oSS</sub>		—	44	—	
Reverse transfer capacitance	C <sub>rSS</sub>		—	32	—	
Total Gate Charge	Q <sub>g</sub>	V <sub>DD</sub> = -10 V, I <sub>D</sub> = -3.5 A V <sub>GS</sub> = -4.5 V	—	4.6	—	nC
Gate-Source Charge	Q <sub>gs1</sub>		—	0.5	—	
Gate-Drain Charge	Q <sub>gd</sub>		—	1.2	—	
Switching time	Turn-on time	t <sub>on</sub>	V <sub>DD</sub> = -10 V, I <sub>D</sub> = -0.5 A, V <sub>GS</sub> = 0 to -2.5 V, R <sub>G</sub> = 4.7 Ω	—	12.0	ns
	Turn-off time	t <sub>off</sub>		—	46.2	
Drain-Source forward voltage	V <sub>DSF</sub>	I <sub>D</sub> = 4.0 A, V <sub>GS</sub> = 0 V (Note 3)	—	0.9	1.2	V

Note 3: Pulse test

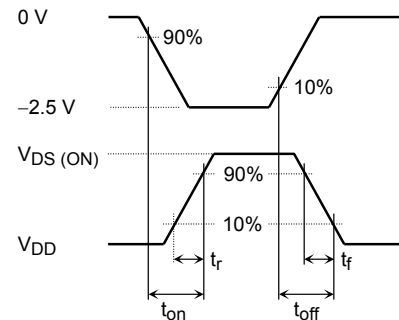
Note 4: If a forward bias is applied between gate and source, this device enters V(BR)DSX mode. Note that the drain-source breakdown voltage is lowered in this mode.

## Switching Time Test Circuit

(a) Test circuit



(b) V<sub>IN</sub>



(c) V<sub>OUT</sub>

## Notice on Usage

Let  $V_{th}$  be the voltage applied between gate and source that causes the drain current ( $I_D$ ) to be low (-1 mA for the SSM6P47NU). Then, for normal switching operation,  $V_{GS(on)}$  must be higher than  $V_{th}$ , and  $V_{GS(off)}$  must be lower than  $V_{th}$ . This relationship can be expressed as:  $V_{GS(off)} < V_{th} < V_{GS(on)}$ .

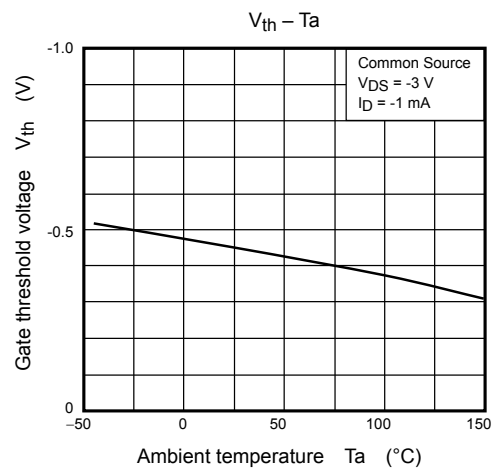
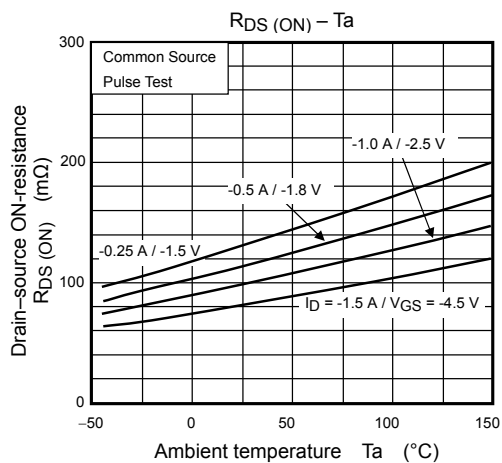
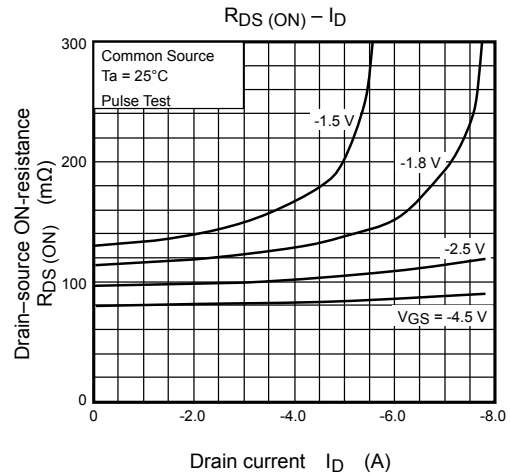
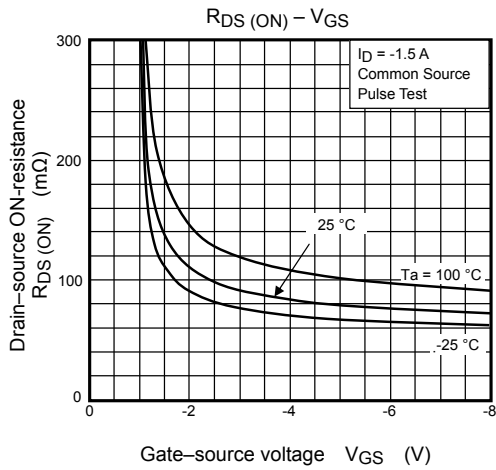
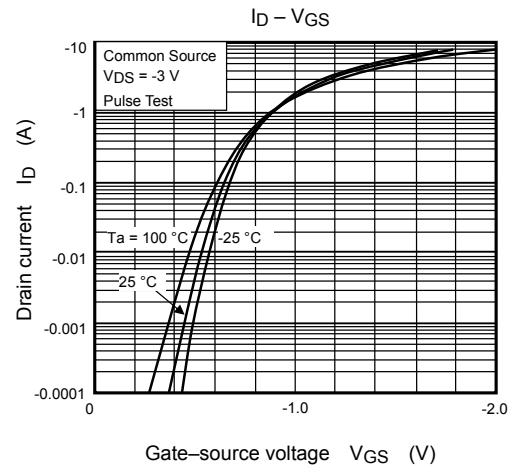
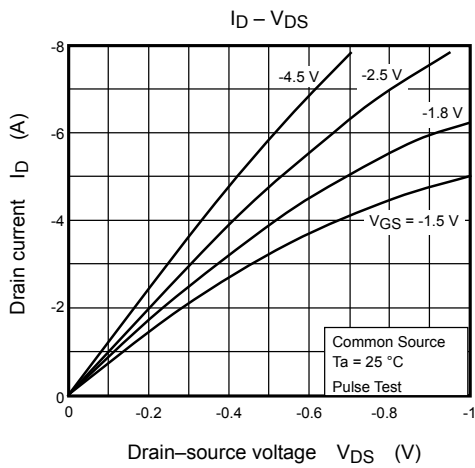
Take this into consideration when using the device.

## Handling Precaution

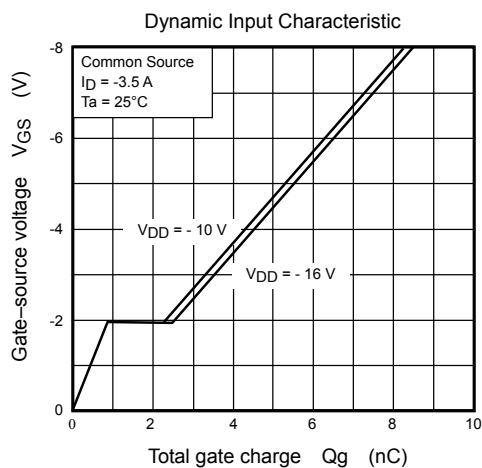
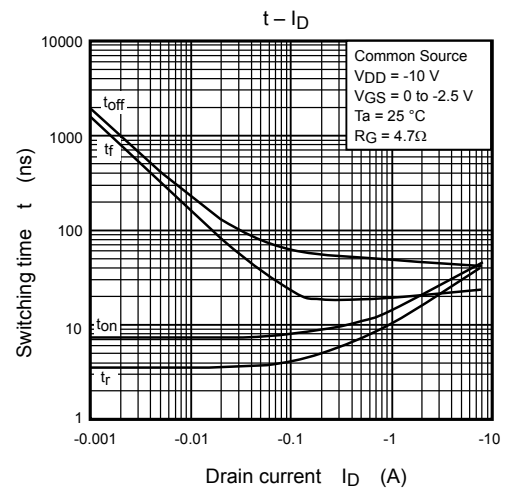
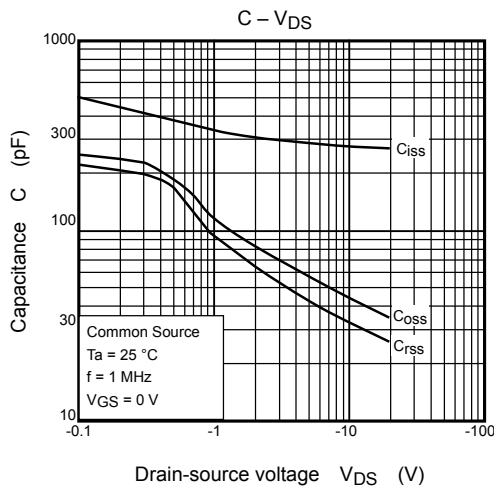
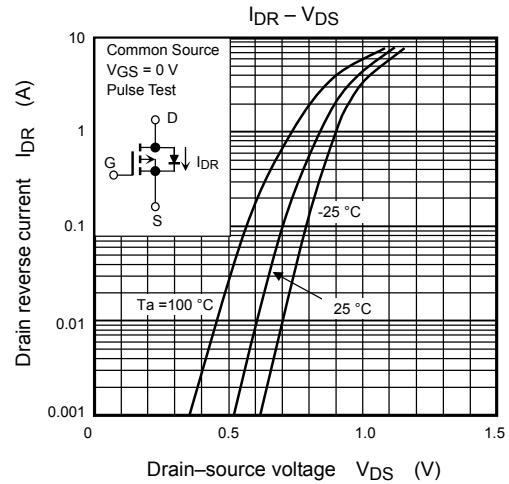
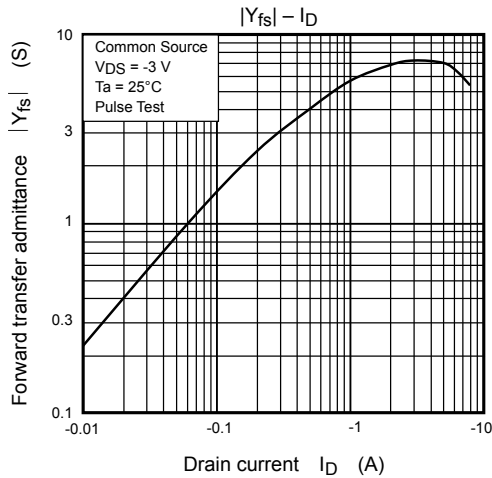
When handling individual devices that are not yet mounted on a circuit board, make sure that the environment is protected against electrostatic discharge. Operators should wear antistatic clothing, and containers and other objects that come into direct contact with devices should be made of antistatic materials.

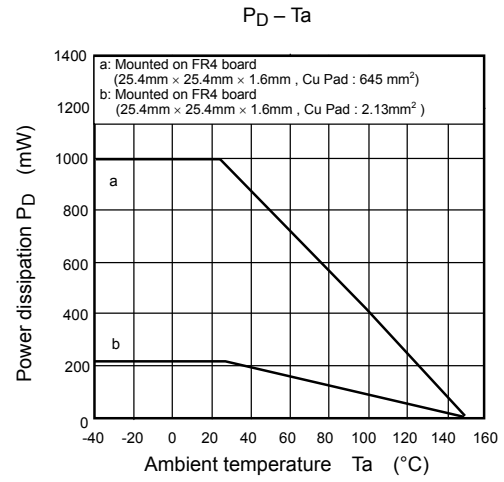
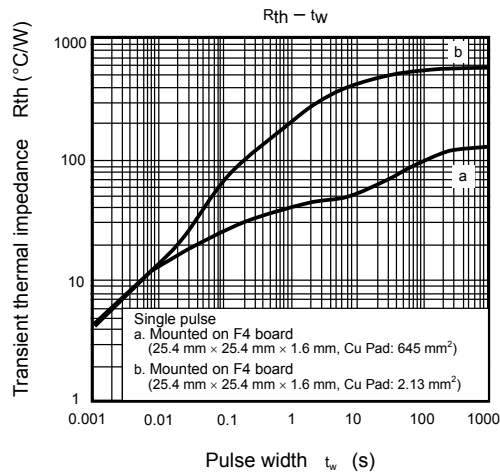
Thermal resistance  $R_{th(ch-a)}$  and power dissipation  $P_D$  vary depending on board material, board area, board thickness and pad area. When using this device, please take heat dissipation into consideration

(Q1, Q2 Common)



(Q1, Q2 Common)





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