Dual P-Channel 12-V (D-S) MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
–12	0.037 @ V_{GS} = –4.5 V	–7.7
	0.048 @ V_{GS} = –2.5 V	–6.8
	0.068 @ V_{GS} = –1.8 V	–5.7

FEATURES

- TrenchFET® Power MOSFETS: 1.8-V Rated
- New Low Thermal Resistance PowerPAK® Package
- Advanced High Cell Density Process
- Ultra-Low $r_{DS(on)}$, and High P_D Capability

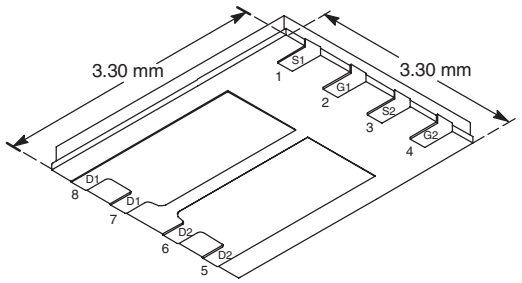
Pb-free Available

RoHS* COMPLIANT

APPLICATIONS

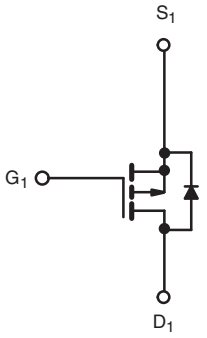
- Load Switch
- PA Switch
- Battery Switch
- Bi-Directional Switch

PowerPAK 1212-8

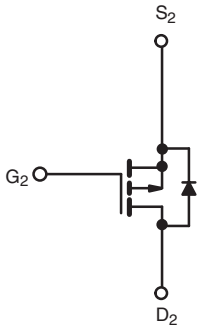


Bottom View

Ordering Information: Si7909DN-T1
Si7909DN–T1–E3 (Lead (Pb)–free)



P-Channel MOSFET



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T_A = 25°C, unless otherwise noted					
Parameter		Symbol	10 secs	Steady State	Unit
Drain-Source Voltage		V_{DS}	–12		V
Gate-Source Voltage		V_{GS}	±8		
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	–7.7	–5.3	A
	T_A = 85°C		–5.5	–3.8	
Pulsed Drain Current		I_{DM}	–20		
Continuous Source Current (Diode Conduction)[a]		I_S	–2.3	–1.1	
Maximum Power Dissipation[a]	T_A = 25°C	P_D	2.8	1.3	W
	T_A = 85°C		1.5	0.85	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150		°C
Soldering Recommendations (Peak Temperature)[b,c]			260		

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient[a]	t ≤ 10 sec	R_{thJA}	35	44	°C/W
	Steady State		75	94	
Maximum Junction-to-Case	Steady State	R_{thJC}	4	5	

Notes
a. Surface Mounted on 1" x 1" FR4 Board.
b. See Solder Profile (*http://www.vishay.com/ppg?73257*). The PowerPAK 1212-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
c. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

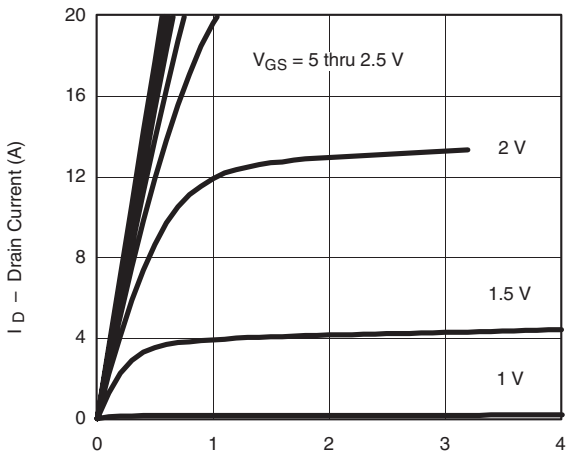
* Pb containing terminations are not RoHS compliant, exemptions may apply

SPECIFICATIONS T_J = 25°C, unless otherwise noted						
Parameter	**Symbol**	**Test Condition**	**Min**	**Typ**	**Max**	**Unit**
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = –700 µA	–0.40		–1.0	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±8 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = –12 V, V_{GS} = 0 V			–1	µA
		V_{DS} = –12 V, V_{GS} = 0 V, T_J = 85°C			–5	
On-State Drain Current[a]	$I_{D(on)}$	$V_{DS} \leq$ –5 V, V_{GS} = –4.5 V	–20			A
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = –4.5 V, I_D = –7.7 A		0.031	0.037	Ω
		V_{GS} = –2.5 V, I_D = –6.8 A		0.040	0.048	
		V_{GS} = –1.8 V, I_D = –3.0 A		0.057	0.068	
Forward Transconductance[a]	g_{fs}	V_{DS} = –6 V, I_D = –7.7 A		17		S
Diode Forward Voltage[a]	V_{SD}	I_S = –2.3 A, V_{GS} = 0 V		–0.7	–1.2	V
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = –6 V, V_{GS} = –4.5 V, I_D = –7.7 A		15.5	24	nC
Gate-Source Charge	Q_{gs}			2.5		
Gate-Drain Charge	Q_{gd}			4.3		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = –6 V, R_L = 6 Ω $I_D \cong$ –1 A, V_{GEN} = –4.5 V, R_G = 6 Ω		25	40	ns
Rise Time	t_r			45	70	
Turn-Off DelayTime	$t_{d(off)}$			90	135	
Fall Time	t_f			85	130	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = –2.3 A, di/dt = 100 A/µs		70	110	

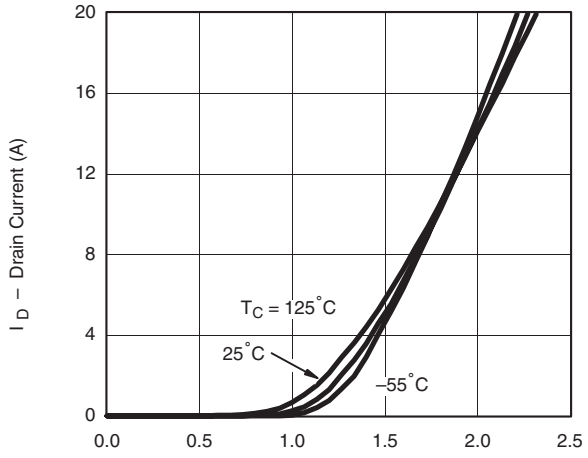
Notes
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS T_A = 25°C, unless otherwise noted

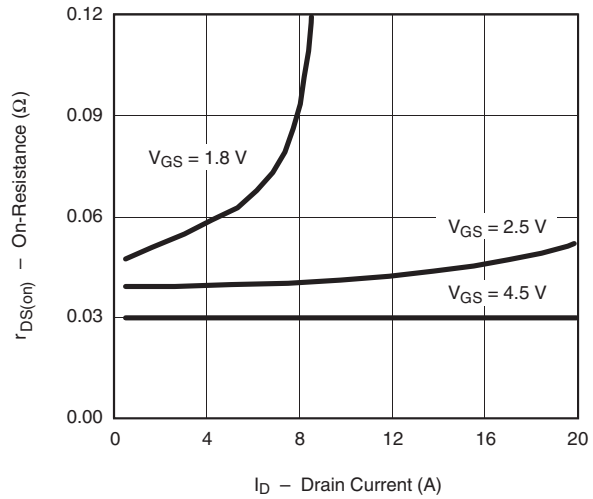


Output Characteristics

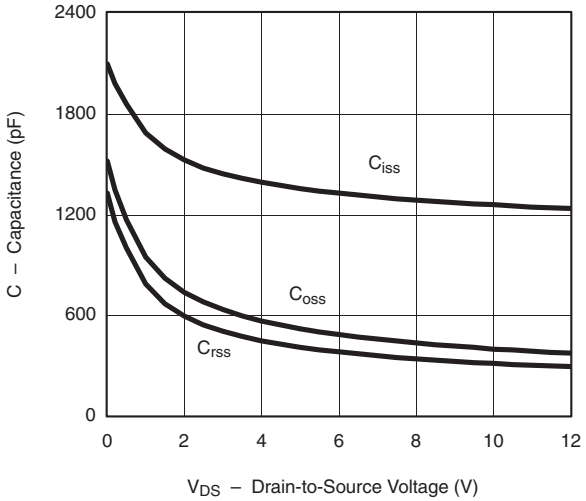


Transfer Characteristics

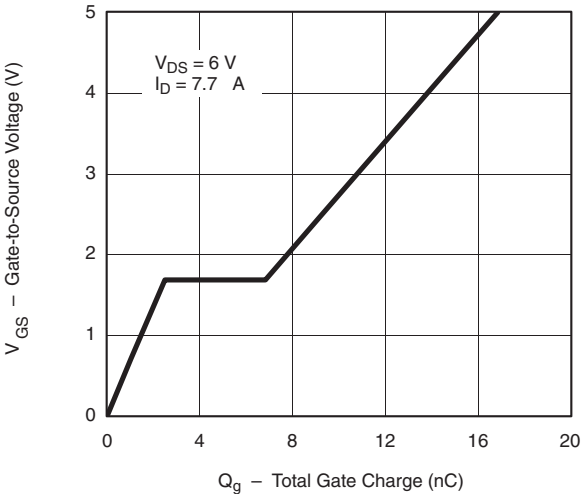
TYPICAL CHARACTERISTICS T_A = 25°C, unless otherwise noted



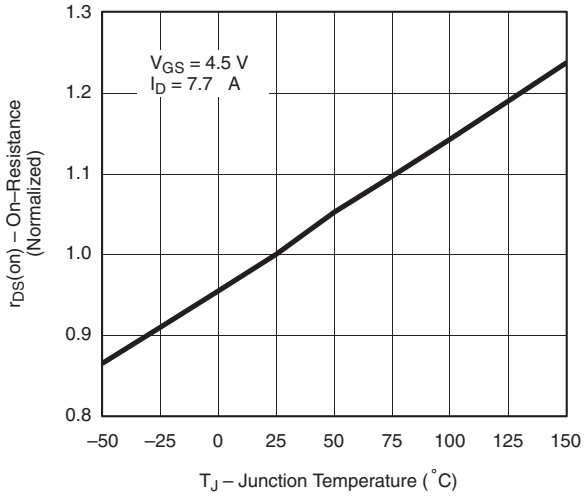
On-Resistance vs. Drain Current



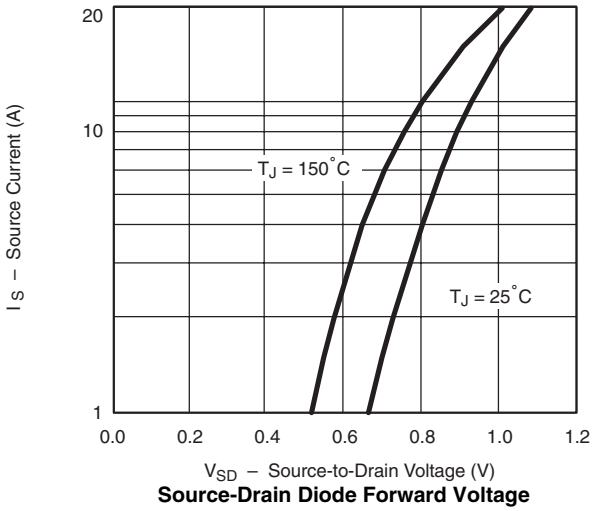
Capacitance



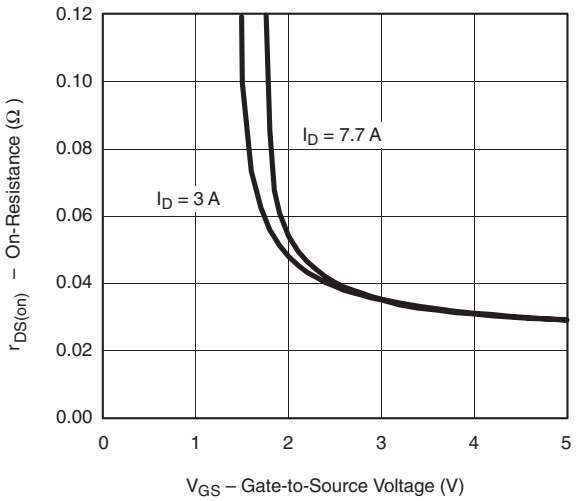
Gate Charge



On-Resistance vs. Junction Temperature

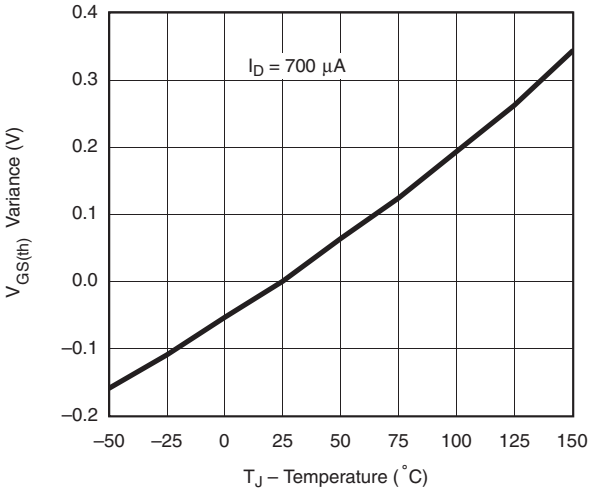


Source-Drain Diode Forward Voltage

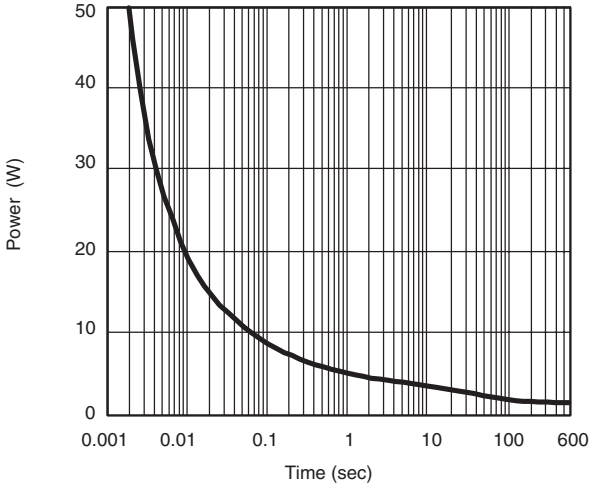


On-Resistance vs. Gate-to-Source Voltage

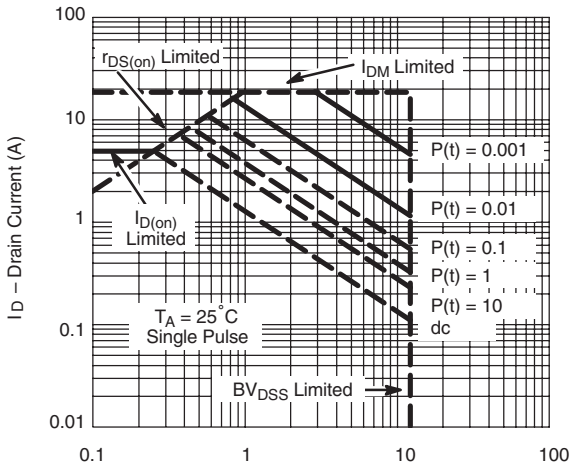
TYPICAL CHARACTERISTICS T_A = 25°C, unless otherwise noted



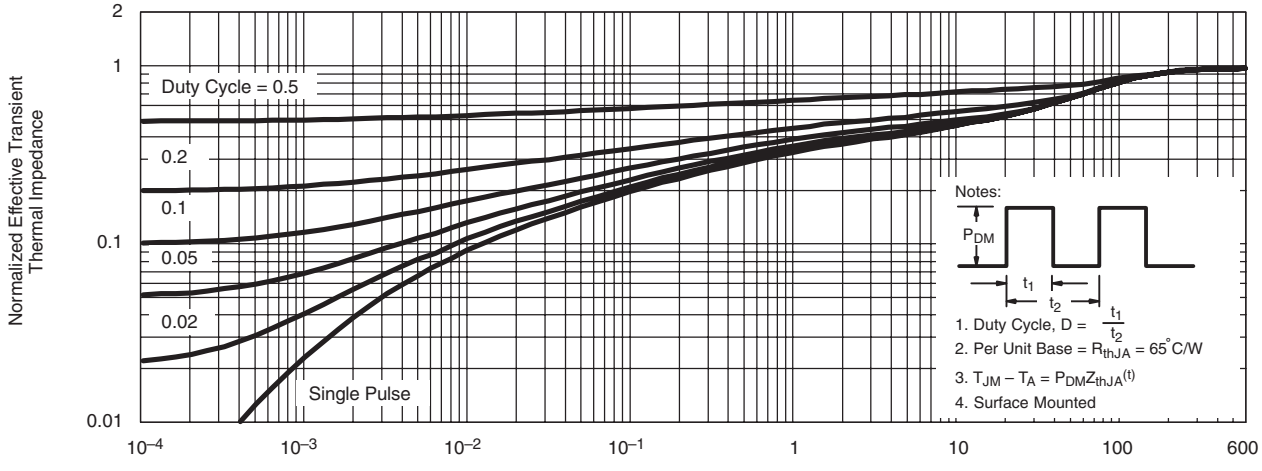
Threshold Voltage



Single Pulse Power, Juncion-To-Ambient

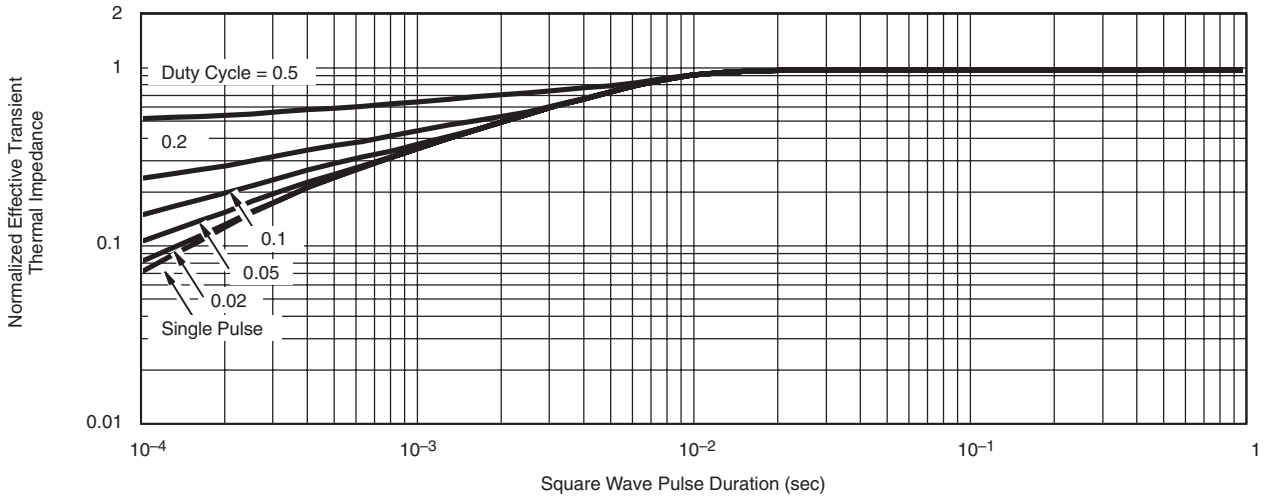


Safe Operating Area, Junction-To-Ambient



Normalized Thermal Transient Impedance, Junction-to-Ambient

TYPICAL CHARACTERISTICS $T_A = 25°C$, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see http://www.vishay.com/ppg?71996.