

Product Summary

Device	$V_{(BR)DSS}$	$R_{DS(ON)}$ max	I_D max $T_A = 25^\circ\text{C}$
Q1	30V	21m Ω @ $V_{GS} = 10\text{V}$	9.4A
		32m Ω @ $V_{GS} = 4.5\text{V}$	7.3A
Q2	-30V	39m Ω @ $V_{GS} = -10\text{V}$	-6.8A
		53m Ω @ $V_{GS} = -4.5\text{V}$	-5.8A

Features and Benefits

- Low On-Resistance
- Low Input Capacitance
- Fast Switching Speed
- **Lead Free By Design/RoHS Compliant (Note 1)**
- **"Green" Device (Note 2)**
- **Qualified to AEC-Q101 standards for High Reliability**

Description and Applications

This MOSFET has been designed to minimize the on-state resistance ($R_{DS(on)}$) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

- Motor control
- Power Management Functions
- DC-DC Converters
- Backlighting

Mechanical Data

- Case: TO252-4L
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections Indicator: See diagram
- Terminals: Finish — NiPdAu over Copper leadframe. Solderable per MIL-STD-202, Method 208
- Weight: 0.027 grams (approximate)



Ordering Information (Note 3)

Part Number	Case	Packaging
DMC3021LK4-13	TO252-4L	2500/Tape & Reel

- Notes:
1. No purposefully added lead.
 2. Diodes Inc.'s "Green" policy can be found on our website at <http://www.diodes.com>.
 3. For packaging details, go to our website at <http://www.diodes.com>.

Marking Information



J; ; = Manufacturer's Marking
 C3021L = Product Type Marking Code
 YYWW = Date Code Marking
 YY = Year (ex: 09 = 2009)
 WW = Week (01 – 53)

Thermal Characteristics @ $T_A = 25^\circ\text{C}$ unless otherwise specified

Characteristic	Symbol	Value	Units
Total Power Dissipation (Note 4)	P_D	2.75	W
Thermal Resistance, Junction to Ambient (Note 4)	$R_{\theta JA}$	46.3	$^\circ\text{C/W}$
Total Power Dissipation (Note 5)	P_D	1.52	W
Thermal Resistance, Junction to Ambient (Note 5)	$R_{\theta JA}$	81.3	$^\circ\text{C/W}$
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +150	$^\circ\text{C}$

Maximum Ratings N-CHANNEL – Q1 @ $T_A = 25^\circ\text{C}$ unless otherwise specified

Characteristic	Symbol	Value	Units	
Drain-Source Voltage	V_{DSS}	30	V	
Gate-Source Voltage	V_{GSS}	± 20	V	
Continuous Drain Current (Note 4) $V_{GS} = 10\text{V}$	Steady State	$T_A = 25^\circ\text{C}$	9.4	A
		$T_A = 70^\circ\text{C}$	7.5	
Continuous Drain Current (Note 5) $V_{GS} = 10\text{V}$	Steady State	$T_A = 25^\circ\text{C}$	6.7	A
		$T_A = 70^\circ\text{C}$	5.4	
Continuous Drain Current (Note 4) $V_{GS} = 4.5\text{V}$	Steady State	$T_A = 25^\circ\text{C}$	7.3	A
		$T_A = 70^\circ\text{C}$	5.8	
Pulsed Drain Current (Note 6)	I_{DM}	40	A	

Maximum Ratings P-CHANNEL – Q2 @ $T_A = 25^\circ\text{C}$ unless otherwise specified

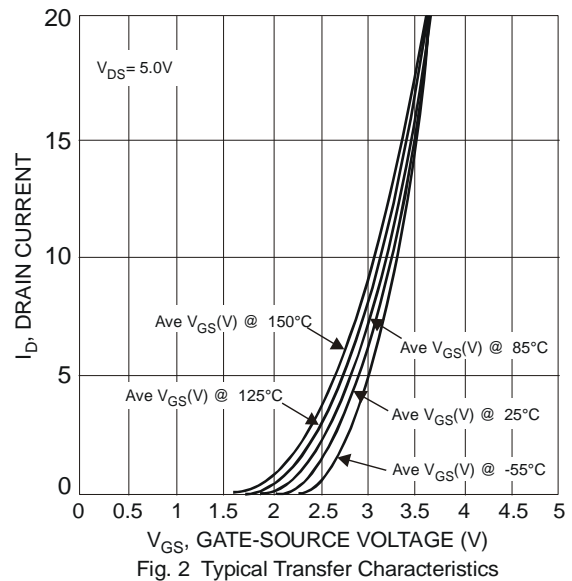
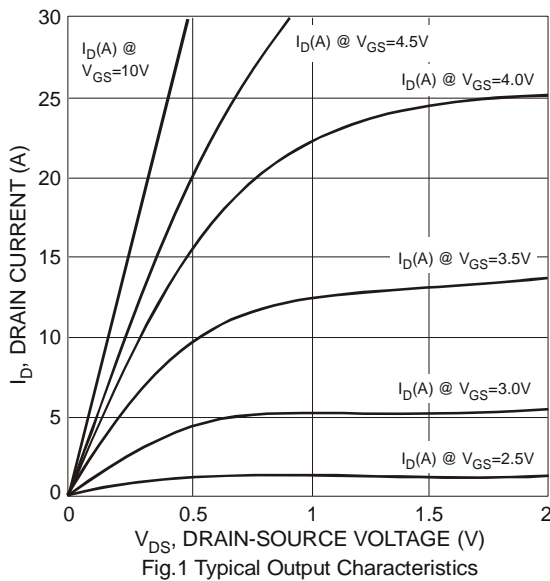
Characteristic	Symbol	Value	Units	
Drain-Source Voltage	V_{DSS}	-30	V	
Gate-Source Voltage	V_{GSS}	± 20	V	
Continuous Drain Current (Note 4) $V_{GS} = -10\text{V}$	Steady State	$T_A = 25^\circ\text{C}$	-6.8	A
		$T_A = 70^\circ\text{C}$	-5.3	
Continuous Drain Current (Note 5) $V_{GS} = -10\text{V}$	Steady State	$T_A = 25^\circ\text{C}$	-5.1	A
		$T_A = 70^\circ\text{C}$	-4.1	
Continuous Drain Current (Note 4) $V_{GS} = -4.5\text{V}$	Steady State	$T_A = 25^\circ\text{C}$	-5.8	A
		$T_A = 70^\circ\text{C}$	-4.6	
Pulsed Drain Current (Note 6)	I_{DM}	-40	A	

- Notes:
- Device mounted on FR-4 substrate PC board, 2oz copper, on 1inch square copper plate.
 - Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout
 - Device mounted on minimum recommended pad layout test board, 10 μs pulse duty cycle = 1%.

Electrical Characteristics N-CHANNEL – Q1 @ $T_A = 25^\circ\text{C}$ unless otherwise specified

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV_{DSS}	30	-	-	V	$V_{GS} = 0V, I_D = 250\mu A$
Zero Gate Voltage Drain Current @ $T_c = 25^\circ\text{C}$	I_{DSS}	-	-	1.0	μA	$V_{DS} = 30V, V_{GS} = 0V$
Gate-Source Leakage	I_{GSS}	-	-	± 100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	$V_{GS(th)}$	1	1.5	2.1	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
Static Drain-Source On-Resistance	$R_{DS(on)}$	-	14	21	m Ω	$V_{GS} = 10V, I_D = 7A$
		-	18	32		$V_{GS} = 4.5V, I_D = 5.6A$
Forward Transfer Admittance	$ Y_{fs} $	-	8.5	-	S	$V_{DS} = 5V, I_D = 7A$
Diode Forward Voltage (Note 6)	V_{SD}	-	0.7	1.0	V	$V_{GS} = 0V, I_S = 1A$
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C_{iss}	-	751	-	pF	$V_{DS} = 10V, V_{GS} = 0V, f = 1.0\text{MHz}$
Output Capacitance	C_{oss}	-	121	-	pF	
Reverse Transfer Capacitance	C_{rss}	-	110	-	pF	
Gate Resistance	R_g	-	1.5	-	Ω	$V_{DS} = 10V, V_{GS} = 0V, f = 1.0\text{MHz}$
Total Gate Charge (4.5V)	Q_g	-	9	-	nC	$V_{GS} = 10V, V_{DS} = 15V, I_D = 6A$
Total Gate Charge (10V)	Q_g	-	17.4	-	nC	
Gate-Source Charge	Q_{gs}	-	2.2	-	nC	
Gate-Drain Charge	Q_{gd}	-	3	-	nC	
Turn-On Delay Time	$t_{D(on)}$	-	2.5	-	ns	$V_{DD} = 15V, V_{GS} = 10V, R_G = 6\Omega, R_L = 1.8\Omega, I_D = 6.7A$
Turn-On Rise Time	t_r	-	6.6	-	ns	
Turn-Off Delay Time	$t_{D(off)}$	-	19.0	-	ns	
Turn-Off Fall Time	t_f	-	6.3	-	ns	

Notes: 7. Short duration pulse test used to minimize self-heating effect.
8. Guaranteed by design. Not subject to product testing.



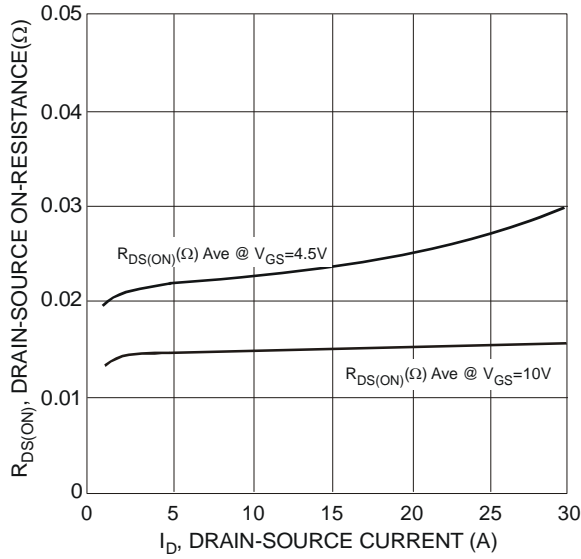


Fig. 3 Typical On-Resistance vs. Drain Current and Gate Voltage

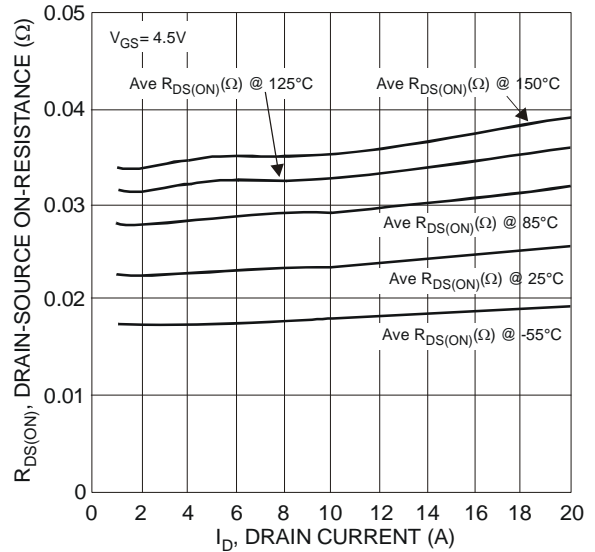


Fig. 4 Typical On-Resistance vs. Drain Current and Temperature

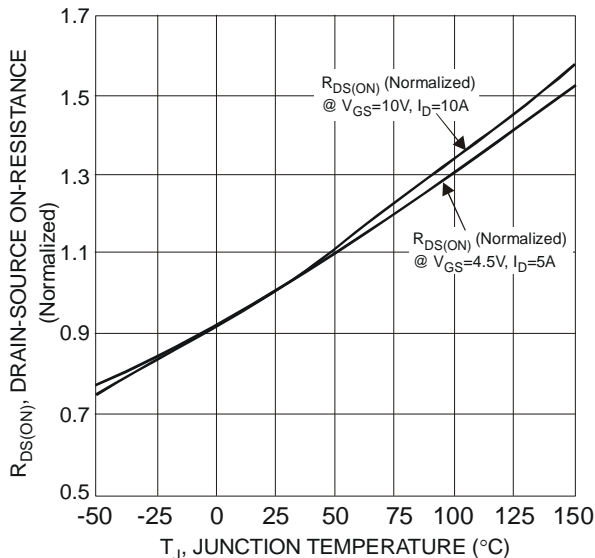


Fig. 5 On-Resistance Variation with Temperature

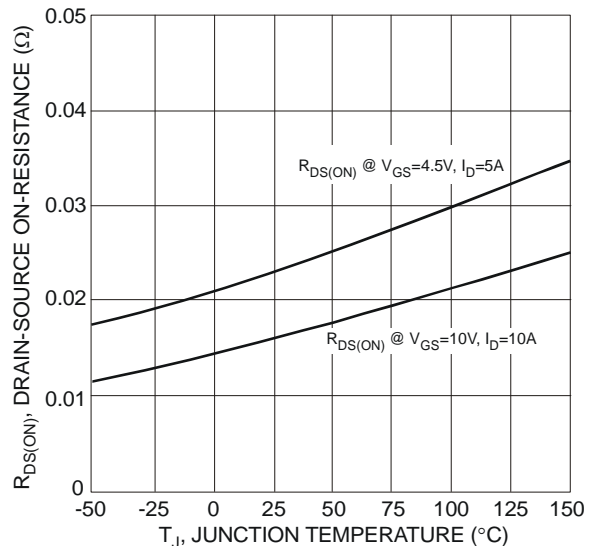


Fig. 6 On-Resistance Variation with Temperature

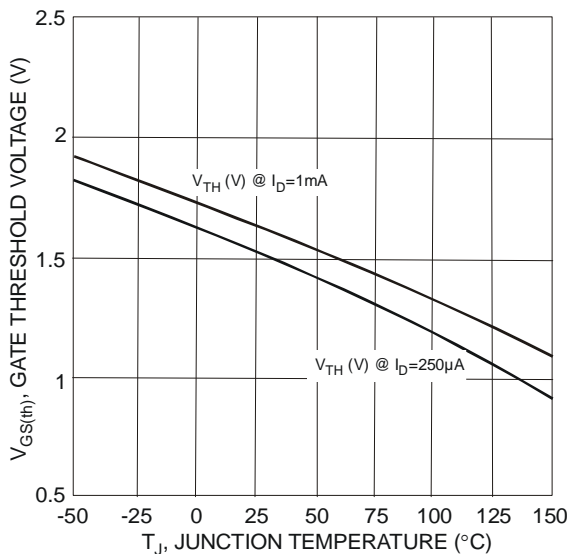


Fig. 7 On-Resistance Variation with Temperature

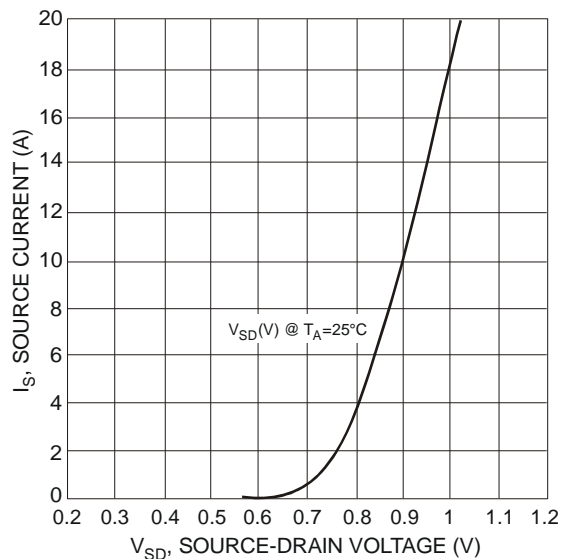


Fig. 8 Diode Forward Voltage vs. Current

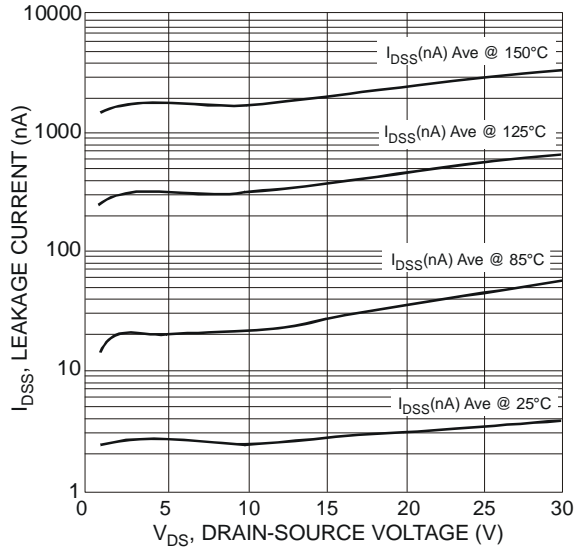


Fig. 9 Typical Drain-Source Leakage Current vs. Voltage

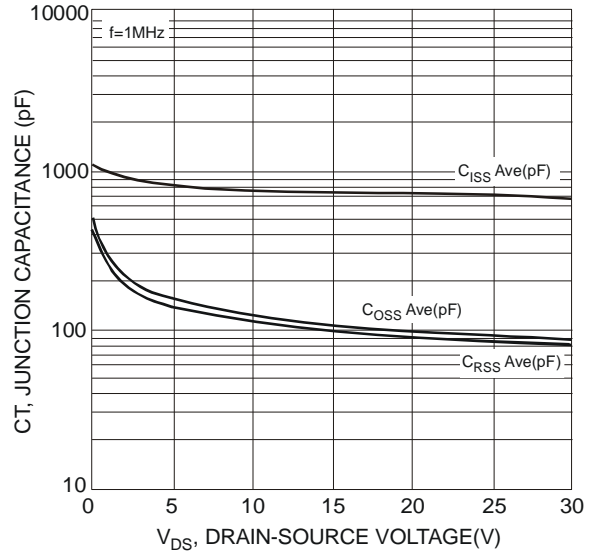


Fig. 10 Typical Junction Capacitance

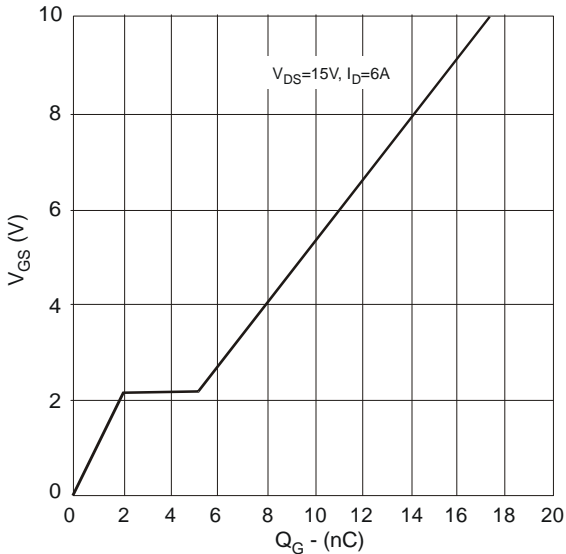


Fig. 11 Gate Charge Characteristics

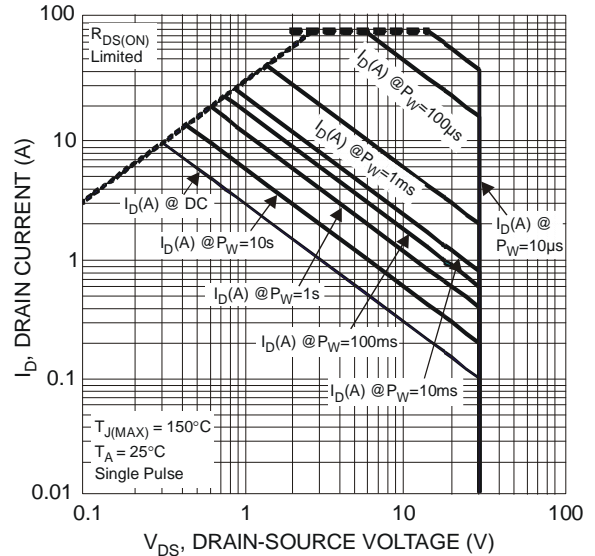
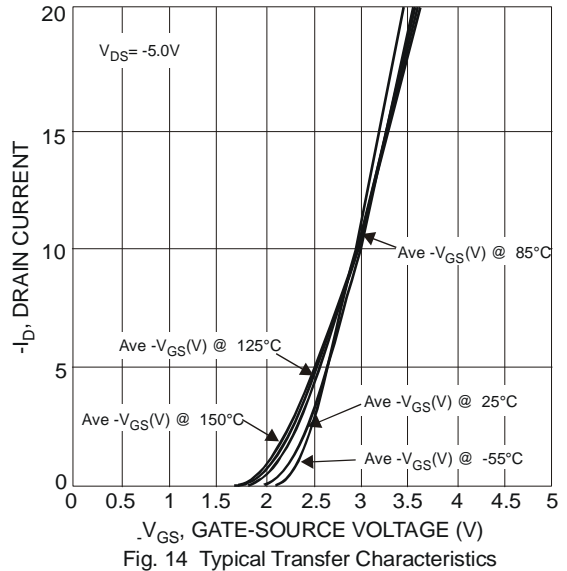
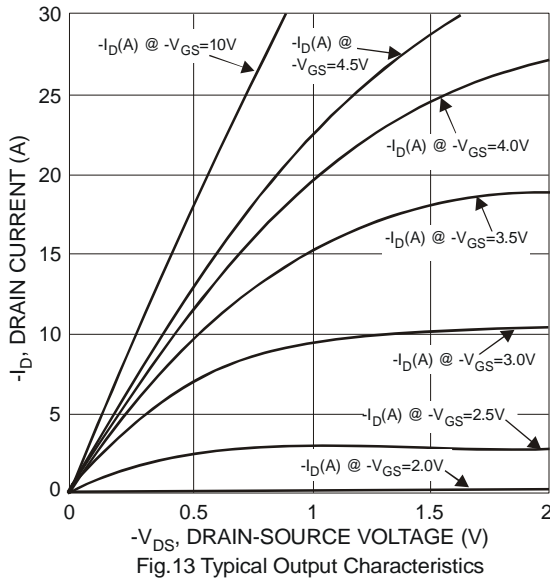


Fig. 12 SOA, Safe Operation Area

Electrical Characteristics P-CHANNEL – Q2 @ $T_A = 25^\circ\text{C}$ unless otherwise specified

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV_{DSS}	-30	-	-	V	$V_{GS} = 0V, I_D = -250\mu A$
Zero Gate Voltage Drain Current @ $T_c = 25^\circ\text{C}$	I_{DSS}	-	-	-1	μA	$V_{DS} = -30V, V_{GS} = 0V$
Gate-Source Leakage	I_{GSS}	-	-	± 100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	$V_{GS(th)}$	-1	-1.7	-2.2	V	$V_{DS} = V_{GS}, I_D = -250\mu A$
Static Drain-Source On-Resistance	$R_{DS(on)}$	-	30	39	Ω	$V_{GS} = -10V, I_D = -4.3A$
		-	42	53		$V_{GS} = -4.5V, I_D = -3.7A$
Forward Transfer Admittance	$ Y_{fs} $	-	10	-	S	$V_{DS} = -5V, I_D = -4.3A$
Diode Forward Voltage (Note 6)	V_{SD}	-	-0.75	-1.0	V	$V_{GS} = 0V, I_S = -1A$
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C_{iss}	-	1039	-	pF	$V_{DS} = -10V, V_{GS} = 0V, f = 1.0\text{MHz}$
Output Capacitance	C_{oss}	-	144	-	pF	
Reverse Transfer Capacitance	C_{rss}	-	134	-	pF	
Gate Resistance	R_g	-	13	-	Ω	$V_{DS} = 0V, V_{GS} = 0V, f = 1.0\text{MHz}$
Total Gate Charge (4.5V)	Q_g	-	10.1	-	nC	$V_{GS} = -10V, V_{DS} = -15V, I_D = -6A$
Total Gate Charge (10V)	Q_g	-	21.1	-	nC	
Gate-Source Charge	Q_{gs}	-	2.8	-	nC	
Gate-Drain Charge	Q_{gd}	-	3.2	-	nC	
Turn-On Delay Time	$t_{D(on)}$	-	10.1	-	ns	$V_{DS} = -15V, V_{GS} = -10V, R_G = 6\Omega, I_D = -1A$
Turn-On Rise Time	t_r	-	6.5	-	ns	
Turn-Off Delay Time	$t_{D(off)}$	-	50.1	-	ns	
Turn-Off Fall Time	t_f	-	22.2	-	ns	

Notes: 7. Short duration pulse test used to minimize self-heating effect
 8. Guaranteed by design. Not subject to product testing.



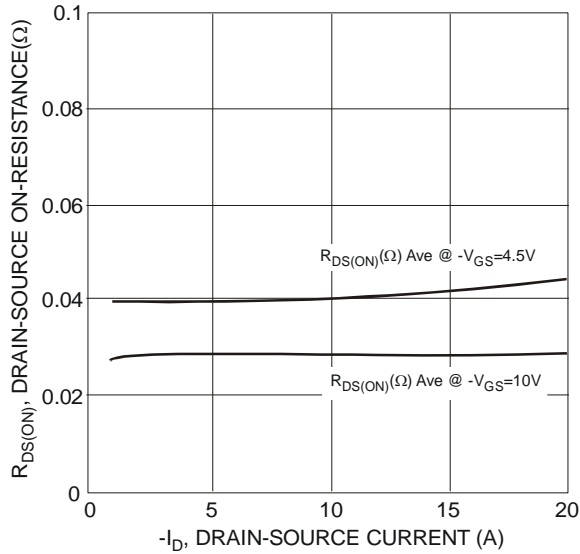


Fig. 15 Typical On-Resistance vs. Drain Current and Gate Voltage

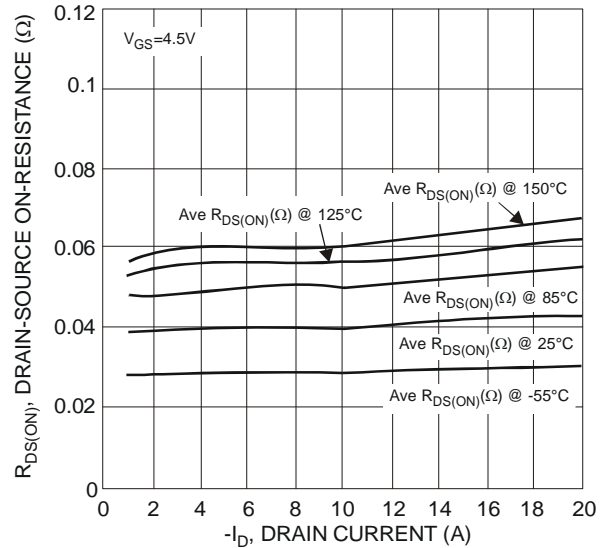


Fig. 16 Typical On-Resistance vs. Drain Current and Temperature

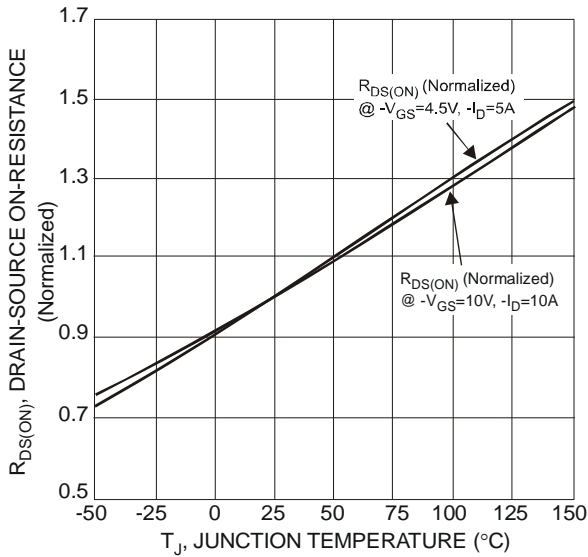


Fig. 17 On-Resistance Variation with Temperature

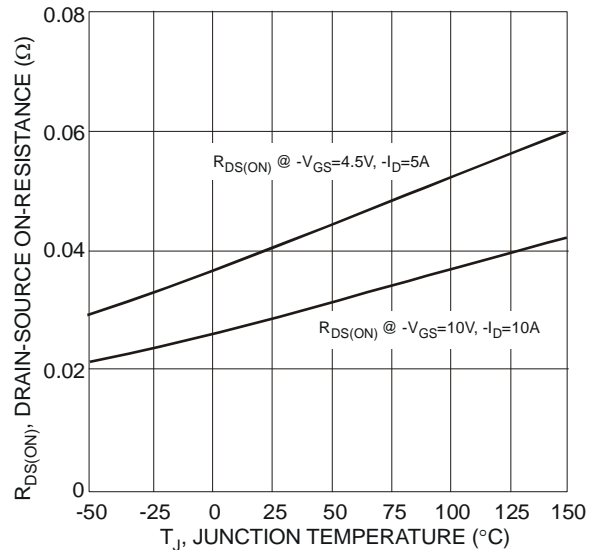


Fig. 18 On-Resistance Variation with Temperature

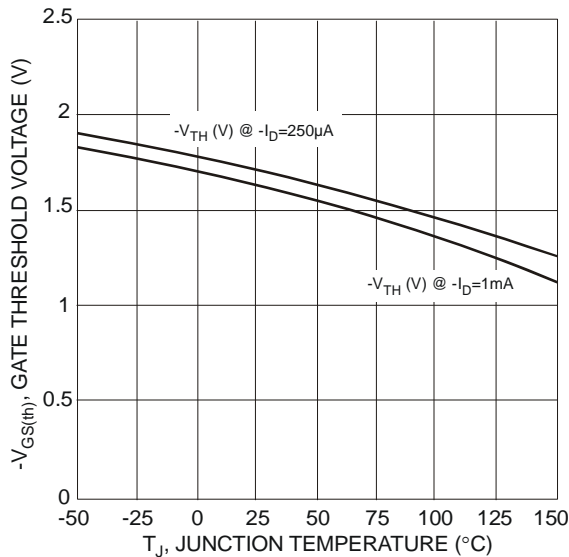


Fig. 19 On-Resistance Variation with Temperature

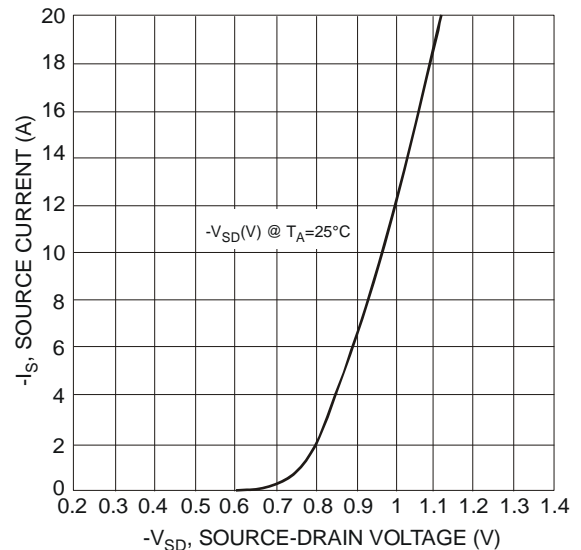


Fig. 20 Diode Forward Voltage vs. Current

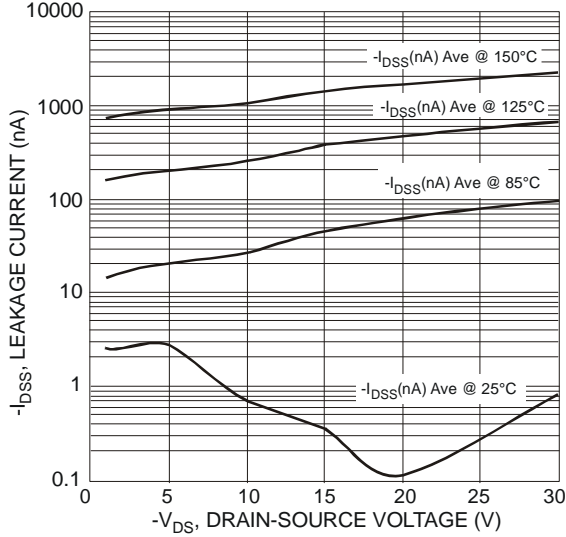


Fig. 21 Typical Drain-Source Leakage Current vs. Voltage

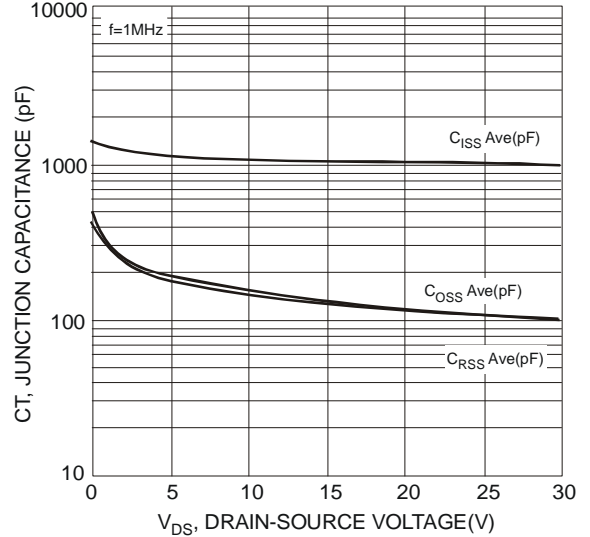


Fig. 22 Typical Junction Capacitance

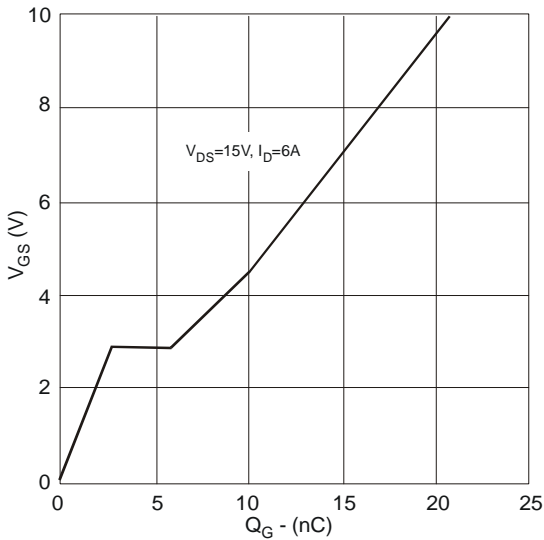


Fig. 23 Gate Charge Characteristics

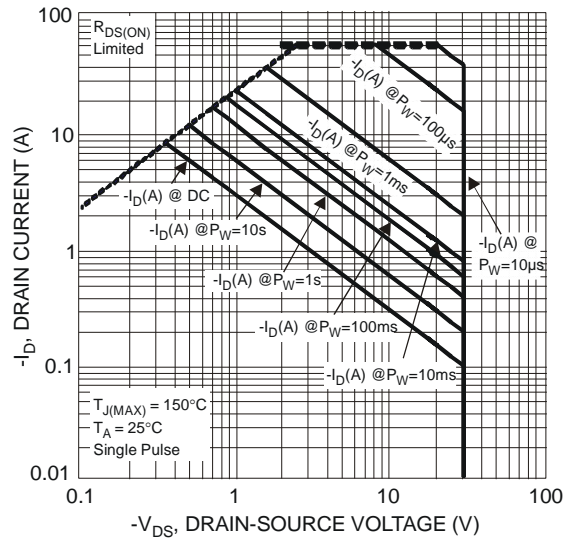


Fig. 24 SOA, Safe Operation Area

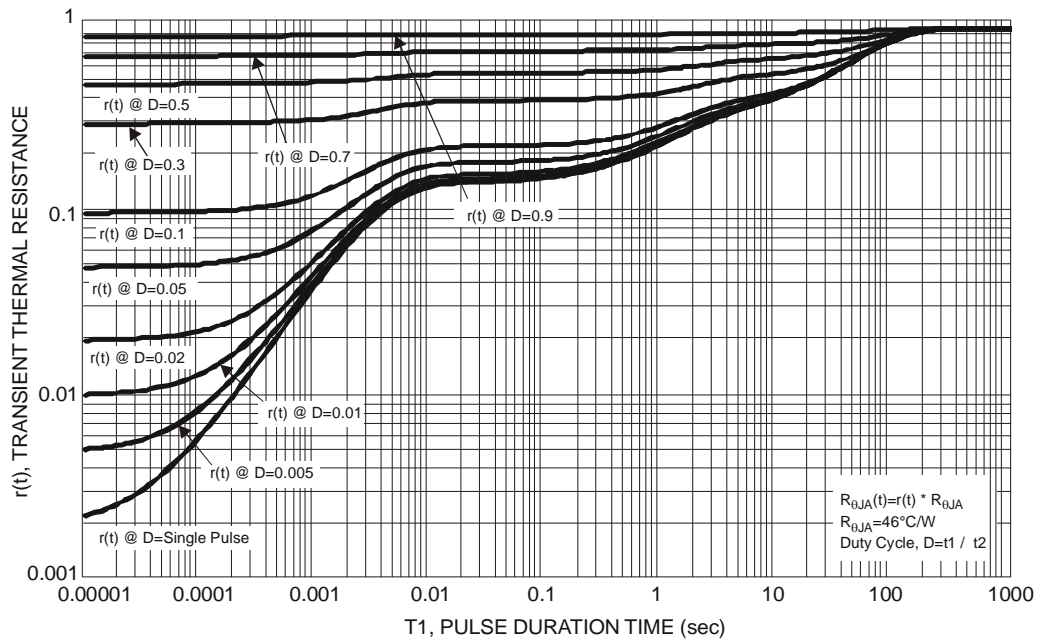
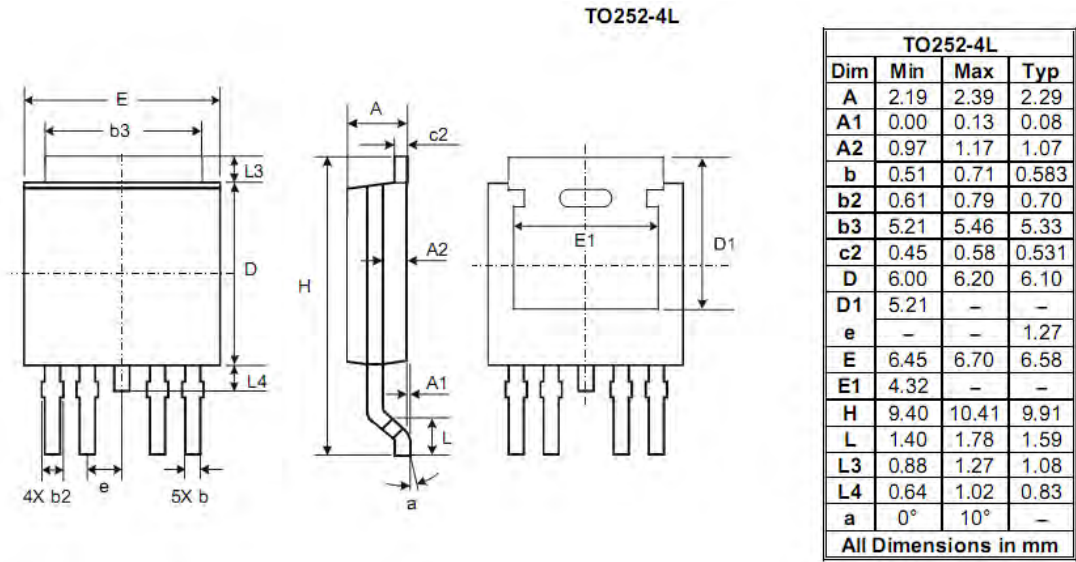
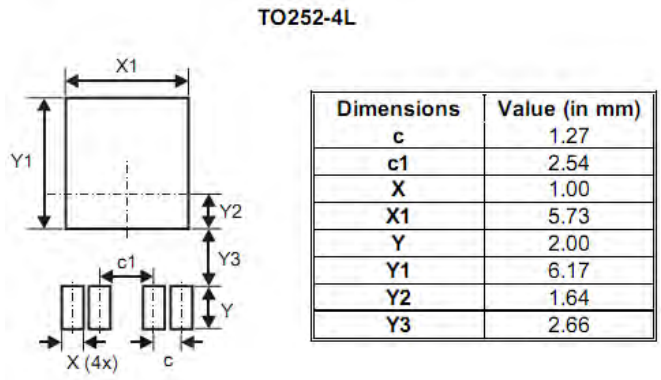


Fig. 25 Transient Thermal Resistance

Package Outline Dimensions



Suggested Pad Layout



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