

N-Channel 12-V (D-S) MOSFET

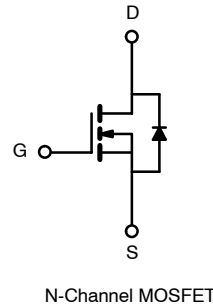
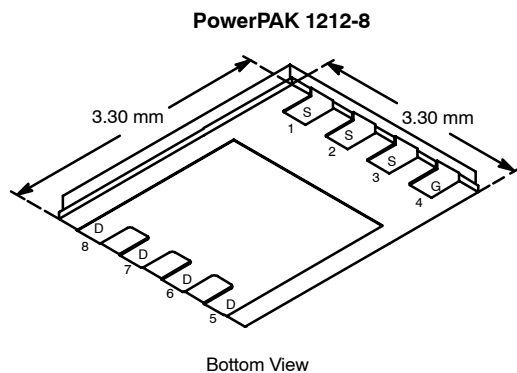
PRODUCT SUMMARY		
V _{DS} (V)	r _{DS(on)} (Ω)	I _D (A)
12	0.0057 @ V _{GS} = 4.5 V	20
	0.0067 @ V _{GS} = 2.5 V	18.8
	0.0085 @ V _{GS} = 1.8 V	16.5

FEATURES

- TrenchFET® Power MOSFET
- New Low Thermal Resistance PowerPAK® Package with Low 1.07-mm Profile

APPLICATIONS

- PA Switch, Load Switch and Battery Switch for Portable Devices
- Point-of-Load for 5-V or 3.3-V BUS Stepdown



Ordering Information: Si7402DN-T1

ABSOLUTE MAXIMUM RATINGS (T _A = 25°C UNLESS OTHERWISE NOTED)					
Parameter	Symbol	10 secs	Steady State	Unit	
Drain-Source Voltage	V _{DS}	12		V	
Gate-Source Voltage	V _{GS}	±8			
Continuous Drain Current (T _J = 150°C) ^a	I _D	T _A = 25°C	20	13	A
		T _A = 70°C	16	10	
Pulsed Drain Current	I _{DM}	50			
Continuous Source Current (Diode Conduction) ^a	I _S	3.2	1.3	W	
Maximum Power Dissipation ^a	P _D	T _A = 25°C	3.8		1.5
		T _A = 70°C	2.4		1.0
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55 to 150		°C	

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^a	R _{thJA}	t ≤ 10 sec	24	33	°C/W
		Steady State	65	81	
Maximum Junction-to-Case (Drain)	R _{thJC}	1.9	2.4		

Notes

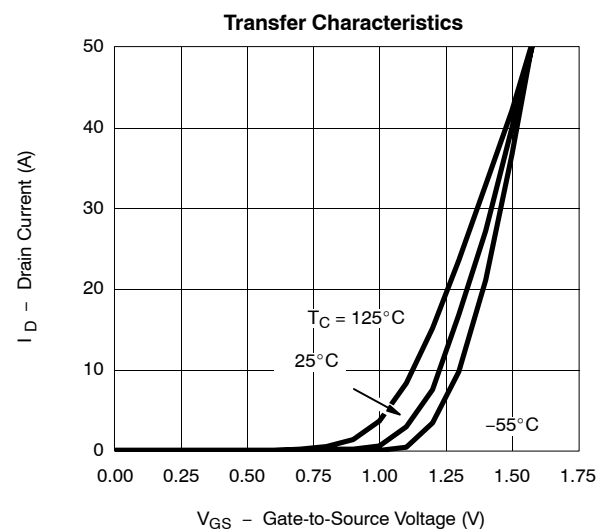
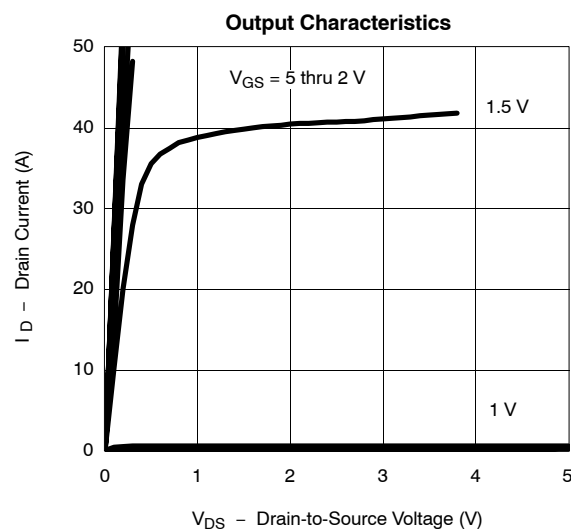
a. Surface Mounted on 1" x 1" FR4 Board.

MOSFET SPECIFICATIONS (T_J = 25 °C UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	0.45		0.85	V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 8 V			± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 12 V, V _{GS} = 0 V			1	μA
		V _{DS} = 12 V, V _{GS} = 0 V, T _J = 55 °C			5	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 4.5 V	50			A
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = 4.5 V, I _D = 20 A		0.0045	0.0057	Ω
		V _{GS} = 2.5 V, I _D = 18 A		0.0053	0.0067	
		V _{GS} = 1.8 V, I _D = 1 A		0.0065	0.0085	
Forward Transconductance ^a	g _{fs}	V _{DS} = 10 V, I _D = 20 A		100		S
Diode Forward Voltage ^a	V _{SD}	I _S = 3.2 A, V _{GS} = 0 V		0.70	1.2	V
Dynamic^b						
Total Gate Charge	Q _g	V _{DS} = 6 V, V _{GS} = 4.5 V, I _D = 20 A		36	55	nC
Gate-Source Charge	Q _{gs}		4			
Gate-Drain Charge	Q _{gd}		9.5			
Gate Resistance	R _g			1.8		Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = 6 V, R _L = 6 Ω I _D ≅ 1 A, V _{GEN} = 4.5 V, R _g = 6 Ω		35	55	ns
Rise Time	t _r		65	100		
Turn-Off Delay Time	t _{d(off)}		110	165		
Fall Time	t _f		60	90		
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 2.3 A, di/dt = 100 A/μs		40	80	

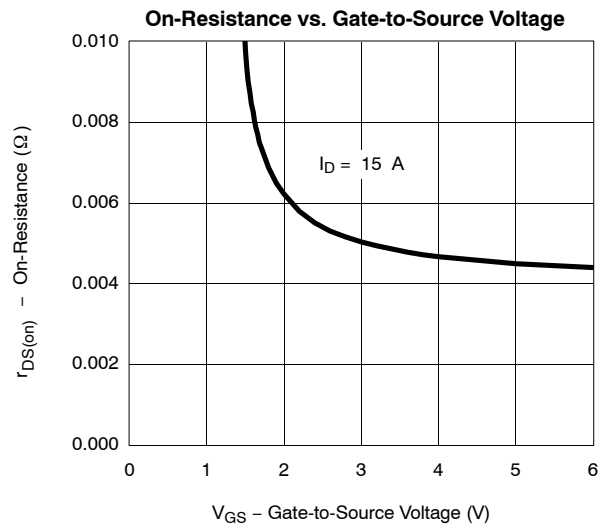
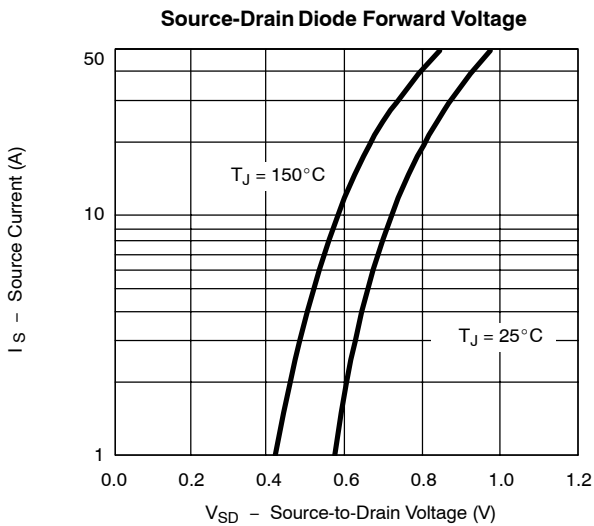
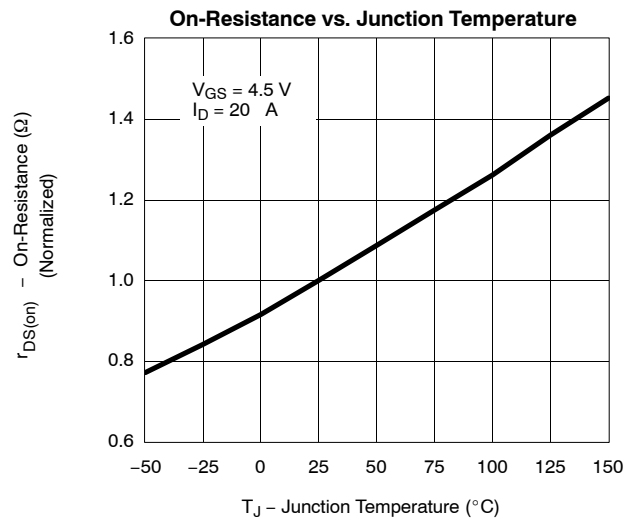
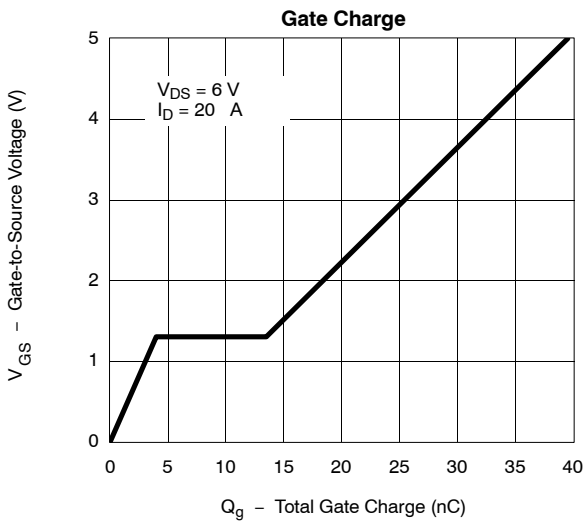
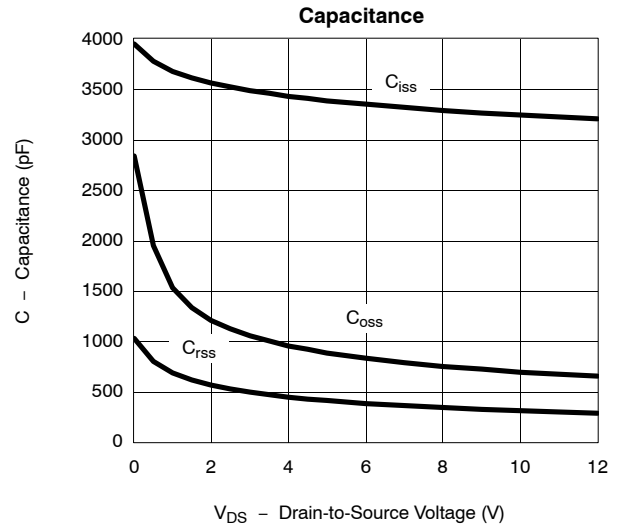
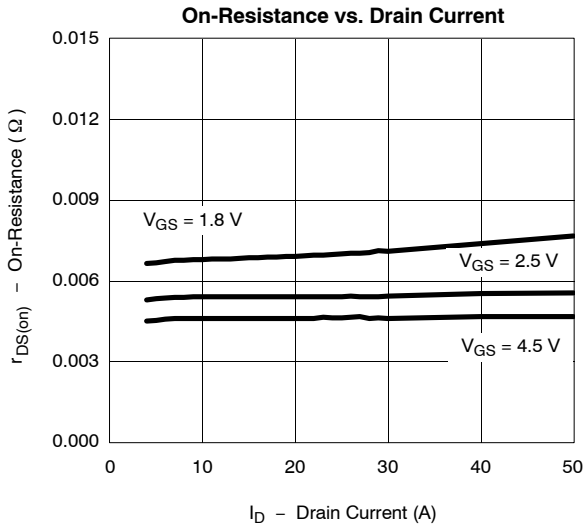
Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

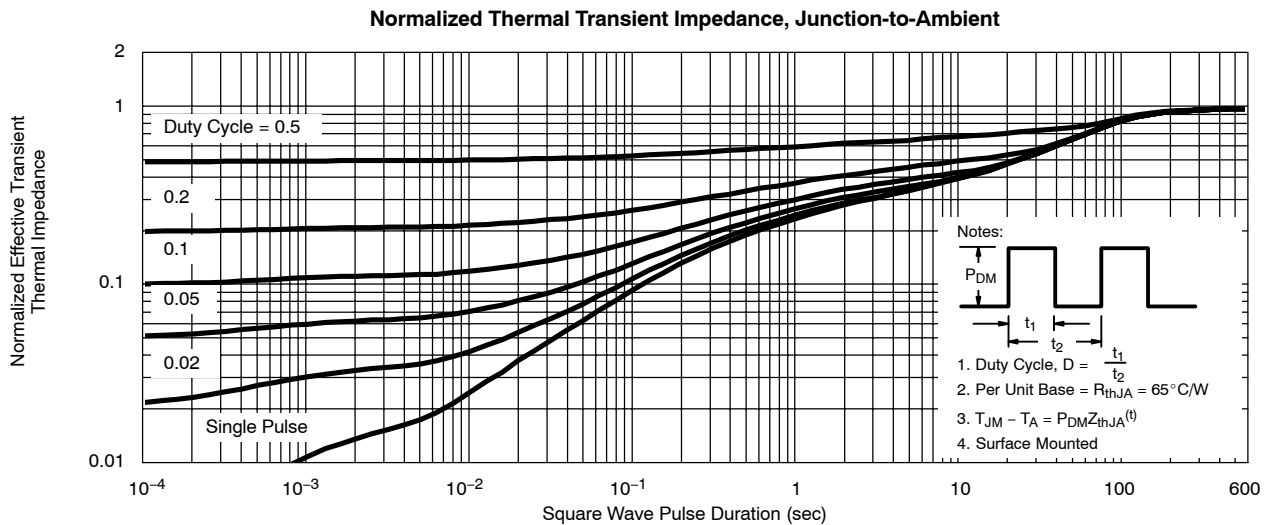
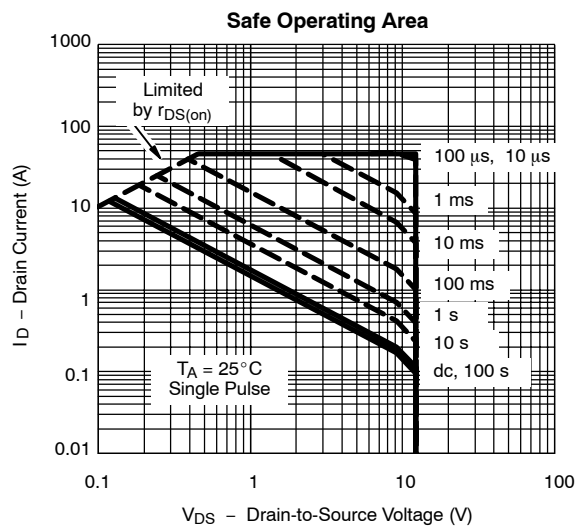
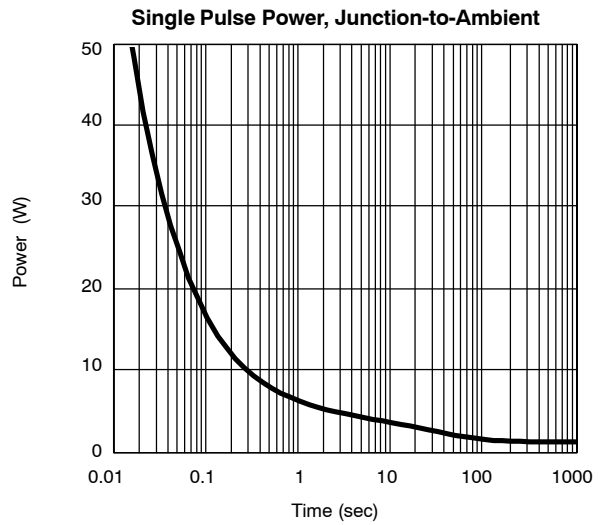
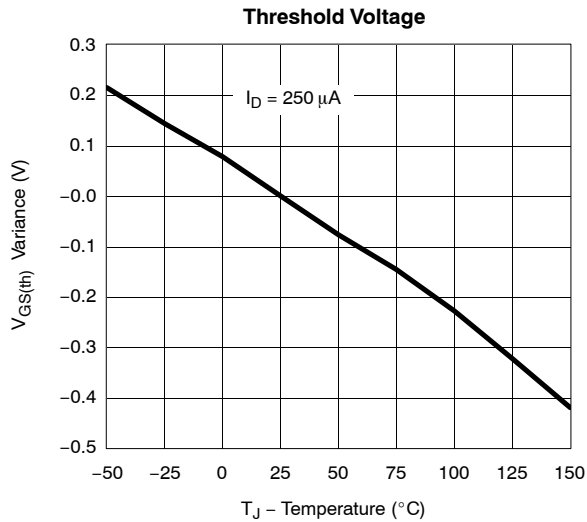
TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)



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