



P-Channel Enhancement-Mode Vertical DMOS FET

Features

- ▶ High input impedance and high gain
- ▶ Low power drive requirement
- ▶ Ease of paralleling
- ▶ Low C_{iss} and fast switching speeds
- ▶ Excellent thermal stability
- ▶ Integral source-drain diode
- ▶ Free from secondary breakdown
- ▶ Complementary N- and P-channel devices

Applications

- ▶ Logic level interfaces - ideal for TTL and CMOS
- ▶ Solid state relays
- ▶ Analog switches
- ▶ Power management
- ▶ Telecom switches

General Description

The Supertex TP5335 is a low threshold enhancement-mode (normally-off) transistor utilizing an advanced vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors and the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Ordering Information

Device	Package Option	BV_{DSS}/BV_{DGS} (V)	$R_{DS(ON)}$ (max) (Ω)	$V_{GS(TH)}$ (max) (V)
	TO-236AB (SOT-23)			
TP5335	TP5335K1-G	-350	30	-2.4

-G indicates package is RoHS compliant ("Green")



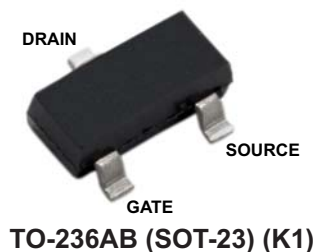
Absolute Maximum Ratings

Parameter	Value
Drain-to-source voltage	BV_{DSS}
Drain-to-gate voltage	BV_{DGS}
Gate-to-source voltage	$\pm 20V$
Operating and storage temperature	-55°C to +150°C
Soldering temperature*	300°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

* Distance of 1.6mm from case for 10 seconds.

Pin Configuration



Product Marking Information

P3SW W = Code for week sealed
 _____ = "Green" Packaging
TO-236AB (SOT-23) (K1)

Thermal Characteristics

Package	I_D (continuous) [†] (mA)	I_D (pulsed) (mA)	Power Dissipation @ $T_A = 25^\circ\text{C}$ (W)	θ_{jc} ($^\circ\text{C}/\text{W}$)	θ_{ja} ($^\circ\text{C}/\text{W}$)	I_{DR}^{\dagger} (mA)	I_{DRM} (mA)
TO-236AB (SOT-23)	-85	-400	0.36	200	350	-85	-400

Notes:

[†] I_D (continuous) is limited by max rated T_j .

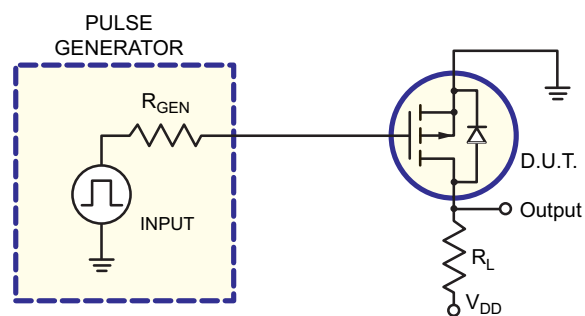
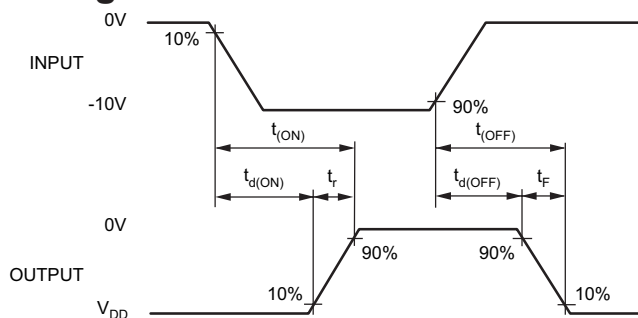
Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Sym	Parameter	Min	Typ	Max	Units	Conditions
BV_{DSS}	Drain-to-source breakdown voltage	-350	-	-	V	$V_{GS} = 0V, I_D = -100\mu\text{A}$
$V_{GS(TH)}$	Gate threshold voltage	-1.0	-	-2.4	V	$V_{DS} = V_{GS}, I_D = -1.0\text{mA}$
$\Delta V_{GS(TH)}$	Change in $V_{GS(TH)}$ with temperature	-	-	4.5	mV/ $^\circ\text{C}$	$V_{DS} = V_{GS}, I_D = -1.0\text{mA}$
I_{GSS}	Gate body leakage current	-	-	-100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$
I_{DSS}	Zero gate voltage drain current	-	-	-10	μA	$V_{DS} = \text{Max rating}, V_{GS} = 0V$
		-	-	-1.0	mA	$V_{DS} = 0.8 \text{ Max Rating}, V_{GS} = 0V, T_A = 125^\circ\text{C}$
		-	-	-5.0	nA	$V_{GS} = 0V, V_{DS} = -330V$
$I_{D(ON)}$	On-state drain current	-200	-	-	mA	$V_{GS} = -4.5V, V_{DS} = -25V$
		-400	-	-		$V_{GS} = -10V, V_{DS} = -25V$
$R_{DS(ON)}$	Static drain-to-source on-state resistance	-	-	75	Ω	$V_{GS} = -4.5V, I_D = -150\text{mA}$
		-	-	30		$V_{GS} = -10V, I_D = -200\text{mA}$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with temperature	-	-	1.7	%/ $^\circ\text{C}$	$V_{GS} = -10V, I_D = -200\text{mA}$
G_{FS}	Forward transconductance	125	-	-	mmho	$V_{DS} = -25V, I_D = -200\text{mA}$
C_{ISS}	Input capacitance	-	-	110	pF	$V_{GS} = 0V,$ $V_{DS} = -25V,$ $f = 1\text{MHz}$
C_{OSS}	Common source output capacitance	-	-	60		
C_{RSS}	Reverse transfer capacitance	-	-	22		
$t_{d(ON)}$	Turn-on delay time	-	-	20	ns	$V_{DD} = -25V,$ $I_D = -150\text{mA},$ $R_{GEN} = 25\Omega,$
t_r	Rise time	-	-	15		
$t_{d(OFF)}$	Turn-off delay time	-	-	25		
t_f	Fall time	-	-	25		
V_{SD}	Diode forward voltage drop	-	-	-1.8	V	$V_{GS} = 0V, I_{SD} = -200\text{mA}$
t_{rr}	Reverse recovery time	-	800	-	ns	$V_{GS} = 0V, I_{SD} = -200\text{mA}$

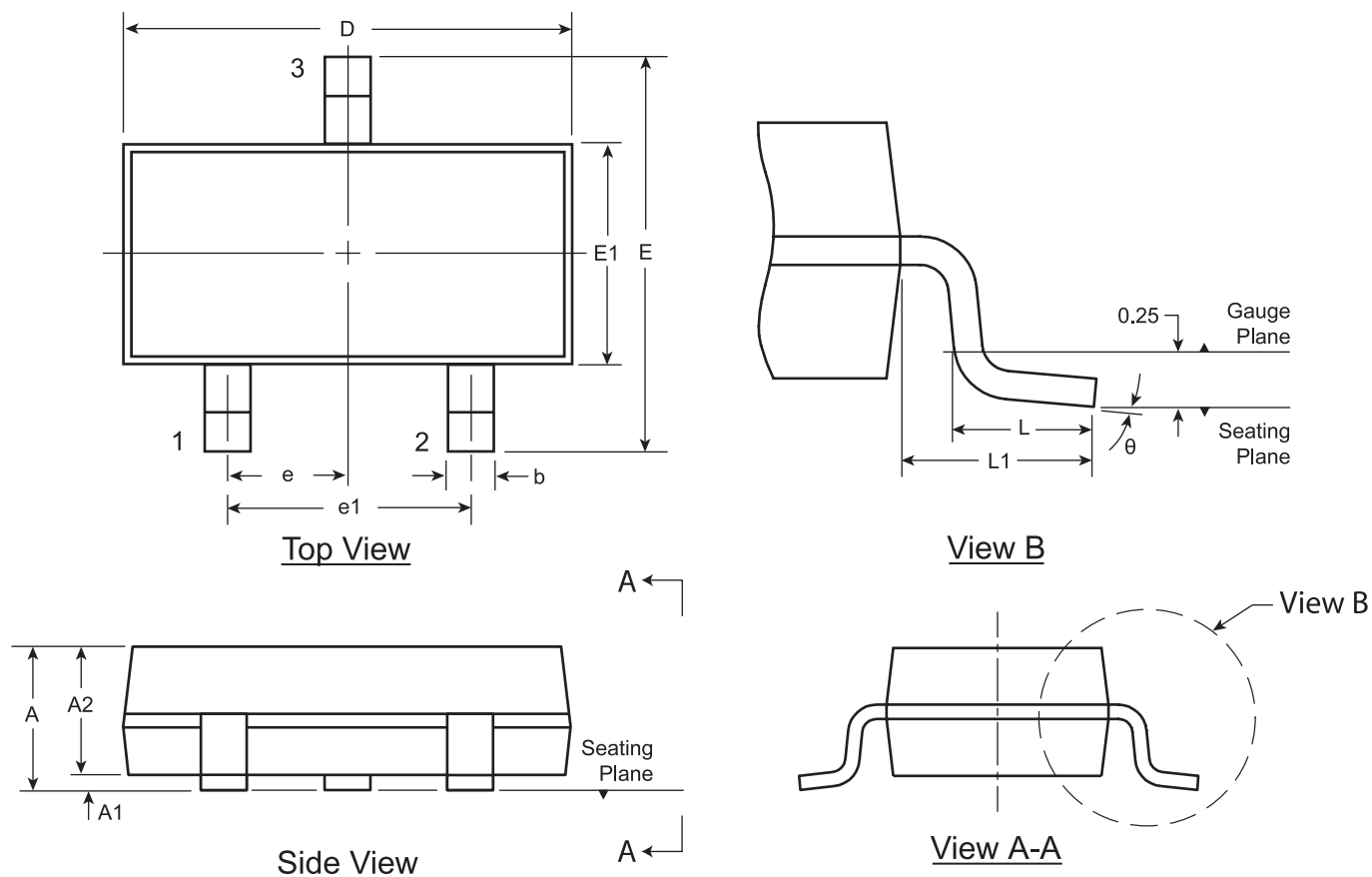
Notes:

1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: $300\mu\text{s}$ pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

Switching Waveforms and Test Circuit



3-Lead TO-236AB (SOT-23) Package Outline (K1) 2.90x1.30mm body, 1.12mm height (max), 1.90mm pitch



Symbol		A	A1	A2	b	D	E	E1	e	e1	L	L1	θ
Dimension (mm)	MIN	0.89	0.01	0.88	0.30	2.80	2.10	1.20	0.95 BSC	1.90 BSC	0.40	0.54 REF	0°
	NOM	-	-	0.95	-	2.90	-	1.30			0.50		-
	MAX	1.12	0.10	1.02	0.50	3.04	2.64	1.40			0.60		8°

JEDEC Registration TO-236, Variation AB, Issue H, Jan. 1999.

Drawings not to scale.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

Supertex inc. does not recommend the use of its products in life support applications, and will not knowingly sell its products for use in such applications, unless it receives an adequate "product liability indemnification insurance agreement". **Supertex** does not assume responsibility for use of devices described and limits its liability to the replacement of the devices determined defective due to workmanship. No responsibility is assumed for possible omissions or inaccuracies. Circuitry and specifications are subject to change without notice. For the latest product specifications, refer to the **Supertex** website: <http://www.supertex.com>.

©2008 **Supertex inc.** All rights reserved. Unauthorized use or reproduction is prohibited.

Supertex inc.

1235 Bordeaux Drive, Sunnyvale, CA 94089
TEL: (408) 222-8888 / FAX: (408) 222-4895

www.supertex.com