



P-Channel Enhancement-Mode Vertical DMOS FETs

Features

- ▶ High input impedance
- ▶ Low threshold (-2.4V max.)
- ▶ Low input capacitance (110pF max.)
- ▶ Fast switching speeds
- ▶ Low on-resistance
- ▶ Low input and output leakage
- ▶ Free from secondary breakdown
- ▶ Complementary N- and P-channel devices

Applications

- ▶ Logic level interfaces - ideal for TTL and CMOS
- ▶ Battery operated systems
- ▶ Photo voltaic devices
- ▶ Analog switches
- ▶ General purpose line drivers
- ▶ Telecom switches

General Description

The Supertex TP5322 is a low threshold enhancement-mode (normally-off) transistor utilizing an advanced vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Ordering Information

Device	Package Options		BV _{DSS} /BV _{DGS} (V)	R _{DS(ON)} (max) (Ω)	V _{GS(TH)} (max) (V)	I _{D(ON)} (min) (A)
	TO-236AB (SOT-23)	TO-243AA (SOT-89)				
TP5322	TP5322K1-G	TP5322N8-G	-220	12	12	-0.7

-G indicates package is RoHS compliant ('Green')



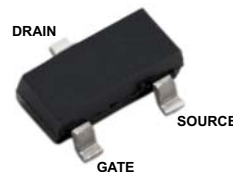
Absolute Maximum Ratings

Parameter	Value
Drain-to-source voltage	BV _{DSS}
Drain-to-gate voltage	BV _{DGS}
Gate-to-source voltage	±20V
Operating and storage temperature	-55°C to +150°C
Soldering temperature*	300°C

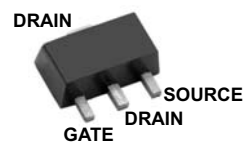
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

* Distance of 1.6mm from case for 10 seconds.

Pin Configurations



TO-236AB (SOT-23) (K1)



TO-243AA (SOT-89) (N8)

Product Marking

P3CW W = Code for week sealed
 _____ = "Green" Packaging
TO-236AB (SOT-23) (K1)

TP3CW W = Code for week sealed
 _____ = "Green" Packaging
TO-243AA (SOT-89) (N8)

Thermal Characteristics

Package	I_D (continuous) [†] (A)	I_D (pulsed) (A)	Power Dissipation @ $T_c = 25^\circ\text{C}$ (W)	θ_{jc} ($^\circ\text{C}/\text{W}$)	θ_{ja} ($^\circ\text{C}/\text{W}$)	I_{DR}^\ddagger (A)	I_{DRM} (A)
TO-236AB (SOT-23)	-0.12	-0.70	0.36	200	350	-0.12	-0.7
TO-243AA (SOT-89)	-0.26	-0.90	1.6	15	78 [‡]	-0.26	-0.9

Notes:

- [†] I_D (continuous) is limited by max rated T_f .
- [‡] Mounted on FR4 board, 25mm x 25mm x 1.57mm.

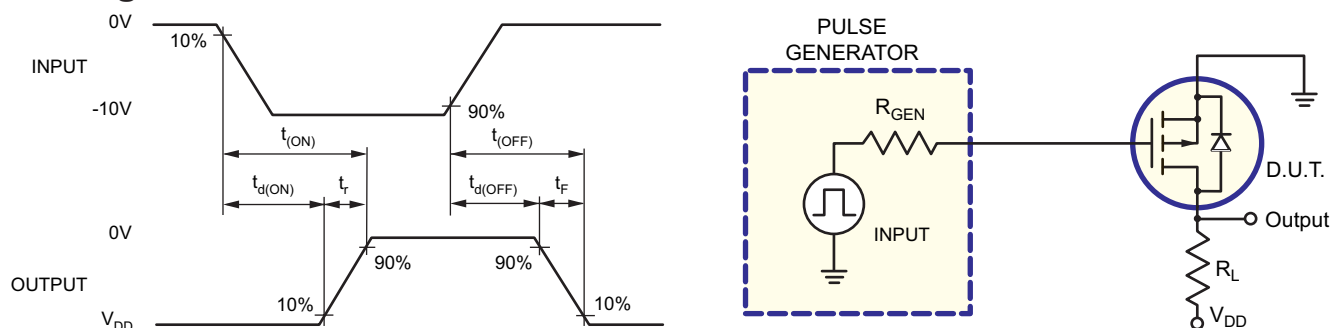
Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Sym	Parameter	Min	Typ	Max	Units	Conditions
BV_{DSS}	Drain-to-source breakdown voltage	-220	-	-	V	$V_{GS} = 0\text{V}, I_D = -2.0\text{mA}$
$V_{GS(TH)}$	Gate threshold voltage	-1.0	-	-2.4	V	$V_{GS} = V_{DS}, I_D = -1.0\text{mA}$
$\Delta V_{GS(TH)}$	Change in $V_{GS(TH)}$ with temperature	-	-	4.5	mV/ $^\circ\text{C}$	$V_{GS} = V_{DS}, I_D = -1.0\text{mA}$
I_{GSS}	Gate body leakage current	-	-	-100	nA	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$
$I_{D(SS)}$	Zero gate voltage drain current	-	-	-10	μA	$V_{DS} = \text{Max rating}, V_{GS} = 0\text{V}$
		-	-	-1.0	mA	$V_{DS} = 0.8 \text{ Max Rating}, V_{GS} = 0\text{V}, T_A = 125^\circ\text{C}$
$I_{D(ON)}$	On-state drain current	-0.7	-0.95	-	A	$V_{GS} = -10\text{V}, V_{DS} = -25\text{V}$
$R_{DS(ON)}$	Static drain-to-source on-state resistance	-	10	15	Ω	$V_{GS} = -4.5\text{V}, I_D = -100\text{mA}$
		-	8.0	12		$V_{GS} = -10\text{V}, I_D = -200\text{mA}$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with temperature	-	-	1.7	%/ $^\circ\text{C}$	$V_{GS} = -10\text{V}, I_D = -200\text{mA}$
G_{FS}	Forward transconductance	100	250	-	mmho	$V_{DS} = -25\text{V}, I_D = -200\text{mA}$
C_{ISS}	Input capacitance	-	-	110	pF	$V_{GS} = 0\text{V}, V_{DS} = -25\text{V}, f = 1.0\text{MHz}$
C_{OSS}	Common source output capacitance	-	-	45		
C_{RSS}	Reverse transfer capacitance	-	-	20		
$t_{d(ON)}$	Turn-on delay time	-	-	10	ns	$V_{DD} = -25\text{V}, I_D = -700\text{mA}, R_{GEN} = 25\Omega,$
t_r	Rise time	-	-	15		
$t_{d(OFF)}$	Turn-off delay time	-	-	20		
t_f	Fall time	-	-	15		
V_{SD}	Diode forward voltage drop	-	-	-1.8	V	$V_{GS} = 0\text{V}, I_{SD} = -500\text{mA}$
t_{rr}	Reverse recovery time	-	300	-	ns	$V_{GS} = 0\text{V}, I_{SD} = -500\text{mA}$

Notes:

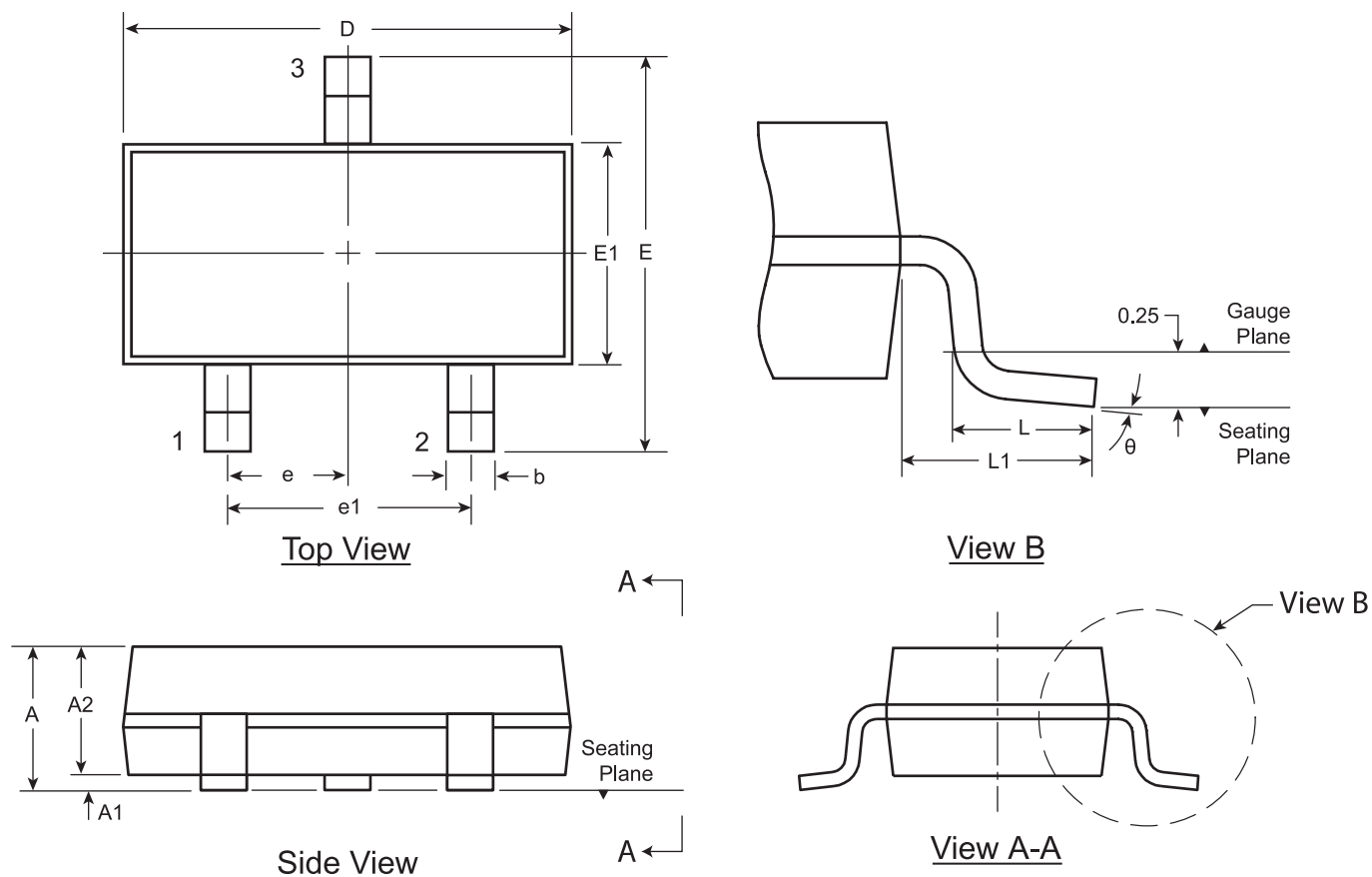
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300 μs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

Switching Waveforms and Test Circuit



3-Lead TO-236AB (SOT-23) Package Outline (K1)

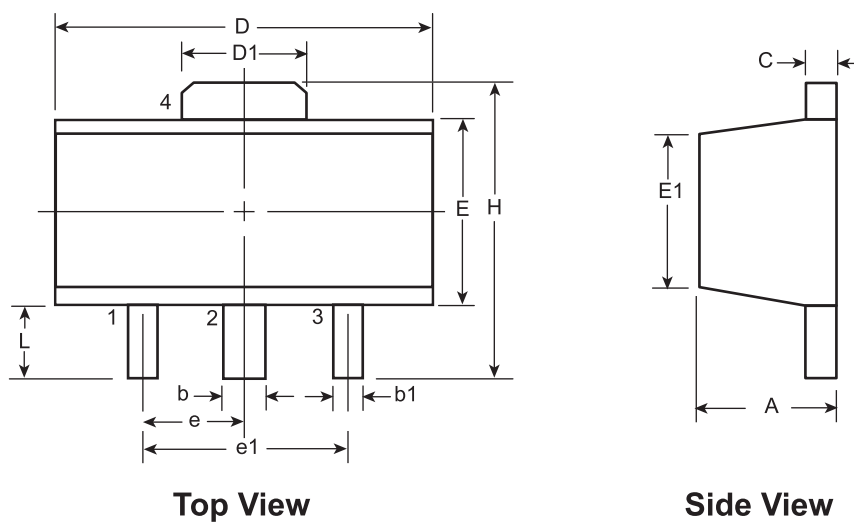
2.90x1.30mm body, 1.12mm height (max), 1.90mm pitch



Symbol		A	A1	A2	b	D	E	E1	e	e1	L	L1	θ
Dimension (mm)	MIN	0.89	0.01	0.88	0.30	2.80	2.10	1.20	0.95 BSC	1.90 BSC	0.40	0.54 REF	0°
	NOM	-	-	0.95	-	2.90	-	1.30			0.50		-
	MAX	1.12	0.10	1.02	0.50	3.04	2.64	1.40			0.60		8°

JEDEC Registration TO-236, Variation AB, Issue H, Jan. 1999.
 Drawings not to scale.

3-Lead TO-243AA (SOT-89) Package Outline (N8)



Symbol		A	b	b1	C	D	D1	E	E1	e	e1	H	L	
Dimensions (mm)	MIN	1.40	0.44	0.36	0.35	4.40	1.62	2.29	2.13	1.50 BSC	3.00 BSC	3.94	0.89	
	NOM	-	-	-	-	-	-	-	-			-	-	-
	MAX	1.60	0.56	0.48	0.44	4.60	1.83	2.60	2.29			4.25	1.20	

JEDEC Registration TO-243, Variation AA, Issue C, July 1986.

Drawings not to scale.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

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