# P-Channel Enhancement-Mode Lateral MOSFET

## Ordering Information

| $BV_{DSS}$ / $BV_{DGS}$ | $R_{DS(ON)}$ (max) | $I_{D(ON)}$ (min) | $V_{GS(th)}$ (max) | Order Number / Package | | |
|---|---|---|---|---|---|---|
| | | | | TO-92 | SO-8 | Die |
| -16.5V | 1.5Ω | -1.25A | -1.0V | LP0701N3 | LP0701LG | LP0701ND |

## Features

- ❏ Ultra low threshold
- ❏ High input impedance
- ❏ Low input capacitance
- ❏ Fast switching speeds
- ❏ Low on resistance
- ❏ Freedom from secondary breakdown
- ❏ Low input and output leakage
- ❏ Complementary N- and P-channel devices

## Advanced MOS Technology

These enhancement-mode (normally-off) transistors utilize a lateral MOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown. The low threshold voltage and low on-resistance characteristics are ideally suited for hand held battery operated applications.

## Applications

- ❏ Logic level interfaces
- ❏ Solid state relays
- ❏ Battery operated systems
- ❏ Photo voltaic drives
- ❏ Analog switches
- ❏ General purpose line drivers

## Absolute Maximum Ratings

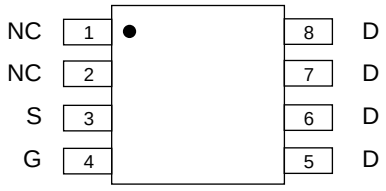
| | |
|---|---|
| Drain-to-Source Voltage | $BV_{DSS}$ |
| Drain-to-Gate Voltage | $BV_{DGS}$ |
| Gate-to-Source Voltage | ± 10V |
| Operating and Storage Temperature | -55°C to +150°C |
| Soldering Temperature* | 300°C |

*Distance of 1.6 mm from case for 10 seconds.

## Package Options

S G D

TO-92




SO-8
top view

Note: See Package Outline section for dimensions.

# Thermal Characteristics

| Package | $I_D$ (continuous)* | $I_D$ (pulsed)* | Power Dissipation @ $T_C$ = 25°C | $\theta_{jc}$ °C/W | $\theta_{ja}$ °C/W | $I_{DR}$ | $I_{DRM}$* |
|---|---|---|---|---|---|---|---|
| TO-92 | -0.5A | -1.25A | 1W | 125 | 170 | -0.5A | -1.25A |
| SO-8 | -0.7A | -1.25A | 1.5W† | 83 | 104† | -0.7A | -1.25A |

* $I_D$ (continuous) is limited by max rated $T_j$.

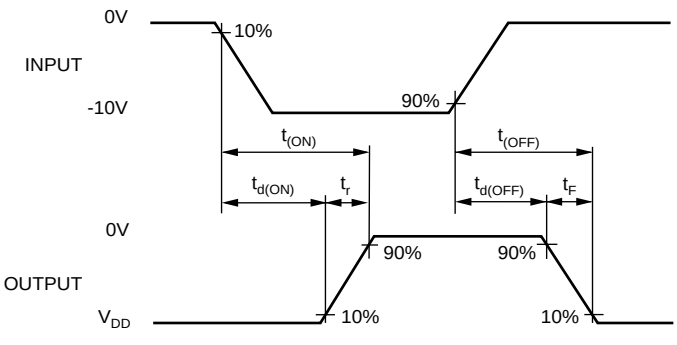
† Mounted on FR4 board, 25mm x 25mm x 1.57mm.

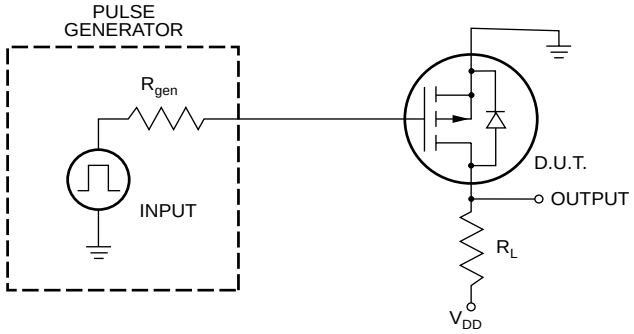
# Electrical Characteristics (@ 25°C unless otherwise specified)

| Symbol | Parameter | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| $BV_{DSS}$ | Drain-to-Source Breakdown Voltage | -16.5 | | | V | $V_{GS}$ = 0V, $I_D$ = -1mA |
| $V_{GS(th)}$ | Gate Threshold Voltage | -0.5 | -0.7 | -1.0 | V | $V_{GS}$ = $V_{DS}$, $I_D$ = -1mA |
| $\Delta V_{GS(th)}$ | Change in $V_{GS(th)}$ with Temperature | | | -4.0 | mV/°C | $V_{GS}$ = $V_{DS}$, $I_D$ = -1mA |
| $I_{GSS}$ | Gate Body Leakage | | | -100 | nA | $V_{GS}$ = ±10V, $V_{DS}$ = 0V |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | | | -100 | nA | $V_{DS}$ = -15V, $V_{GS}$ = 0V |
| | | | | -1.0 | mA | $V_{DS}$ = 0.8 Max Rating, $V_{GS}$ = 0V, TA = 125°C |
| $I_{D(ON)}$ | ON-State Drain Current | | -0.4 | | A | $V_{GS}$ = $V_{DS}$ = -2V |
| | | -0.6 | -1.0 | | | $V_{GS}$ = $V_{DS}$ = -3V |
| | | -1.25 | -2.3 | | A | $V_{GS}$ = $V_{DS}$ = -5V |
| $R_{DS(ON)}$ | Static Drain-to-Source ON-State Resistance | | 2.0 | 4.0 | Ω | $V_{GS}$ = -2V, $I_D$ = -50mA |
| | | | 1.7 | 2.0 | | $V_{GS}$ = -3V, $I_D$ = -150mA |
| | | | 1.3 | 1.5 | | $V_{GS}$ = -5V, $I_D$ = -300mA |
| $\Delta R_{DS(ON)}$ | Change in $R_{DS(ON)}$ with temperature | | | 0.75 | %/°C | $V_{GS}$ = -5V, $I_D$ = -300mA |
| $G_{FS}$ | Forward Transconductance | 500 | 700 | | m℧ | $V_{DS}$ = -15V, $I_D$ = -1A |
| $C_{ISS}$ | Input Capacitance | | 120 | 250 | pF | $V_{GS}$ = 0V, $V_{DS}$ = -15V, f = 1MHz |
| $C_{OSS}$ | Common Source Output Capacitance | | 100 | 125 | | |
| $C_{RSS}$ | Reverse Transfer Capacitance | | 40 | 60 | | |
| $t_{d(ON)}$ | Turn-ON Delay Time | | | 20 | ns | $V_{DD}$ =-15V, $I_D$ = -1.25A, $R_{GEN}$ = 25Ω |
| $t_r$ | Rise Time | | | 20 | | |
| $t_{d(OFF)}$ | Turn-OFF Delay Time | | | 30 | | |
| $t_f$ | Fall Time | | | 30 | | |
| $V_{SD}$ | Diode Forward Voltage Drop | | -1.2 | -1.5 | V | $V_{GS}$ = 0V, $I_{SD}$ = -500mA |

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300μs pulse, 2% duty cycle.)
Note 2: All A.C. parameters sample tested.

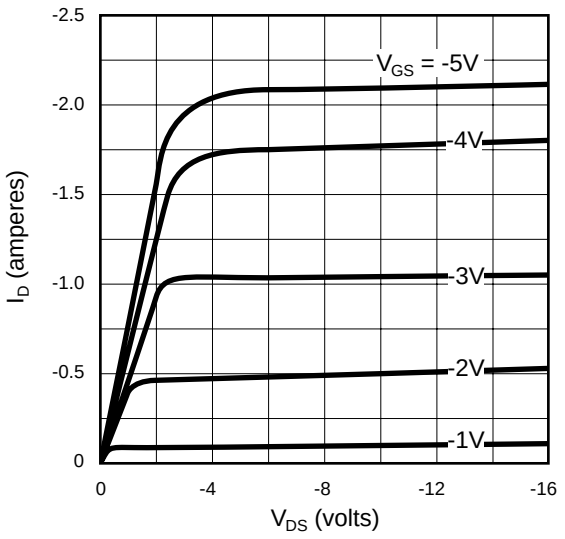
# Switching Waveforms and Test Circuit



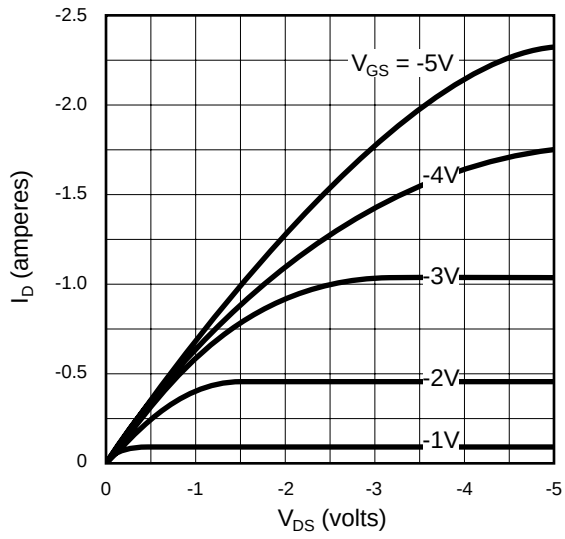



# Typical Performance Curves

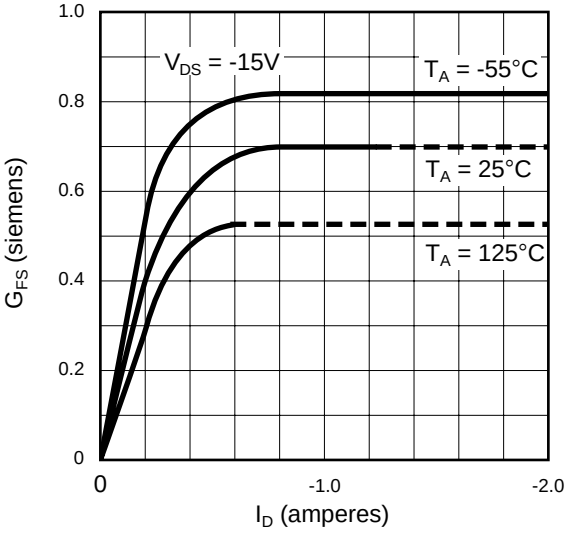
Output Characteristics



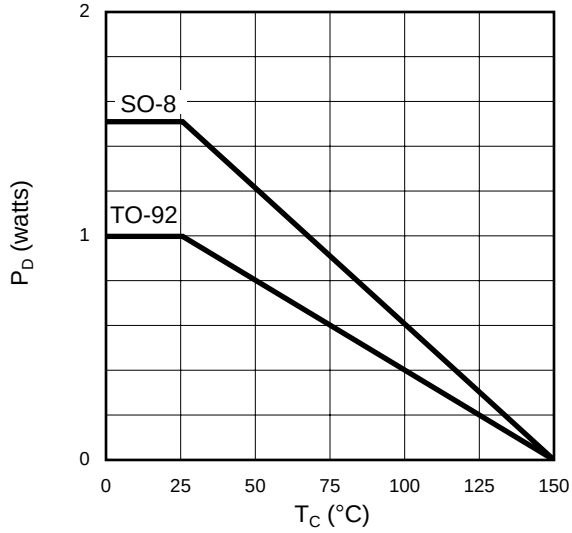

Saturation Characteristics



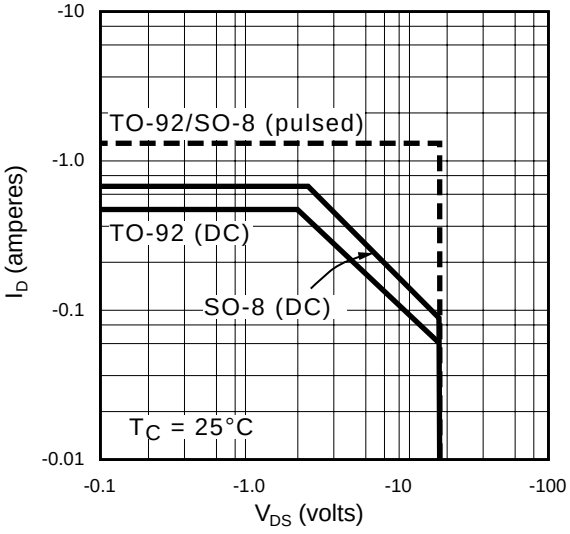

Transconductance vs. Drain Current



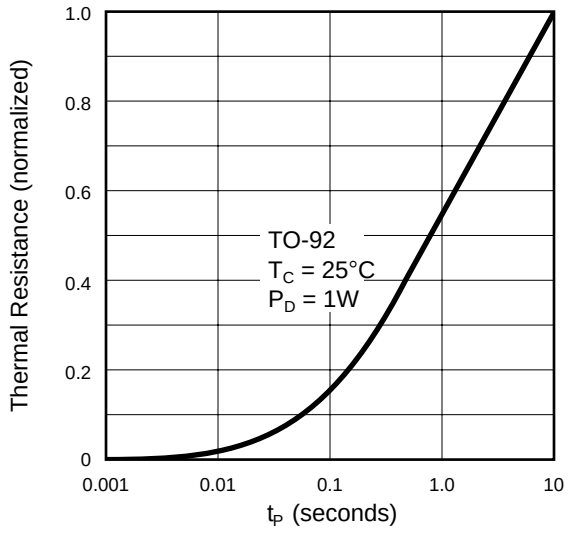

Power Dissipation vs. Case Temperature




Maximum Rated Safe Operating Area

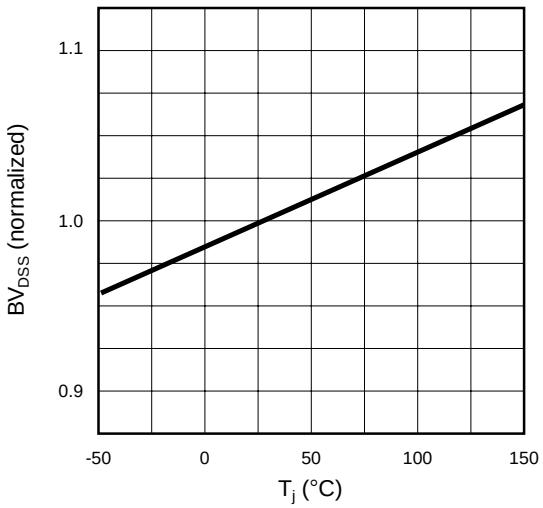



Thermal Response Characteristics

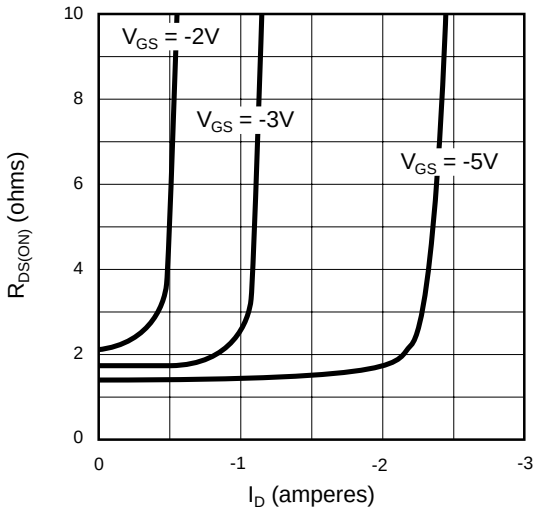


# Typical Performance Curves

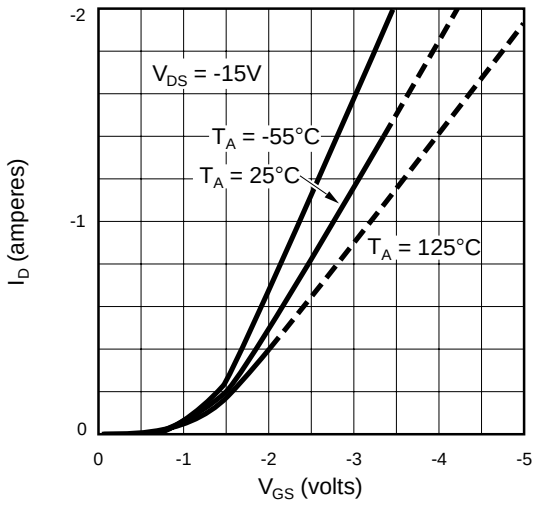
$BV_{DSS}$ Variation with Temperature



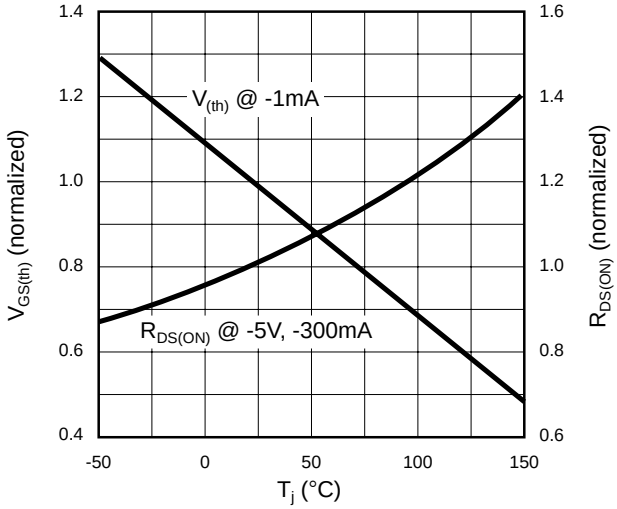

On-Resistance vs. Drain Current



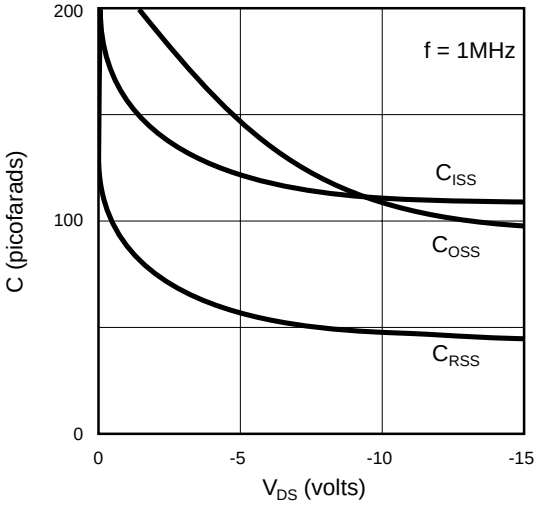

Transfer Characteristics



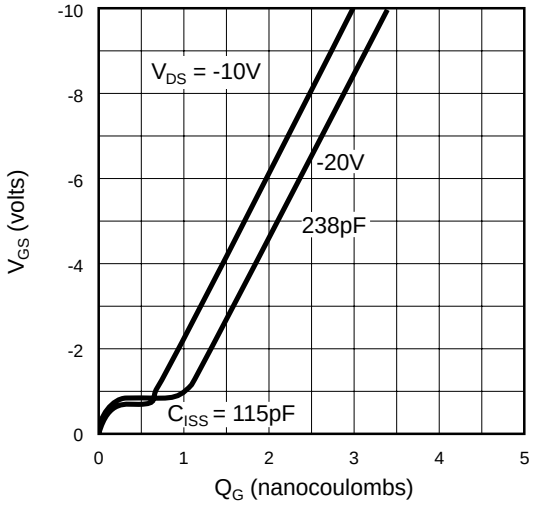

$V_{(th)}$ and $R_{DS}$ Variation with Temperature




Capacitance vs. Drain-to-Source Voltage




Gate Drive Dynamic Characteristics



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