# Supertex inc.



## P-Channel Enhancement-Mode Lateral MOSFET

#### **Ordering Information**

BV <sub>DSS</sub> /	R <sub>DS(ON)</sub>	I <sub>D(ON)</sub>	V <sub>GS(th)</sub>	Ord	er Number / Package		
BV	(max)	(min)	(max)	TO-92	SO-8	Die	
-16.5V	1.5Ω	-1.25A	-1.0V	LP0701N3	LP0701LG	LP0701ND	

#### **Features**

- Ultra low threshold
- High input impedance
- Low input capacitance
- Fast switching speeds
- Low on resistance
- □ Freedom from secondary breakdown
- Low input and output leakage
- Complementary N- and P-channel devices

## Applications

- Logic level interfaces
- Solid state relays
- Battery operated systems
- Photo voltaic drives
- Analog switches
- General purpose line drivers

## **Absolute Maximum Ratings**

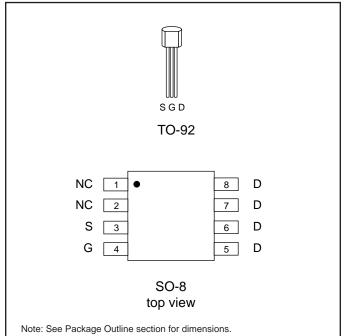
Drain-to-Source Voltage	D V DSS
Drain-to-Gate Voltage	BV <sub>DGS</sub>
Gate-to-Source Voltage	± 10V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

\*Distance of 1.6 mm from case for 10 seconds.

## **Advanced MOS Technology**

These enhancement-mode (normally-off) transistors utilize a lateral MOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown. The low threshold voltage and low onresistance characteristics are ideally suited for hand held battery operated applications.

## Package Options



#### 01/06/03

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## **Thermal Characteristics**

Package	I <sub>D</sub> (continuous)*	l <sub>D</sub> (pulsed)*	Power Dissipation @ T <sub>c</sub> = 25°C	θ <sub>jc</sub> °C/W	θ <sub>ja</sub> °C/W	l <sub>DR</sub>	I <sub>DRM</sub> *
TO-92	-0.5A	-1.25A	1W	125	170	-0.5A	-1.25A
SO-8	-0.7A	-1.25A	1.5W <sup>†</sup>	83	104 <sup>†</sup>	-0.7A	-1.25A

\*  $I_{D}$  (continuous) is limited by max rated  $T_{i}$ .

<sup>†</sup> Mounted on FR4 board, 25mm x 25mm x 1.57mm.

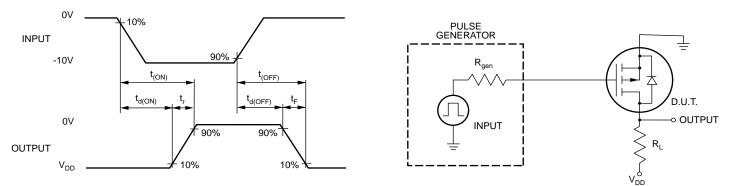
#### Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter	Min	Тур	Max	Unit	Conditions
BV <sub>DSS</sub>	Drain-to-Source Breakdown Voltage	-16.5			V	$V_{GS} = 0V, I_D = -1mA$
V <sub>GS(th)</sub>	Gate Threshold Voltage	-0.5	-0.7	-1.0	V	$V_{GS} = V_{DS}, I_D = -1mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-4.0	mV/°C	$V_{GS} = V_{DS}, I_D = -1mA$
I <sub>GSS</sub>	Gate Body Leakage			-100	nA	$V_{GS} = \pm 10V, V_{DS} = 0V$
I <sub>DSS</sub>	Zero Gate Voltage Drain Current			-100	nA	$V_{DS} = -15V, V_{GS} = 0V$
				-1.0	mA	$V_{DS} = 0.8$ Max Rating, $V_{GS} = 0V$ , TA = 125°C
			-0.4		А	$V_{GS} = V_{DS} = -2V$
I <sub>D(ON)</sub>	ON-State Drain Current	-0.6	-1.0			$V_{GS} = V_{DS} = -3V$
		-1.25	-2.3		А	$V_{GS} = V_{DS} = -5V$
			2.0	4.0	Ω	$V_{GS} = -2V, I_{D} = -50mA$
R <sub>DS(ON)</sub>	Static Drain-to-Source ON-State Resistance		1.7	2.0	]	V <sub>GS</sub> = -3V, I <sub>D</sub> = -150mA
			1.3	1.5		V <sub>GS</sub> = -5V, I <sub>D</sub> = -300mA
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with temperature			0.75	%/°C	V <sub>GS</sub> = -5V, I <sub>D</sub> = -300mA
$G_{FS}$	Forward Transconductance	500	700		mછ	V <sub>DS</sub> = -15V, I <sub>D</sub> = -1A
C <sub>ISS</sub>	Input Capacitance		120	250		
C <sub>OSS</sub>	Common Source Output Capacitance		100	125	pF	$V_{GS} = 0V$ , $V_{DS} = -15V$ , f = 1MHz
C <sub>RSS</sub>	Reverse Transfer Capacitance		40	60		
t <sub>d(ON)</sub>	Turn-ON Delay Time			20	ns	
t <sub>r</sub>	Rise Time			20		V <sub>DD</sub> =-15V, I <sub>D</sub> = -1.25A,
t <sub>d(OFF)</sub>	Turn-OFF Delay Time			30		$R_{GEN} = 25\Omega$
t <sub>f</sub>	Fall Time			30		
V <sub>SD</sub>	Diode Forward Voltage Drop		-1.2	-1.5	V	V <sub>GS</sub> = 0V, I <sub>SD</sub> = -500mA

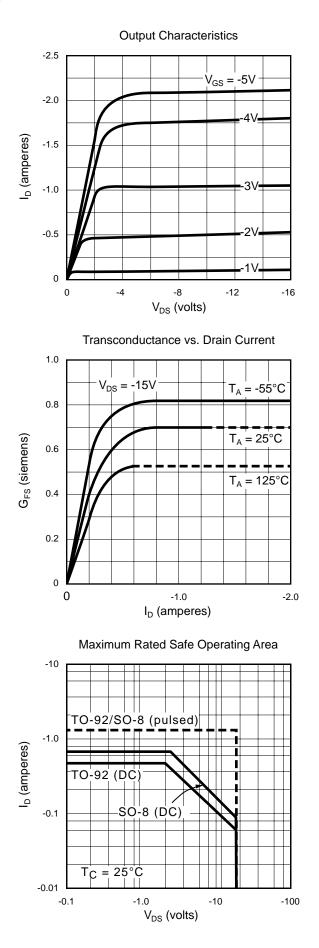
Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)

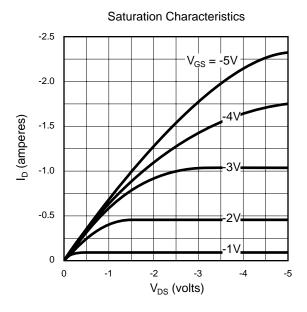
Note 2: All A.C. parameters sample tested.

## **Switching Waveforms and Test Circuit**

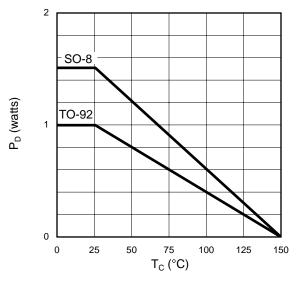


#### **Typical Performance Curves**

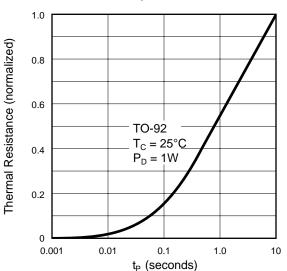




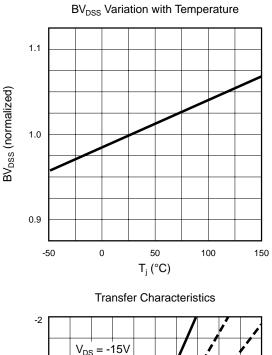
Power Dissipation vs. Case Temperature

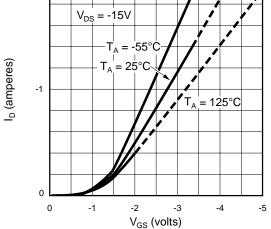


Thermal Response Characteristics

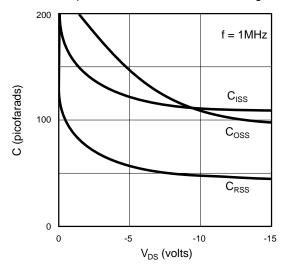


## **Typical Performance Curves**





Capacitance vs. Drain-to-Source Voltage





On-Resistance vs. Drain Current 10  $V_{GS} = -2V$ 8  $V_{GS} = -3V$  $V_{GS} = -5V$ R<sub>DS(ON)</sub> (ohms) 6 4 2 0 0 -1 -3 -2 I<sub>D</sub> (amperes)  $V_{(th)}$  and  $R_{DS}$  Variation with Temperature 1.6 1.4 V<sub>(th)</sub> @ -1mA 1.2 1.4 R<sub>DS(ON)</sub> (normalized) V<sub>GS(th)</sub> (normalized) 1.2 1.0 1.0 0.8 R<sub>DS(ON)</sub> @ -5V, -300mÅ 0.6 0.8 0.4 0.6 -50 0 50 100 150 T<sub>j</sub> (°C) Gate Drive Dynamic Characteristics -10  $V_{DS} = -10V$ -8 ·20 V V<sub>GS</sub> (volts) -6 238pF -4 -2  $C_{ISS} = 115 pF$ 

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Q<sub>G</sub> (nanocoulombs)

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