



New Product

Si7374DP

Vishay Siliconix

N-Channel 30-V (D-S) MOSFET with Schottky Diode

PRODUCT SUMMARY			
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A) ^a	Q_g (Typ)
30	0.0055 at $V_{GS} = 10$ V	24	36 nC
	0.0066 at $V_{GS} = 4.5$ V	24	

SCHOTTKY PRODUCT SUMMARY		
V_{DS} (V)	V_{SD} (V) Diode Forward Voltage	I_F (A)
30	0.39 V at 1.0 A	2.0

FEATURES

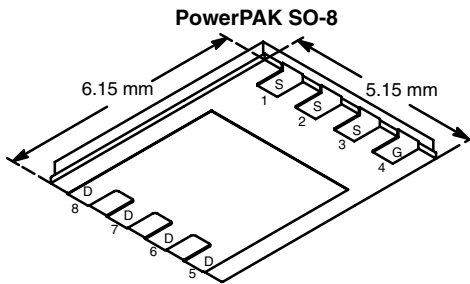
- TrenchFET® PowerMOSFET
- 100 % R_g Tested

APPLICATIONS

- DC/DC Conversion
 - CPU core low side
 - Secondary synchronous rectification

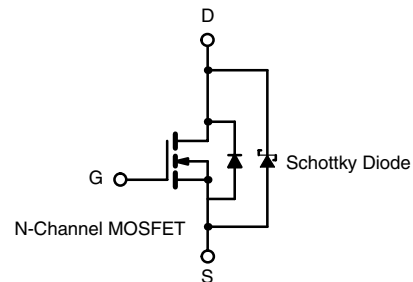


RoHS COMPLIANT



Bottom View

Ordering Information: Si7374DP-T1-E3 (Lead (Pb)-free)



ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C UNLESS OTHERWISE NOTED)			
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ($T_J = 150$ °C)	I_D	$T_C = 25$ °C	24 ^a
		$T_C = 70$ °C	24 ^a
		$T_A = 25$ °C	23.8 ^{b, c}
		$T_A = 70$ °C	19 ^{b, c}
Pulsed Drain Current	I_{DM}	100	A
Continuous Source-Drain Diode Current	I_S	$T_C = 25$ °C	
		$T_A = 25$ °C	4.2 ^{b, c}
Maximum Power Dissipation	P_D	$T_C = 25$ °C	56
		$T_C = 70$ °C	36
		$T_A = 25$ °C	5 ^{b, c}
		$T_A = 70$ °C	3.2 ^{b, c}
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS				
Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, d}	R_{thJA}	20	25	°C/W
Maximum Junction-to-Case (Drain)				

Notes:

- Based on $T_C = 25$ °C.
- Surface mounted on 1" x 1" FR4 board.
- $t = 10$ sec.
- See Solder Profile (<http://www.vishay.com/doc?73461>). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under steady state conditions is 68 °C/W.

SPECIFICATIONS (T _J = 25 °C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 1 mA	30			V
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1.5		2.8	V
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V			500	μA
		V _{DS} = 30 V, V _{GS} = 0 V, T _J = 55 °C			10	mA
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	50			A
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = 10 V, I _D = 23.8 A		0.0046	0.0055	Ω
		V _{GS} = 4.5 V, I _D = 21.8 A		0.0055	0.0066	
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 23.8 A		95		S
Dynamic^b						
Input Capacitance	C _{iss}	V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHz		5500		pF
Output Capacitance	C _{oss}			870		
Reverse Transfer Capacitance	C _{rss}			360		
Total Gate Charge	Q _g	V _{DS} = 15 V, V _{GS} = 10 V, I _D = 20 A		81	122	nC
Gate-Source Charge	Q _{gs}	V _{DS} = 15 V, V _{GS} = 4.5 V, I _D = 20 A		38	57	
Gate-Drain Charge	Q _{gd}			18		
Gate Resistance	R _g		f = 1 MHz		0.95	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 15 V, R _L = 1.5 Ω I _D ≅ 10 A, V _{GEN} = 4.5 V, R _g = 1 Ω		40	60	ns
Rise Time	t _r			160	240	
Turn-Off Delay Time	t _{d(off)}			30	45	
Fall Time	t _f			10	15	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 15 V, R _L = 1.5 Ω I _D ≅ 10 A, V _{GEN} = 10 V, R _g = 1 Ω		15	25	
Rise Time	t _r			15	25	
Turn-Off Delay Time	t _{d(off)}			42	65	
Fall Time	t _f			10	15	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Current	I _S	T _C = 25 °C			24	A
Pulse Forward Diode Current	I _{SM}				100	
Forward Voltage Drop (Schottky Diode)	V _F	I _F = 1 A		0.35	0.39	V
		I _F = 1 A, T _J = 150 °C		0.27	0.31	
Maximal Reverse Leakage Current (Schottky Diode)	I _{rm}	V _r = 30 V		0.07	0.5	mA
		V _r = 30 V, T _J = 100 °C		3.5	10	
		V _r = 30 V, T _J = 125 °C		10	100	
Junction Capacitance (Schottky Diode)	C _T	V _r = 10 V		58		pF
Body Diode Reverse Recovery Time	t _{rr}	I _F = 10 A, di/dt = 100 A/μs, T _J = 25 °C		45	70	ns
Body Diode Reverse Recovery Charge	Q _{rr}			39	60	nC
Reverse Recovery Fall Time	t _a			20		ns
Reverse Recovery Rise Time	t _b			25		

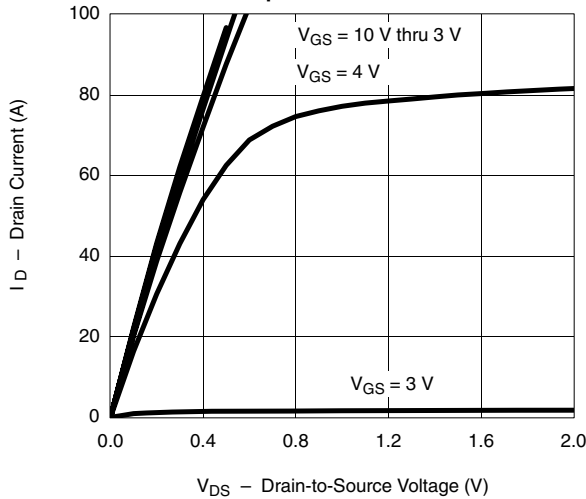
Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

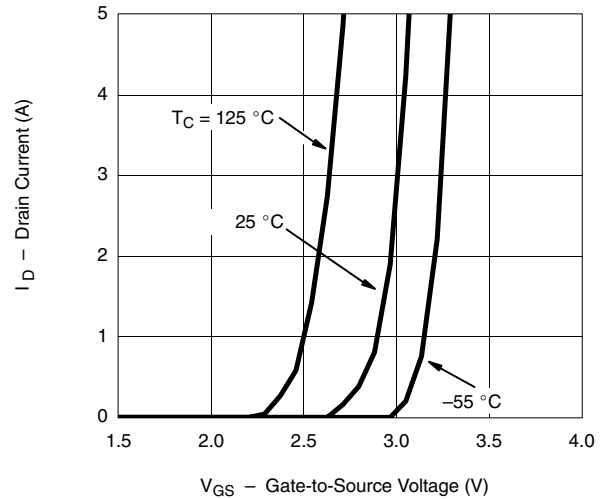
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)

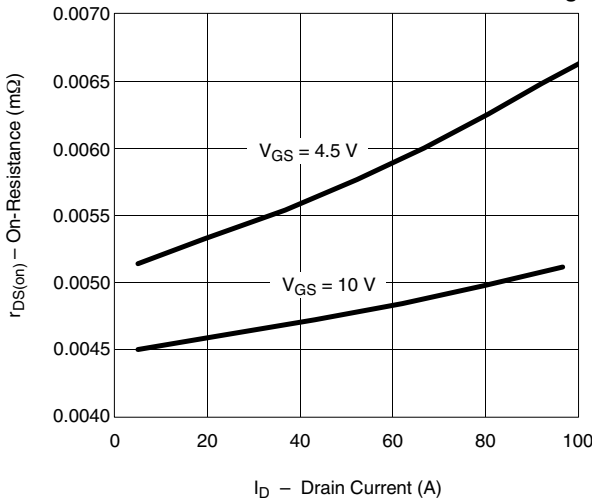
Output Characteristics



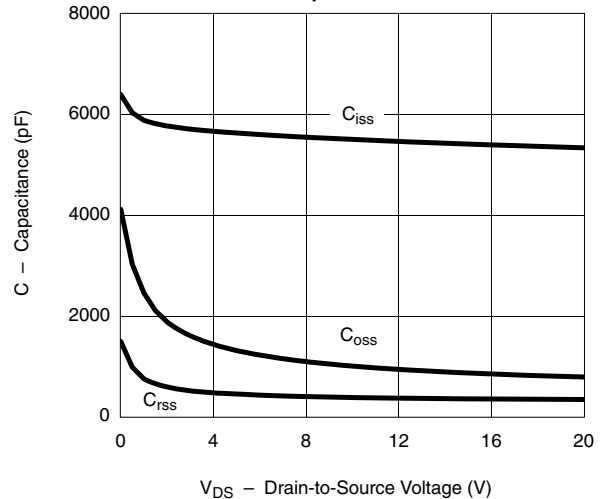
Transfer Characteristics



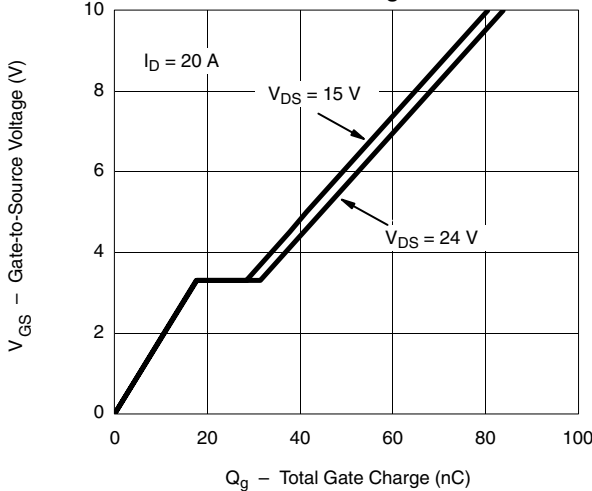
On-Resistance vs. Drain Current and Gate Voltage



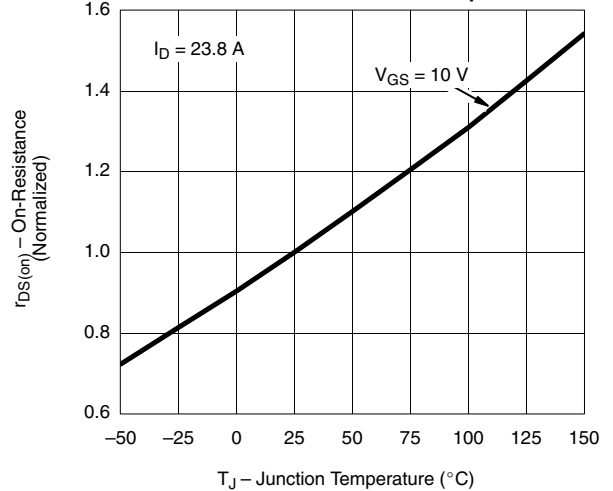
Capacitance



Gate Charge



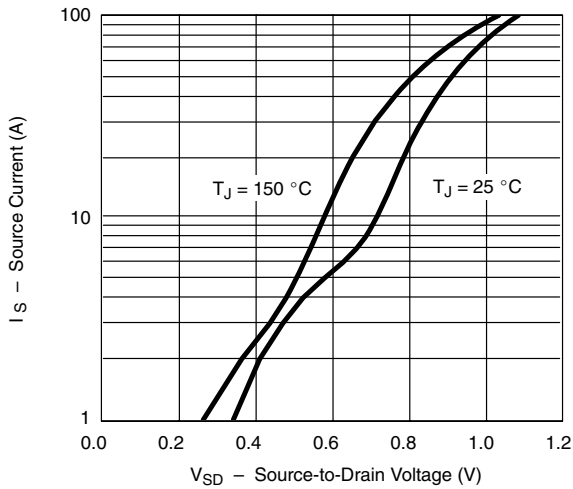
On-Resistance vs. Junction Temperature



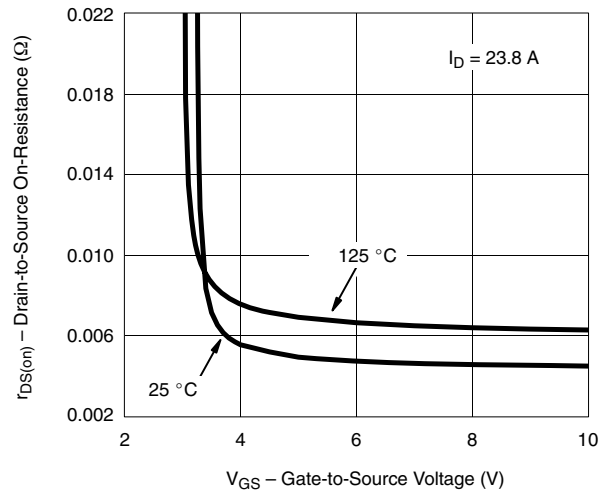


TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)

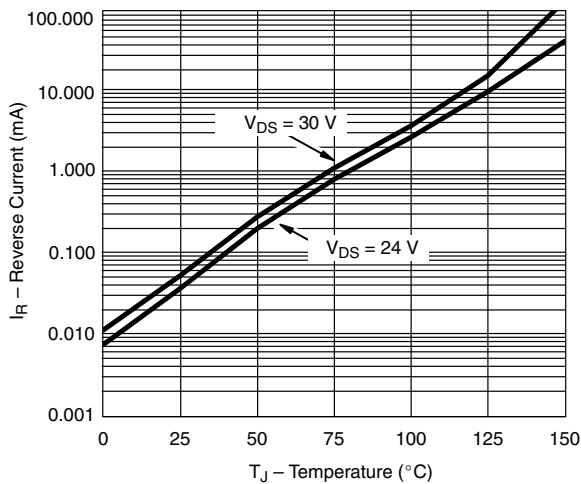
Source-Drain Diode Forward Voltage



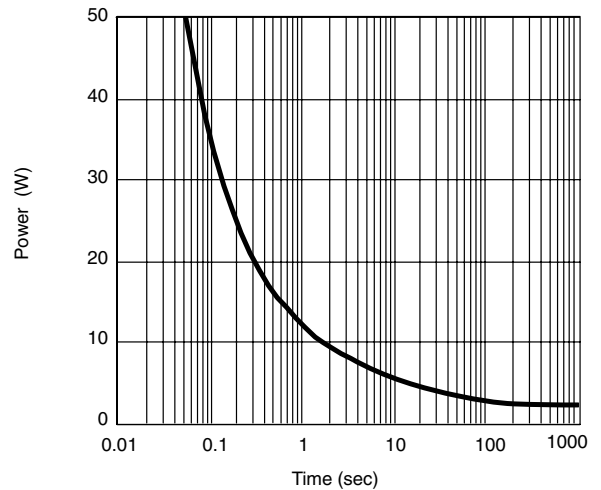
On-Resistance vs. Gate-to-Source Voltage



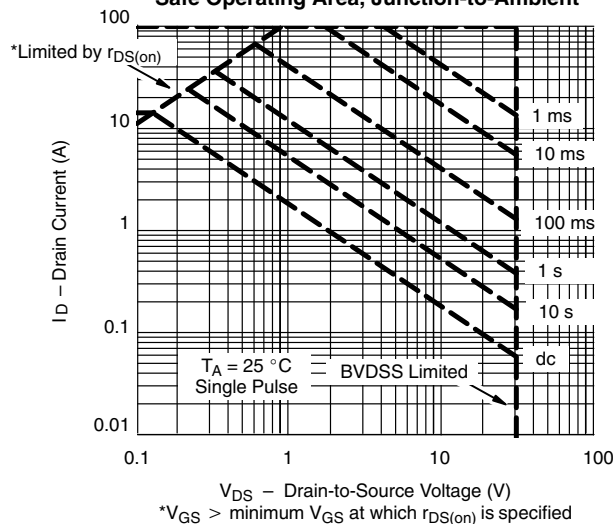
Threshold Voltage



Single Pulse Power

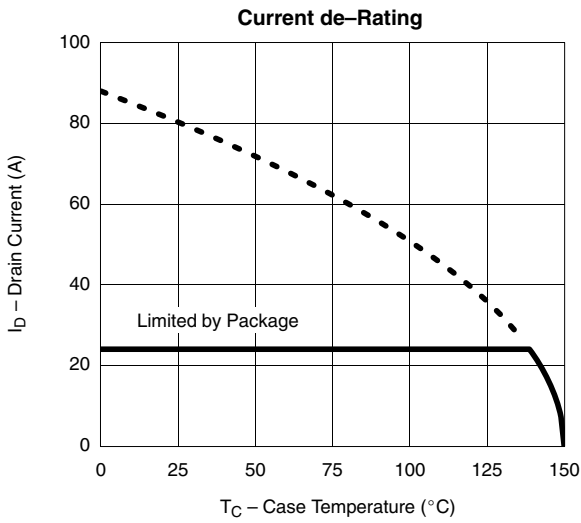


Safe Operating Area, Junction-to-Ambient





TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)

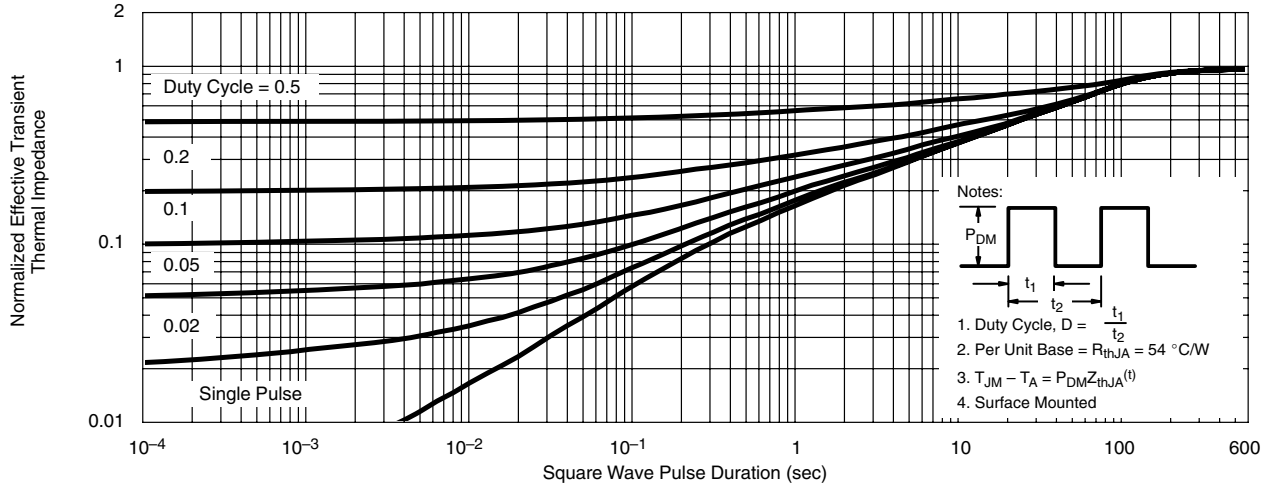


*The power dissipation P_D is based on $T_{J(max)} = 150\text{ }^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

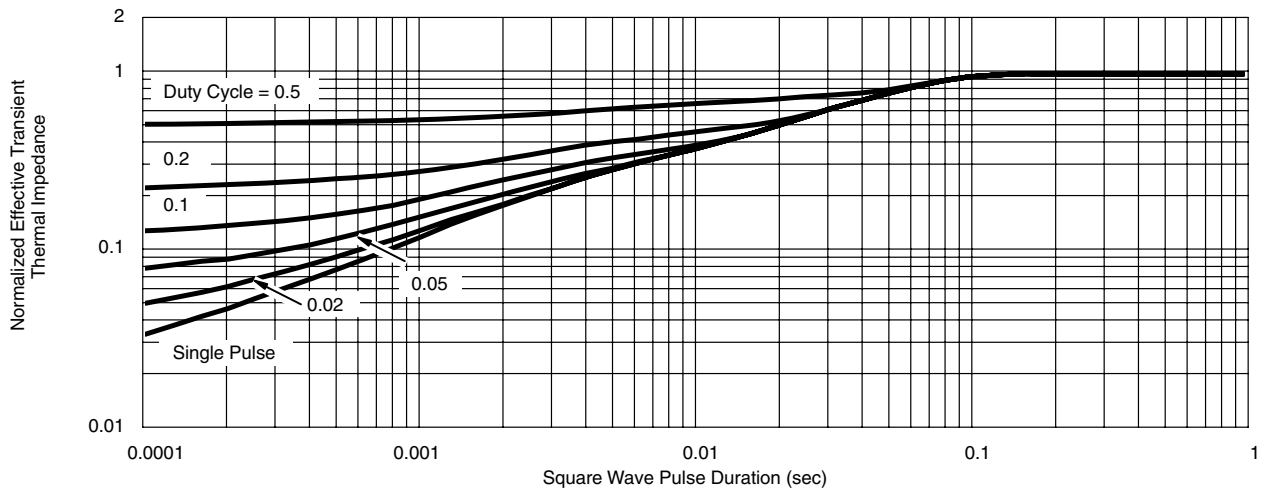


TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)

Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?73560>.



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