

N-Channel 150-V (D-S) MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
150	0.050 at $V_{GS} = 10$ V	6.7

FEATURES

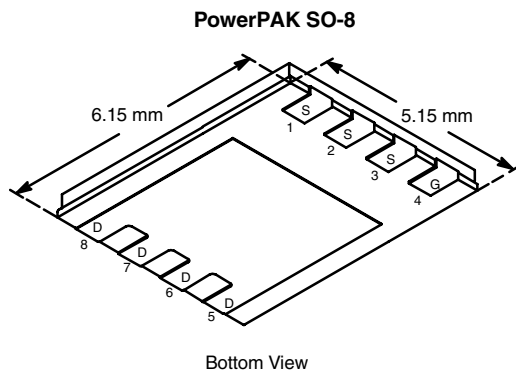
- TrenchFET[®] Power MOSFETS
- New Low Thermal Resistance PowerPAK[®] Package with Low 1.07-mm Profile
- PWM Optimized for Fast Switching
- 100 % R_g Tested



RoHS*
COMPLIANT

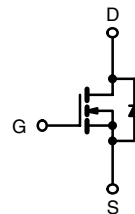
APPLICATIONS

- Primary Side Switch for High Density DC/DC
- Telecom/Server 48-V DC/DC
- Industrial and 42-V Automotive



Bottom View

Ordering Information: Si7846DP-T1
Si7846DP-T1—E3 (Lead (Pb)-free)



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS $T_A = 25$ °C, unless otherwise noted				
Parameter	Symbol	10 secs	Steady State	Unit
Drain-Source Voltage	V_{DS}	150		V
Gate-Source Voltage	V_{GS}	± 20		
Continuous Drain Current ($T_J = 150$ °C) ^a	I_D	$T_C = 25$ °C		A
		$T_C = 70$ °C		
		6.7	4.0	
		5.4	3.3	
Pulsed Drain Current	I_{DM}	50		A
Avalanche Current	I_{AS}	25		
Continuous Source Current (Diode Conduction) ^a	I_S	4.3	1.6	W
Maximum Power Dissipation ^a	P_D	$T_A = 25$ °C	5.2	
		$T_A = 70$ °C	3.3	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	– 55 to 150		°C
Soldering Recommendations (Peak Temperature) ^{b,c}		260		

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^a	R_{thJA}	$t \leq 10$ sec	19	24	°C/W
		Steady State	52	65	
Maximum Junction-to-Case (Drain)	R_{thJC}	1.5	1.8		

Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
b. See Solder Profile (<http://www.vishay.com/ppg?73257>). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
c. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

* Pb containing terminations are not RoHS compliant, exemptions may apply.

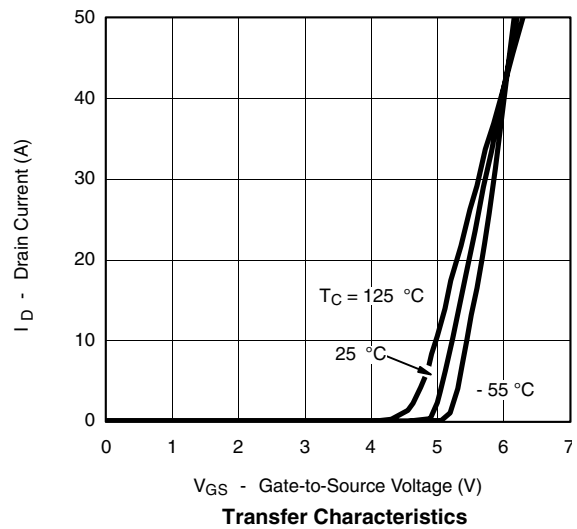
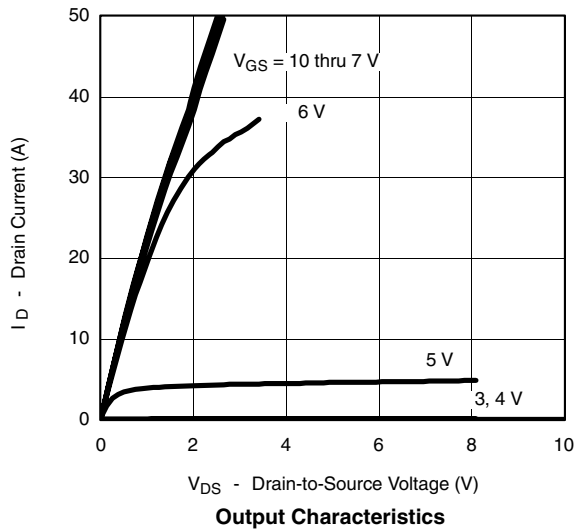
SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.0		4.5	V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 150\text{ V}, V_{GS} = 0\text{ V}$			1	μA
		$V_{DS} = 150\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$			5	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	50			A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 5\text{ A}$		0.041	0.050	Ω
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15\text{ V}, I_D = 5\text{ A}$		18		S
Diode Forward Voltage ^a	V_{SD}	$I_S = 2.8\text{ A}, V_{GS} = 0\text{ V}$		0.75	1.1	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = 75\text{ V}, V_{GS} = 10\text{ V}, I_D = 5\text{ A}$		30	36	nC
Gate-Source Charge	Q_{gs}		8.5			
Gate-Drain Charge	Q_{gd}		8.5			
Gate Resistance	R_g		0.2	0.85	1.4	Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 75\text{ V}, R_L = 15\text{ }\Omega$ $I_D \approx 5\text{ A}, V_{GEN} = 10\text{ V}, R_G = 6\text{ }\Omega$		12	18	ns
Rise Time	t_r		7	11		
Turn-Off Delay Time	$t_{d(off)}$		22	33		
Fall Time	t_f		10	15		
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 2.8\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		40	70	

Notes

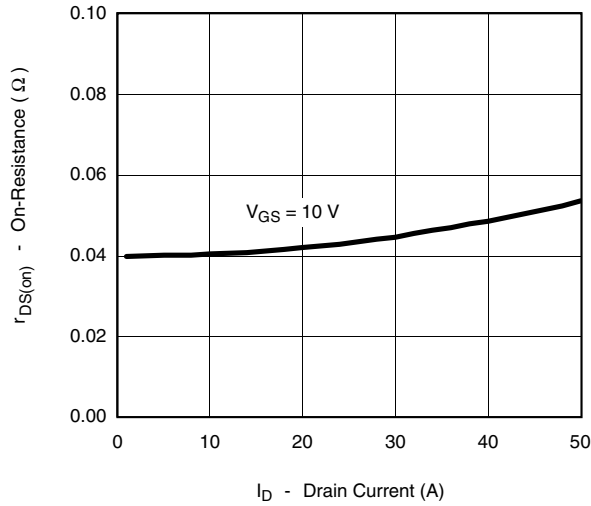
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

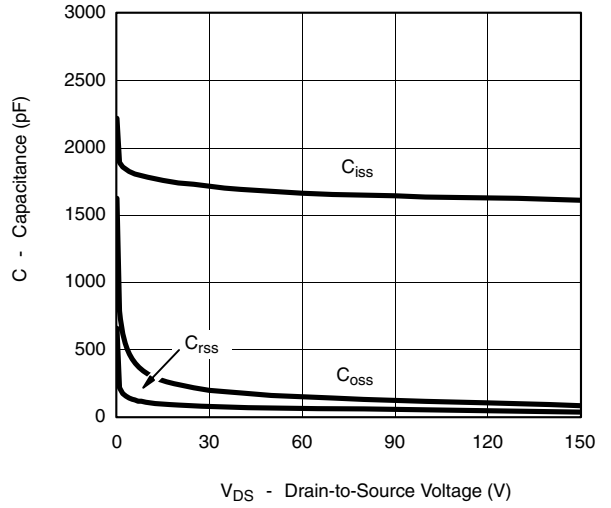
TYPICAL CHARACTERISTICS $25\text{ }^\circ\text{C}$, unless noted



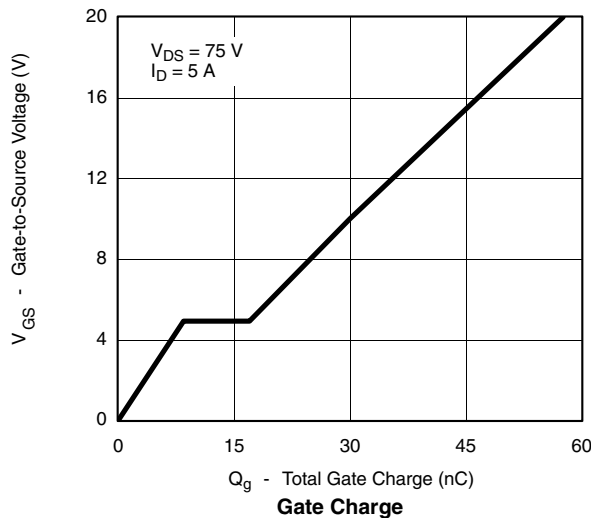
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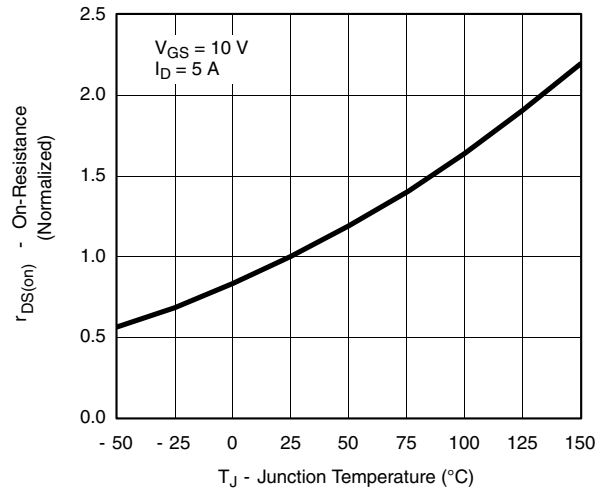
On-Resistance vs. Drain Current



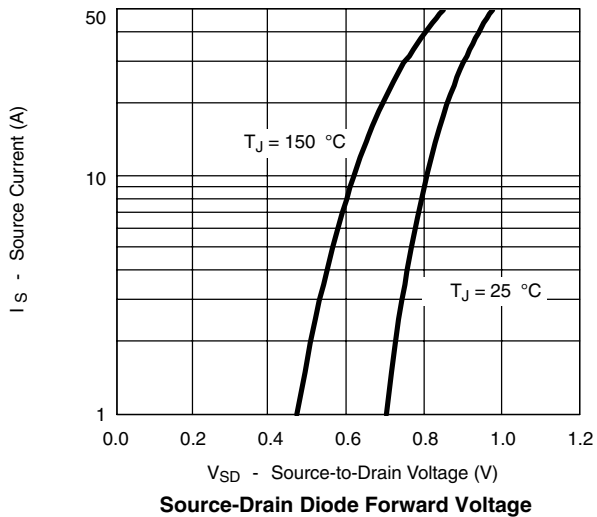
Capacitance



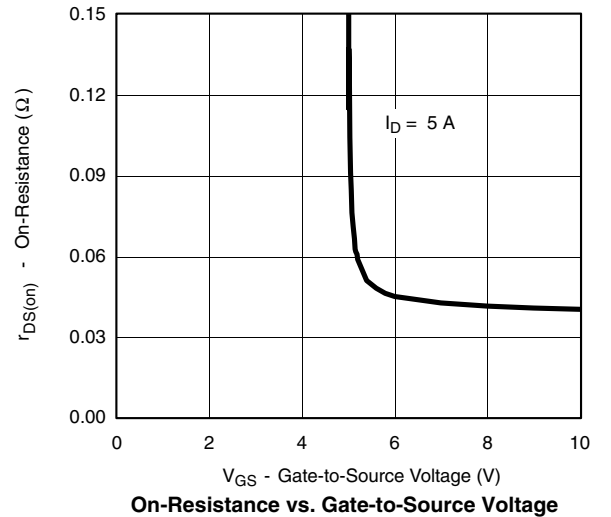
Gate Charge



On-Resistance vs. Junction Temperature

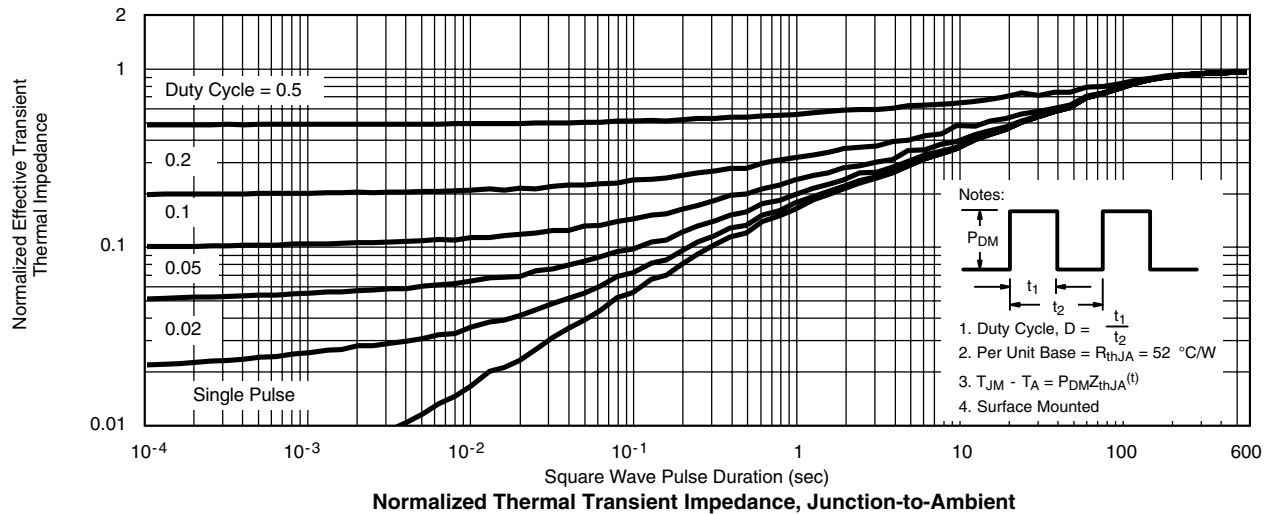
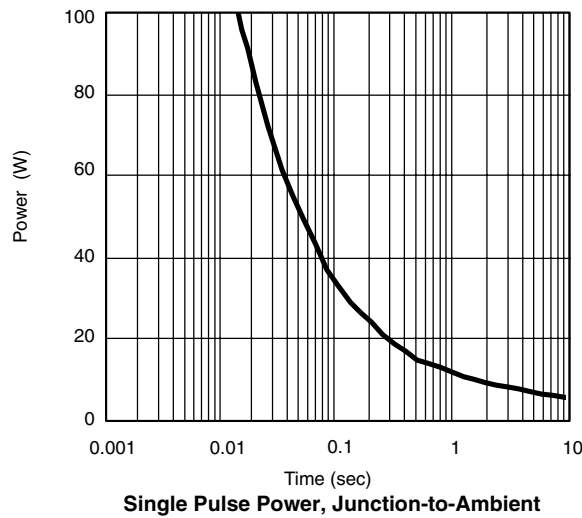
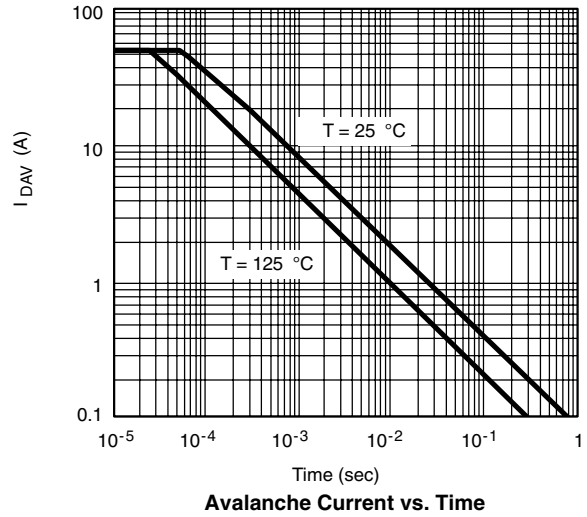
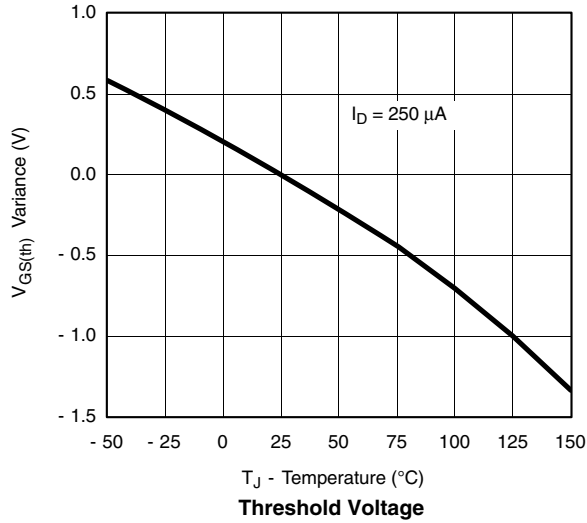


Source-Drain Diode Forward Voltage

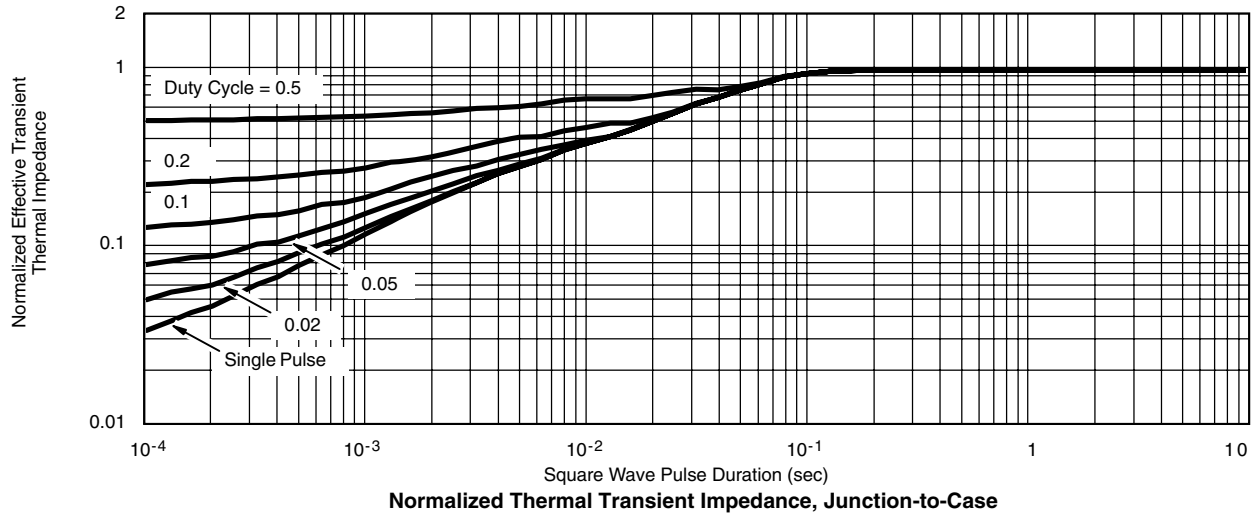


On-Resistance vs. Gate-to-Source Voltage

TYPICAL CHARACTERISTICS 25 °C, unless noted



TYPICAL CHARACTERISTICS 25 °C, unless noted



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