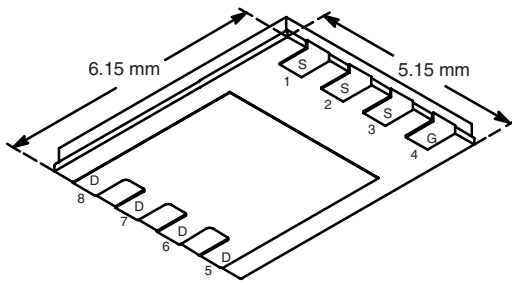


N-Channel 40-V (D-S) MOSFET

PRODUCT SUMMARY			
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A) ^f	Q _g (Typ.)
40	0.009 at V _{GS} = 10 V	47	15 nC
	0.012 at V _{GS} = 4.5 V	40	

PowerPAK SO-8



Bottom View

Ordering Information: Si7848BDP-T1-E3 (Lead (Pb)-free)
Si7848BDP-T1-GE3 (Lead (Pb)-free and Halogen-free)

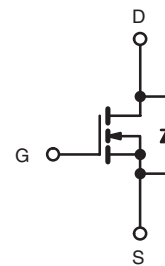
FEATURES

- Halogen-free available
- TrenchFET[®] Power MOSFET
- 100 % R_g and UIS Tested



APPLICATIONS

- DC/DC Converters
 - Synchronous Buck
 - Synchronous Rectifier



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted				
Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V _{DS}	40	V	
Gate-Source Voltage	V _{GS}	± 20		
Continuous Drain Current (T _J = 150 °C)	I _D	T _C = 25 °C	47	A
		T _C = 70 °C	38	
		T _A = 25 °C	16 ^{a, b}	
		T _A = 70 °C	12.8 ^{a, b}	
Pulsed Drain Current	I _{DM}	50		
Avalanche Current	L = 0.1 mH	I _{AS}	15	mJ
Avalanche Energy		E _{AS}	11	
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C	30	A
		T _A = 25 °C	3.5 ^{a, b}	
Maximum Power Dissipation	P _D	T _C = 25 °C	36	W
		T _C = 70 °C	23	
		T _A = 25 °C	4.2 ^{a, b}	
		T _A = 70 °C	2.7 ^{a, b}	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150	°C	
Soldering Recommendations (Peak Temperature) ^{c, d}		260		

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^{a, e}	t ≤ 10 s	R _{thJA}	25	30	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R _{thJC}	2.9	3.5	

Notes:

- Surface Mounted on 1" x 1" FR4 board.
- t = 10 s.
- See Solder Profile (<http://www.vishay.com/ppg?73257>). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under Steady State conditions is 70 °C/W.
- Based on T_C = 25 °C.

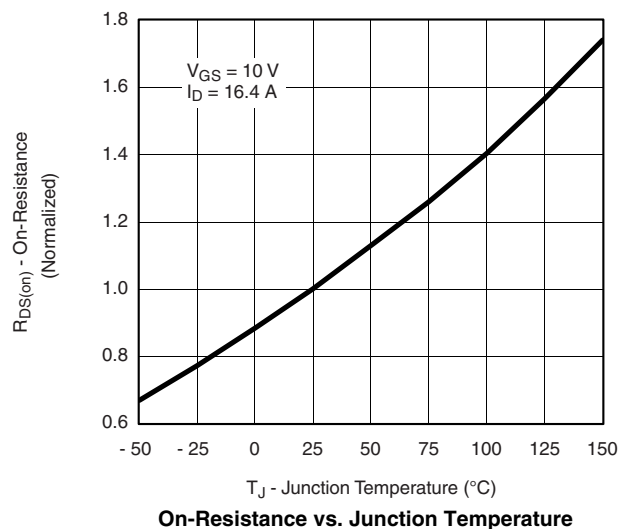
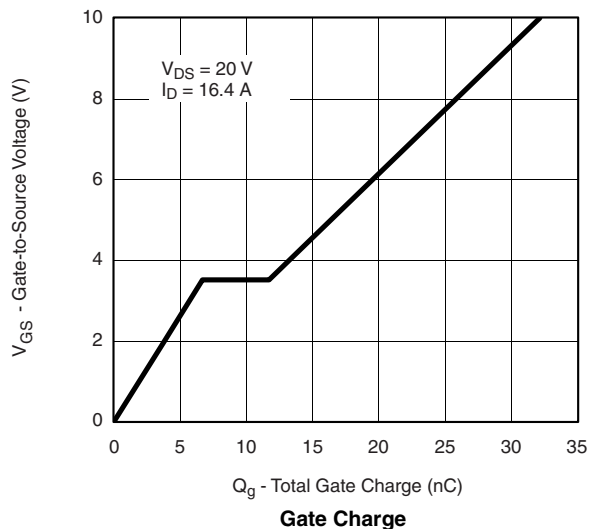
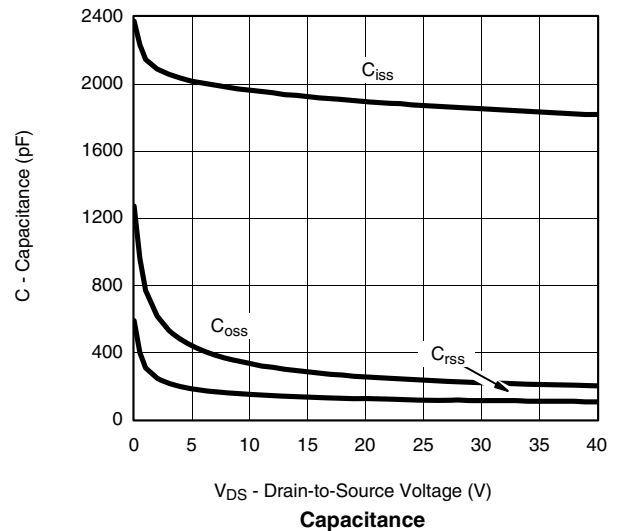
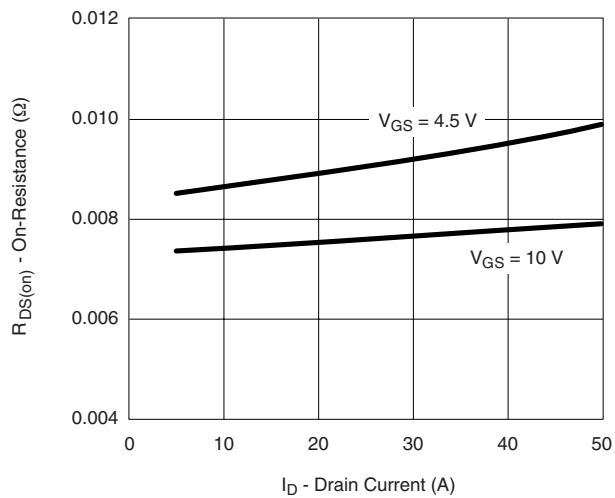
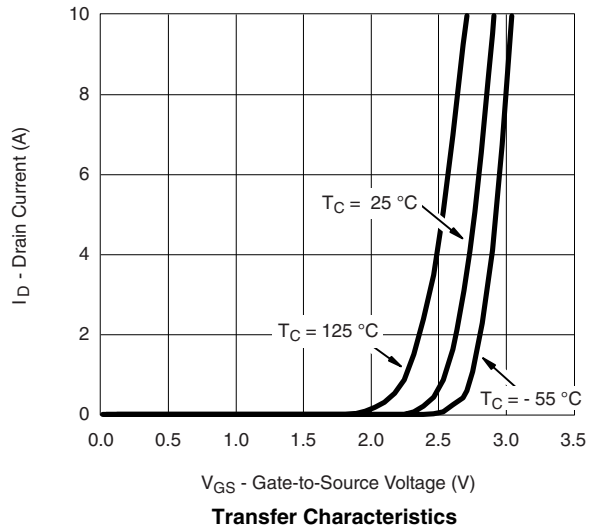
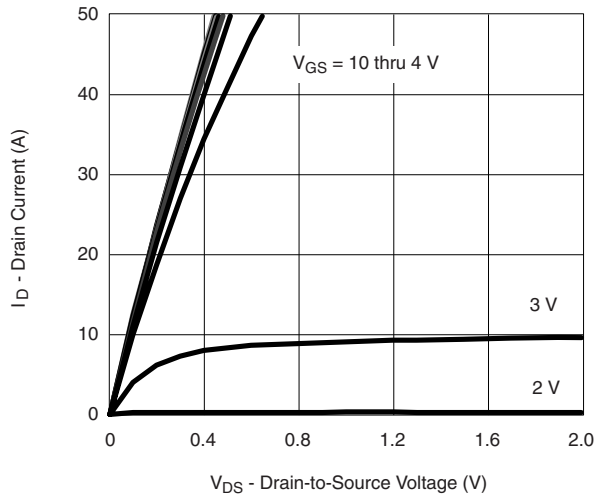
SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted							
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	40			V	
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$		40		mV/ $^\circ\text{C}$	
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			-6			
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1		3	V	
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V}$			1	μA	
		$V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$			5		
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	50			A	
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 16\text{ A}$		0.0074	0.009	Ω	
		$V_{GS} = 4.5\text{ V}, I_D = 13.8\text{ A}$		0.0095	0.012		
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15\text{ V}, I_D = 16\text{ A}$		56		S	
Dynamic^b							
Input Capacitance	C_{iss}	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		2000		pF	
Output Capacitance	C_{oss}				260		
Reverse Transfer Capacitance	C_{rss}				150		
Total Gate Charge	Q_g	$V_{DS} = 10\text{ V}, V_{GS} = 10\text{ V}, I_D = 16\text{ A}$		33	50	nC	
		$V_{DS} = 10\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 16\text{ A}$		15	23		
Gate-Source Charge	Q_{gs}			6.7			
Gate-Drain Charge	Q_{gd}		5.1				
Gate Resistance	R_g	$f = 1\text{ MHz}$		1.4	2.1	Ω	
Turn-on Delay Time	$t_{d(on)}$	$V_{DD} = 20\text{ V}, R_L = 2\text{ }\Omega$ $I_D \cong 10\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 1\text{ }\Omega$		30	45	ns	
Rise Time	t_r			150	225		
Turn-Off Delay Time	$t_{d(off)}$			30	45		
Fall Time	t_f			40	60		
Turn-on Delay Time	$t_{d(on)}$	$V_{DD} = 20\text{ V}, R_L = 2\text{ }\Omega$ $I_D \cong 10\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$		10	15		
Rise Time	t_r			15	25		
Turn-Off Delay Time	$t_{d(off)}$			30	45		
Fall Time	t_f			10	15		
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^\circ\text{C}$			30	A	
Pulse Diode Forward Current	I_{SM}				50		
Body Diode Voltage	V_{SD}	$I_S = 10\text{ A}, V_{GS} = 0\text{ V}$		0.8	1.2	V	
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 10\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$		30	60	ns	
Body Diode Reverse Recovery Charge	Q_{rr}			26	52	nC	
Reverse Recovery Fall Time	t_a			17.5		ns	
Reverse Recovery Rise Time	t_b			12.5			

Notes:

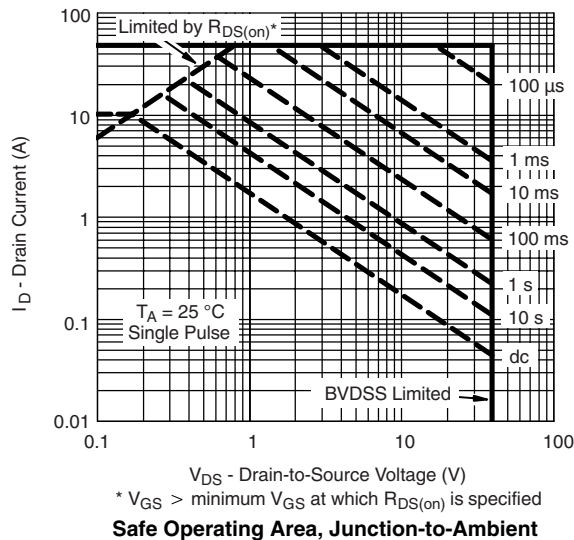
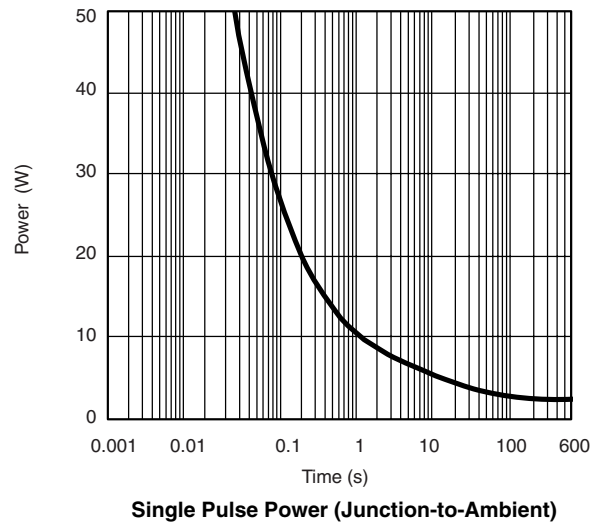
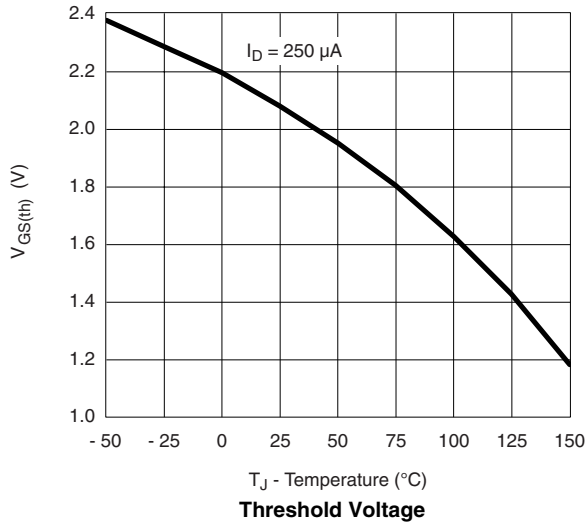
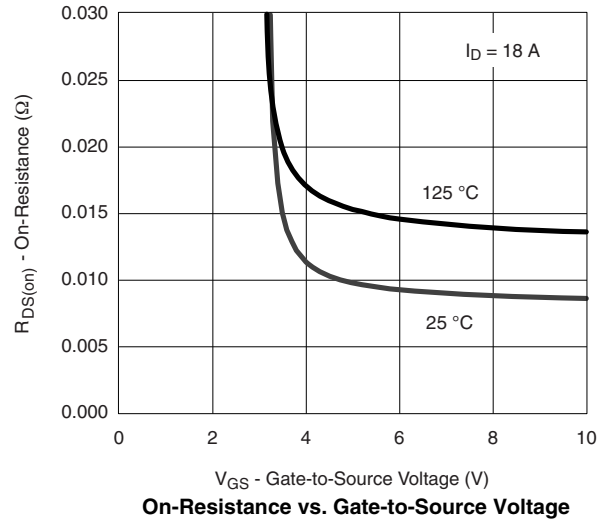
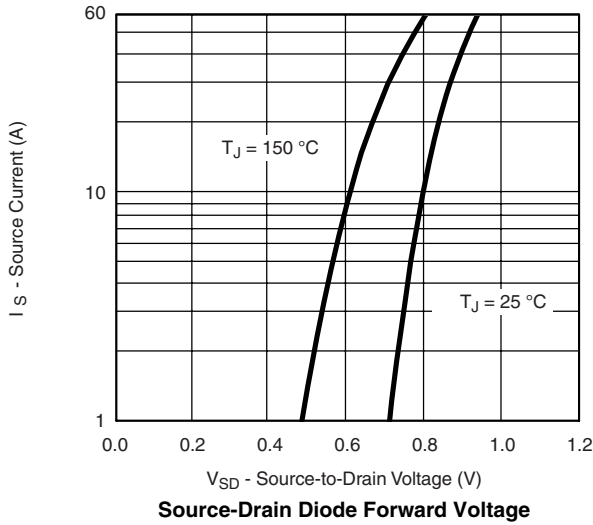
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

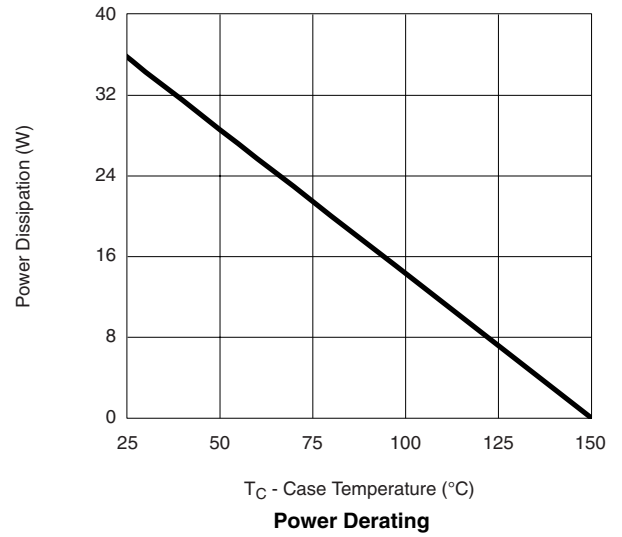
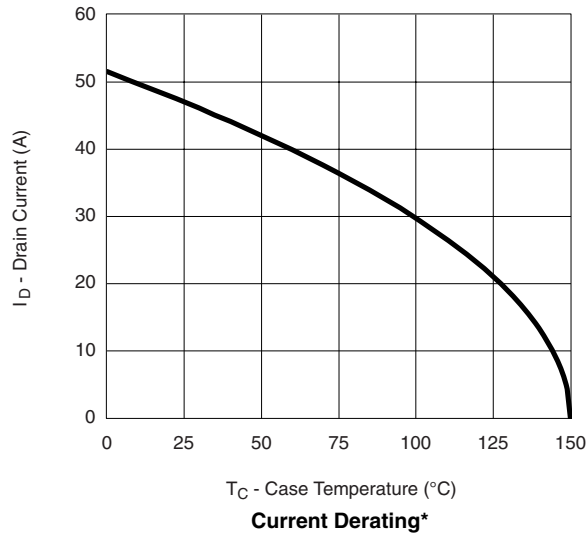
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

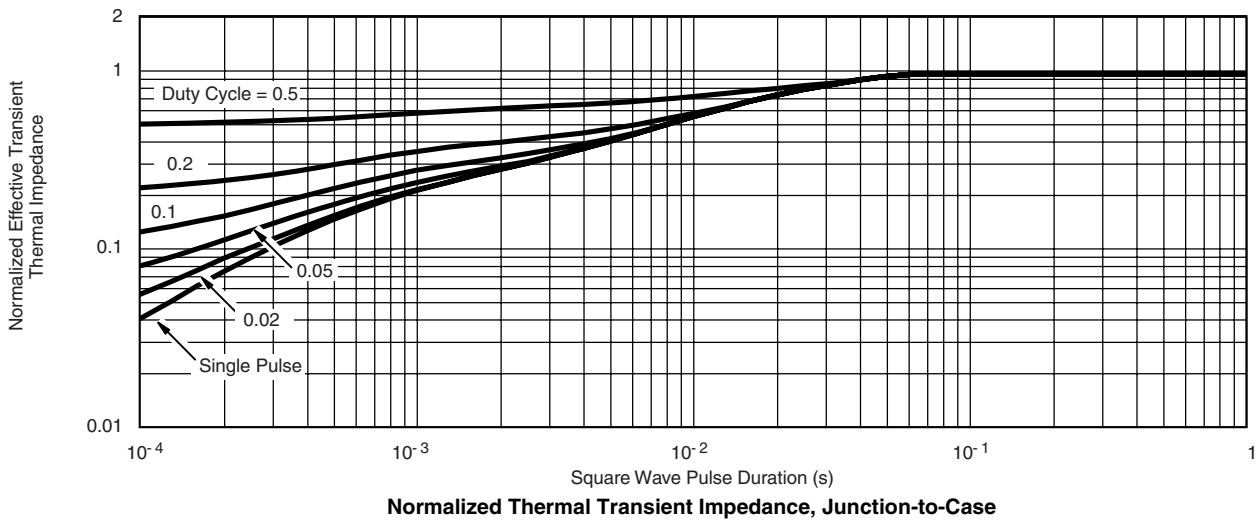
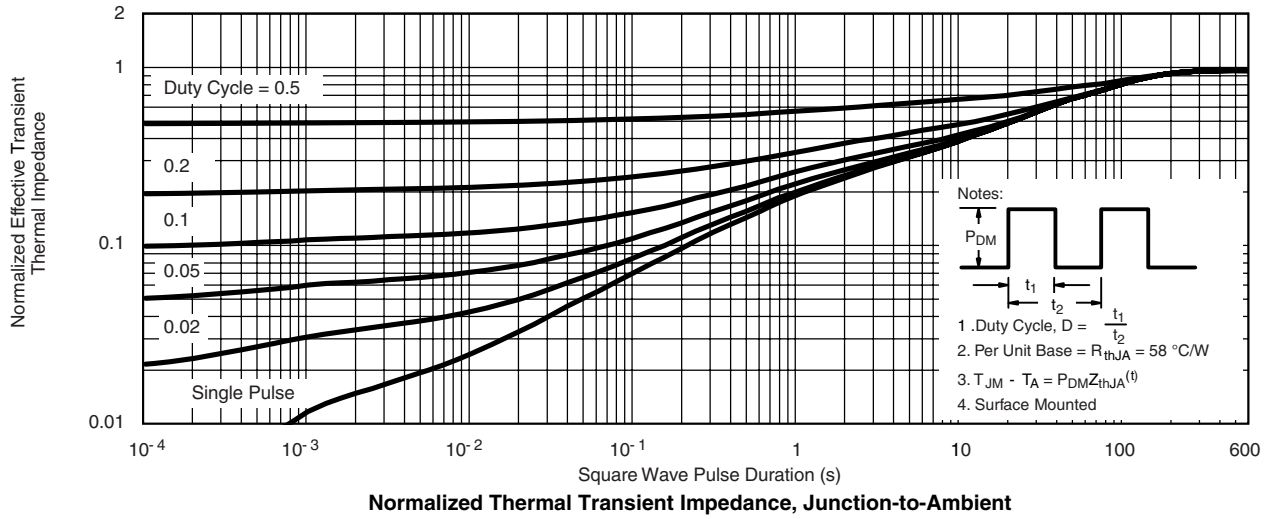


TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?74632>.



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