

N-Channel Reduced Q_g , Fast Switching MOSFET

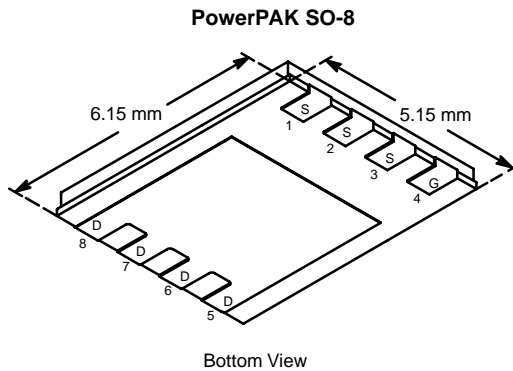
PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
30	0.0095 @ $V_{GS} = 10$ V	16
	0.0125 @ $V_{GS} = 4.5$ V	16

FEATURES

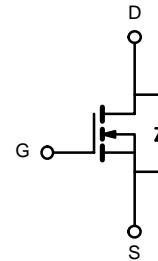
- TrenchFET® Power MOSFET
- PWM Optimized for High Efficiency
- New Low Thermal Resistance PowerPAK® Package with Low 1.07-mm Profile
- 100% R_g Tested

APPLICATIONS

- Buck Converter
 - High Side or Low Side
- Synchronous Rectifier
 - Secondary Rectifier



Ordering Information: Si7860ADP-T1-E3



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)					
Parameter	Symbol	10 secs	Steady State	Unit	
Drain-Source Voltage	V_{DS}	30		V	
Gate-Source Voltage	V_{GS}	± 20			
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	$T_A = 25^\circ\text{C}$	16	11	A
		$T_A = 70^\circ\text{C}$	13	8	
Pulsed Drain Current	I_{DM}	± 50			
Continuous Source Current (Diode Conduction) ^a	I_S	4.1	1.5		
Maximum Power Dissipation ^a	P_D	$T_A = 25^\circ\text{C}$	4.8	1.8	W
		$T_A = 70^\circ\text{C}$	3.1	1.1	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150		$^\circ\text{C}$	

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient (MOSFET) ^a	R_{thJA}	$t \leq 10$ sec	21	26	$^\circ\text{C/W}$
		Steady State	56	70	
Maximum Junction-to-Case (Drain)	R_{thJC}	1.9	2.5		

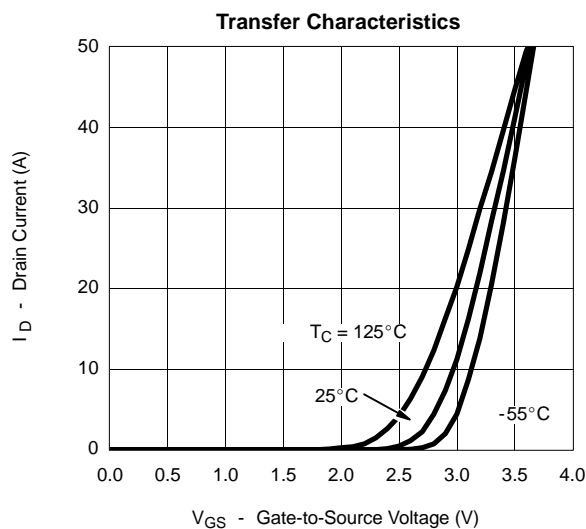
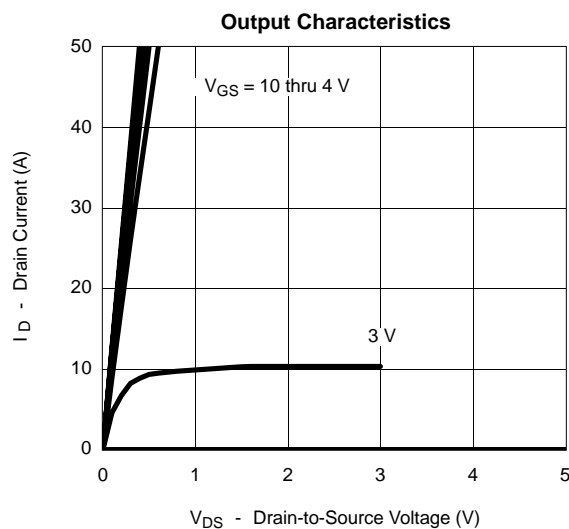
Notes

a. Surface Mounted on 1" x 1" FR4 Board.

MOSFET SPECIFICATIONS ($T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	1.0		3.0	V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}, V_{GS} = \pm 20\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 30\ \text{V}, V_{GS} = 0\ \text{V}$			1	μA
		$V_{DS} = 30\ \text{V}, V_{GS} = 0\ \text{V}, T_J = 70^\circ\text{C}$			5	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\ \text{V}, V_{GS} = 10\ \text{V}$	40			A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = 10\ \text{V}, I_D = 16\ \text{A}$		0.0079	0.0095	Ω
		$V_{GS} = 4.5\ \text{V}, I_D = 14\ \text{A}$		0.0105	0.0125	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15\ \text{V}, I_D = 16\ \text{A}$		60		S
Diode Forward Voltage ^a	V_{SD}	$I_S = 3\ \text{A}, V_{GS} = 0\ \text{V}$		0.70	1.1	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = 15\ \text{V}, V_{GS} = 4.5\ \text{V}, I_D = 16\ \text{A}$		13	18	nC
Gate-Source Charge	Q_{gs}		5			
Gate-Drain Charge	Q_{gd}		4.0			
Gate-Resistance	R_g		0.5	1.7	3.2	Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15\ \text{V}, R_L = 15\ \Omega$ $I_D \cong 1\ \text{A}, V_{GEN} = 10\ \text{V}, R_G = 6\ \Omega$		18	27	ns
Rise Time	t_r		12	18		
Turn-Off Delay Time	$t_{d(off)}$		46	70		
Fall Time	t_f		19	30		
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 3\ \text{A}, di/dt = 100\ \text{A}/\mu\text{s}$		40	70	

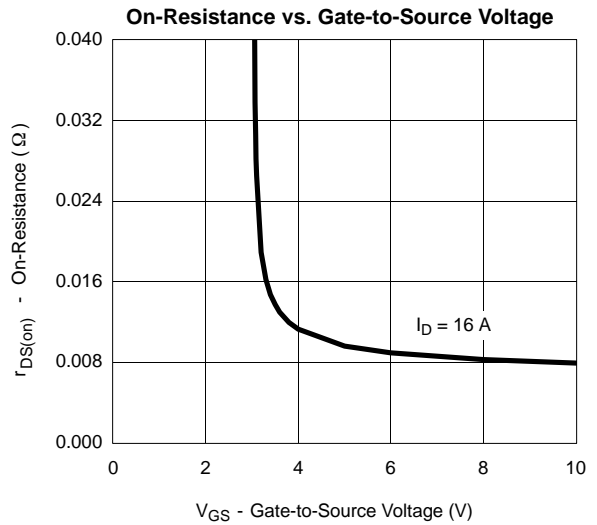
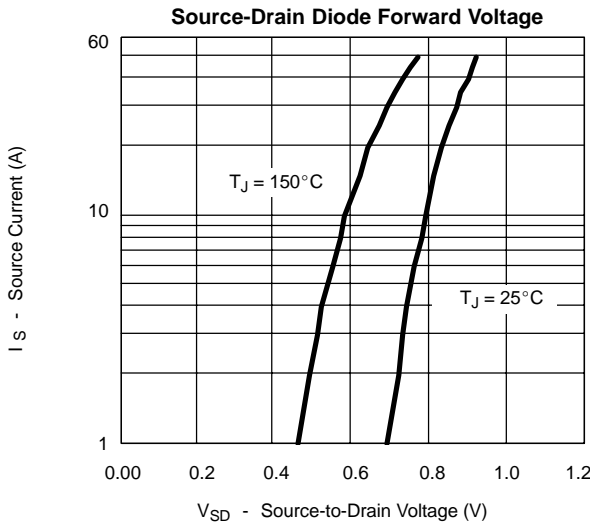
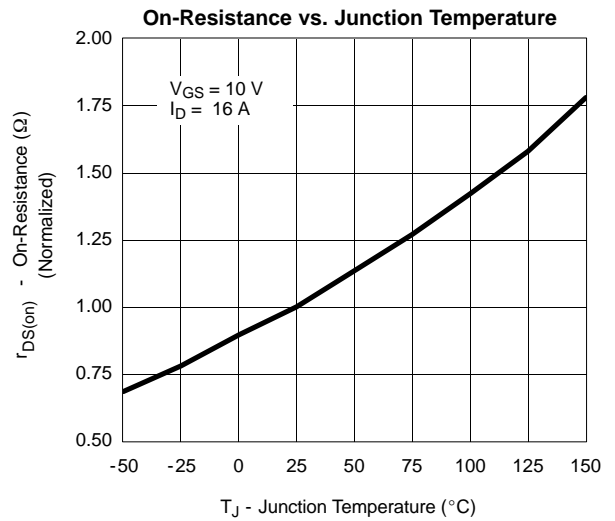
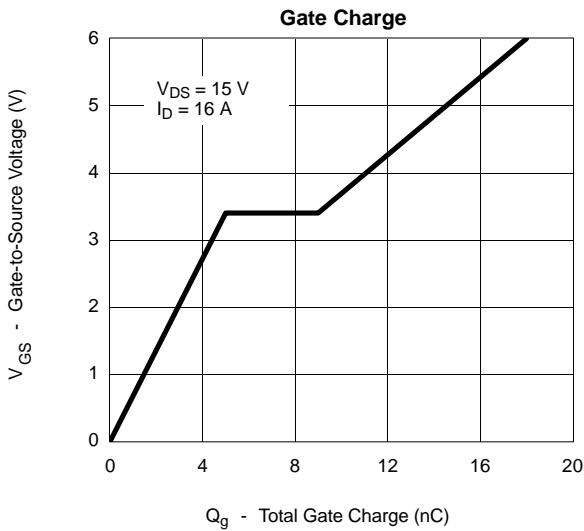
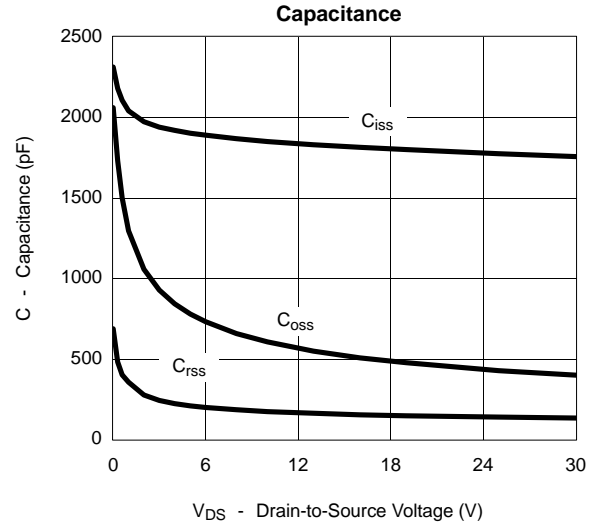
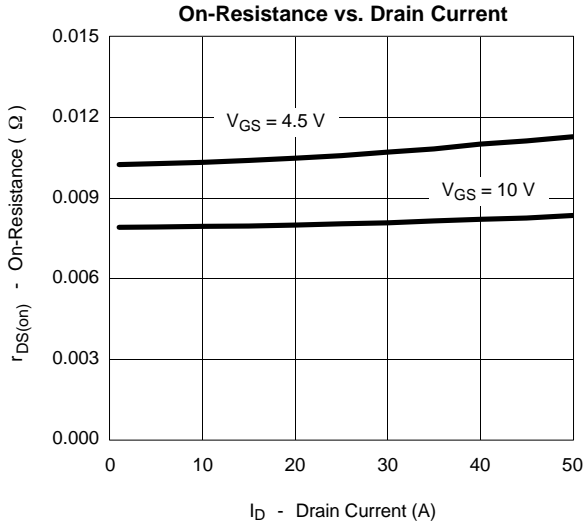
Notes

- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
 b. Guaranteed by design, not subject to production testing.

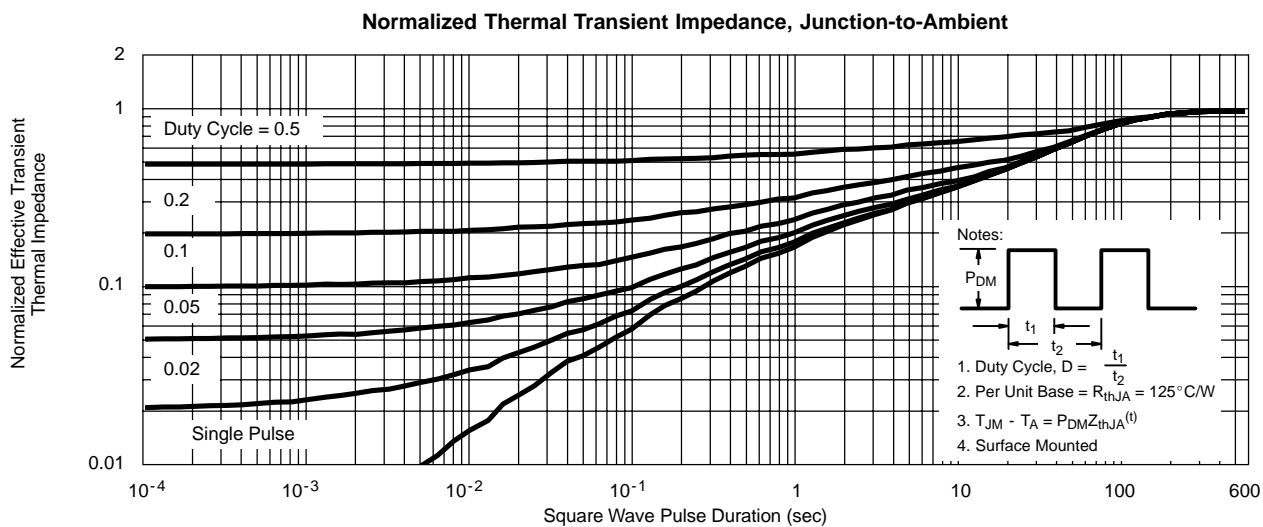
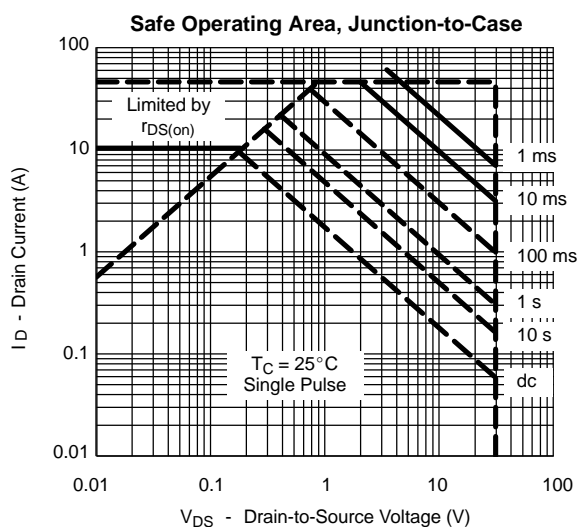
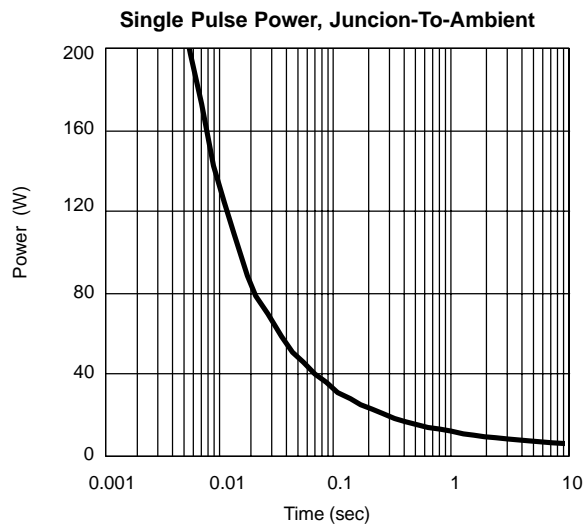
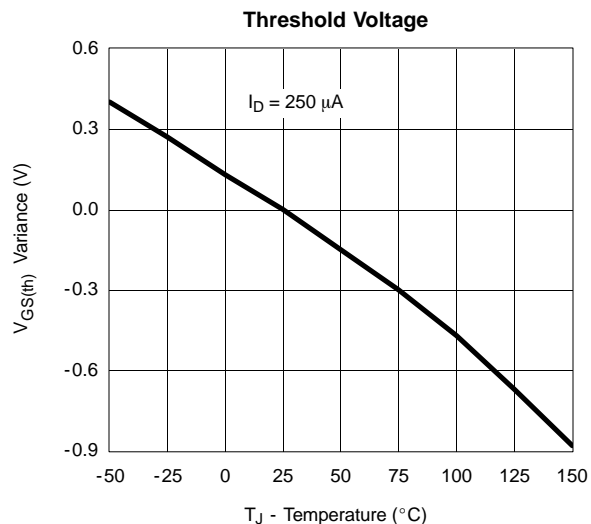
TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)




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