N-Channel 75-V (D-S) MOSFET

PRODUCT SUMMARY			
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)[a]	Q_g (Typ)
75	0.011 @ V_{GS} = 10 V	28	33 nC
	0.0145 @ V_{GS} = 4.5 V	28	

FEATURES

- TrenchFET® Power MOSFET
- 100% R_g Tested
- RoHS Compliant

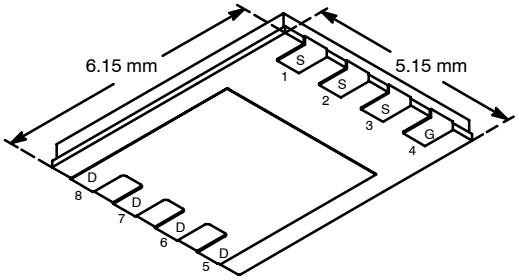
Pb-free

Product Is Completely Pb-free

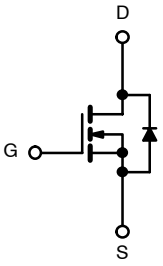
APPLICATIONS

- Primary Side Switch

PowerPAK SO-8



Bottom View



N-Channel MOSFET

Ordering Information: Si7148DP-T1—E3

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C UNLESS OTHERWISE NOTED)				
Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	75	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current (T_J = 150°C)	T_C = 25°C	I_D	28	A
	T_C = 70°C		22	
	T_A = 25°C		28[b, c]	
	T_A = 70°C		12[b, c]	
Pulsed Drain Current		I_{DM}	60	
Continuous Source-Drain Diode Current	T_C = 25°C	I_S	28	
	T_A = 25°C		4.3[b, c]	
Avalanche Current	L = 0.1 mH	I_{AS}	45	
Single-Pulse Avalanche Energy		E_{AS}	100	mJ
Maximum Power Dissipation	T_C = 25°C	P_D	96	W
	T_C = 70°C		61	
	T_A = 25°C		5.4[b, c]	
	T_A = 70°C		3.4[b, c]	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–50 to 150	°C
Soldering Recommendations (Peak Temperature)[d, e]			260	

Notes:
a. Based on T_C = 25°C.
b. Surface Mounted on 1" x 1" FR4 Board.
c. t = 10 sec
d. See Solder Profile (http://www.vishay.com/doc?73257). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
e. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient[a, b]	t ≤ 10 sec	R_{thJA}	18	23	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	1.0	1.3	

Notes:
a. Surface mounted on 1" x 1" FR4 board.
b. Maximum under steady state conditions is 65 °C/W.

SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA	75			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	I_D = 250 µA		75		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			–6		
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	1.5	2.0	2.5	V
		V_{DS} = V_{GS}, I_D = 5 mA		2.3		
Gate-Source Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 75 V, V_{GS} = 0 V			1	µA
		V_{DS} = 75 V, V_{GS} = 0 V, T_J = 55°C			10	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} ≥ 5 V, V_{GS} = 10 V				A
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 15 A		0.0091	0.011	Ω
		V_{GS} = 4.5 V, I_D = 13.5 A		0.012	0.0145	
Forward Transconductance[a]	g_{fs}	V_{DS} = 15 V, I_D = 15 A		60		S
Dynamic[b]						
Input Capacitance	C_{iss}	V_{DS} = 35 V, V_{GS} = 0 V, f = 1 MHz		2900		pF
Output Capacitance	C_{oss}			370		
Reverse Transfer Capacitance	C_{rss}			196		
Total Gate Charge	Q_g	V_{DS} = 38 V, V_{GS} = 10 V, I_D = 15 A		68	100	nC
		V_{DS} = 38 V, V_{GS} = 4.5 V, I_D= 15 A		33	50	
Gate-Source Charge	Q_{gs}			9.5		
Gate-Drain Charge	Q_{gd}			16.8		
Gate Resistance	R_g	f = 1 MHz	0.5	1.1	1.7	Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 38 V, R_L = 3.8 Ω I_D ≅ 10 A, V_{GEN} = 4.5 V, R_g = 1 Ω		33	50	ns
Rise Time	t_r			255	390	
Turn-Off Delay Time	$t_{d(off)}$			35	55	
Fall Time	t_f			100	150	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 38 V, R_L = 3.8 Ω I_D ≅ 10 A, V_{GEN} = 10 V, R_g = 1 Ω		17	26	
Rise Time	t_r			46	70	
Turn-Off Delay Time	$t_{d(off)}$			39	60	
Fall Time	t_f			18	30	

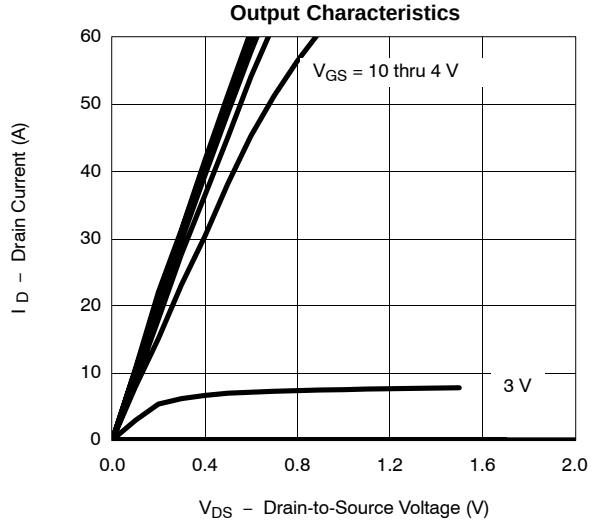
SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)						
Parameter	**Symbol**	**Test Condition**	**Min**	**Typ**	**Max**	**Unit**
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	T_C = 25°C			25	A
Pulse Diode Forward Current[a]	I_{SM}				60	
Body Diode Voltage	V_{SD}	I_S = 4.3 A		0.76	1.1	V
Body Diode Reverse Recovery Time	t_{rr}	I_F = 12 A, di/dt = 100 A/μs, T_J = 25°C		41	65	ns
Body Diode Reverse Recovery Charge	Q_{rr}			67	105	nC
Reverse Recovery Fall Time	t_a			27		ns
Reverse Recovery Rise Time	t_b			14		

Notes
a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

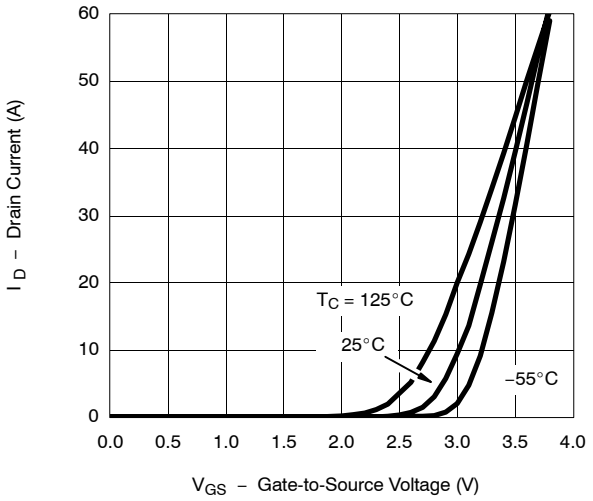
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

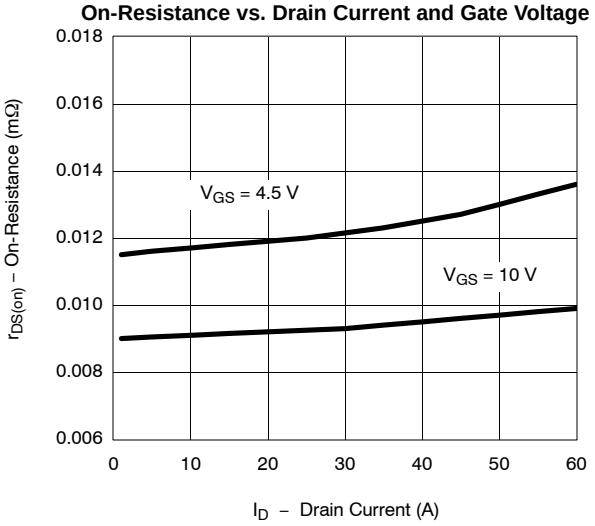
Output Characteristics



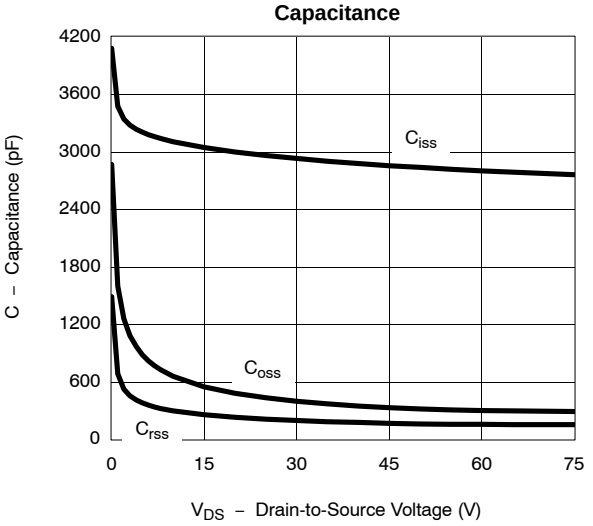
Transfer Characteristics



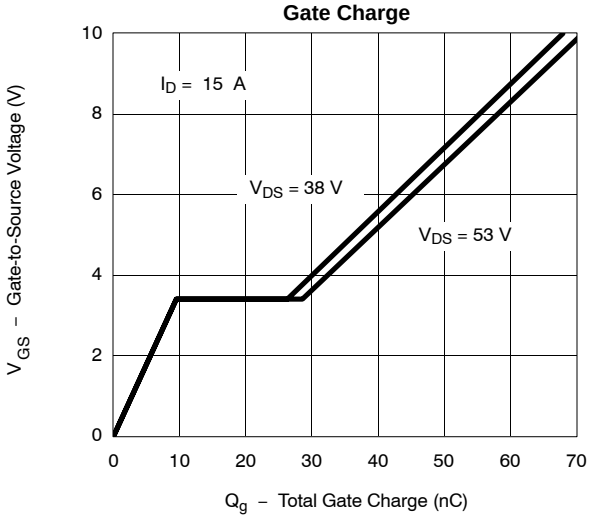
On-Resistance vs. Drain Current and Gate Voltage



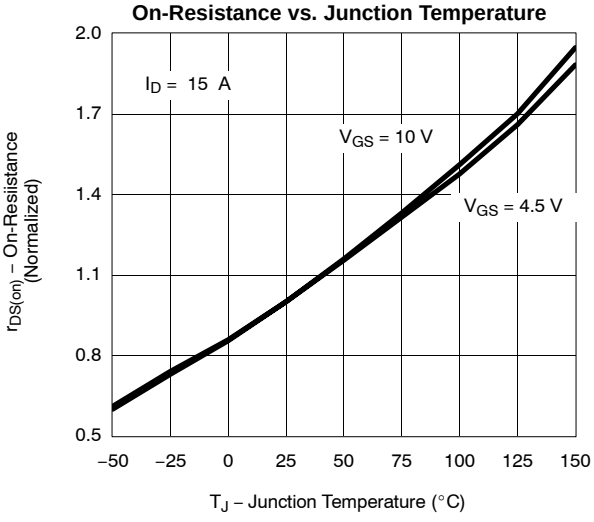
Capacitance



Gate Charge



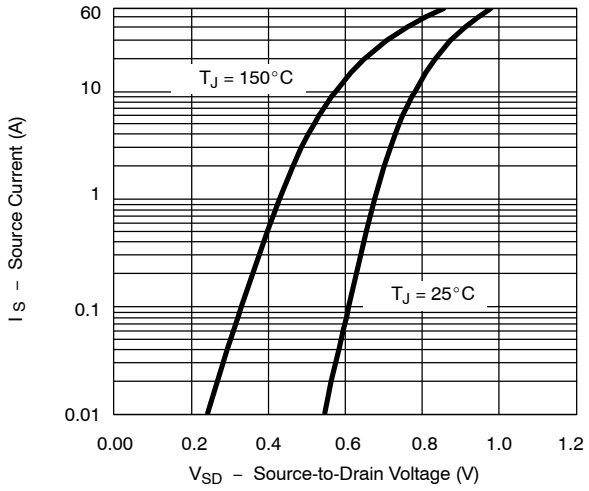
On-Resistance vs. Junction Temperature



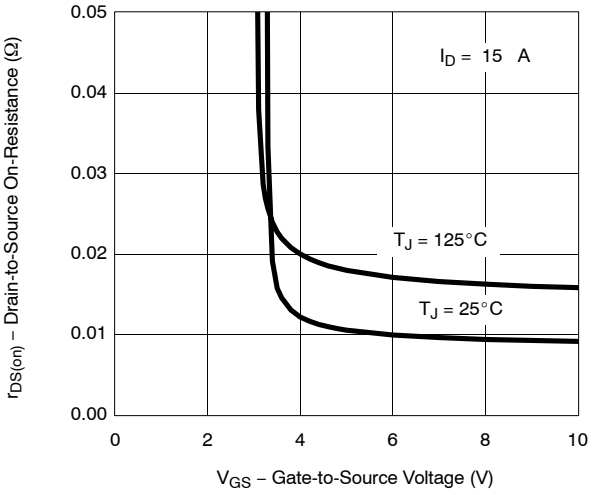
Document Number: 73314
S-50520—Rev. A, 21-Mar-05

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

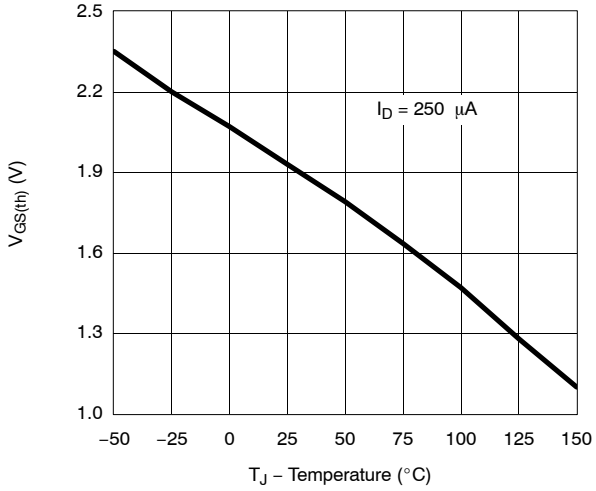
Source-Drain Diode Forward Voltage



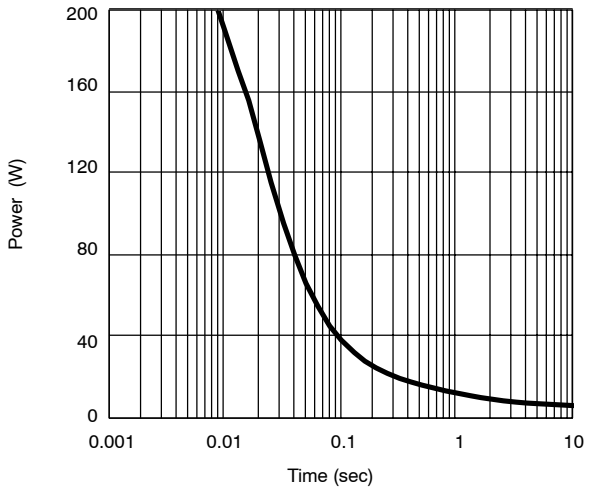
On-Resistance vs. Gate-to-Source Voltage



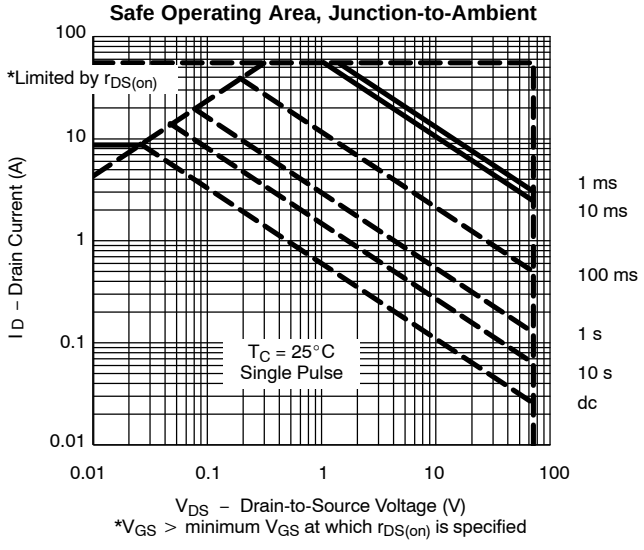
Threshold Voltage



Single Pulse Power, Junction-to-Ambient

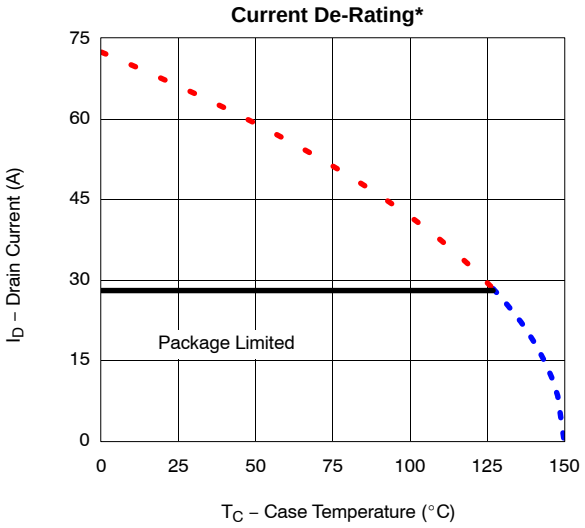


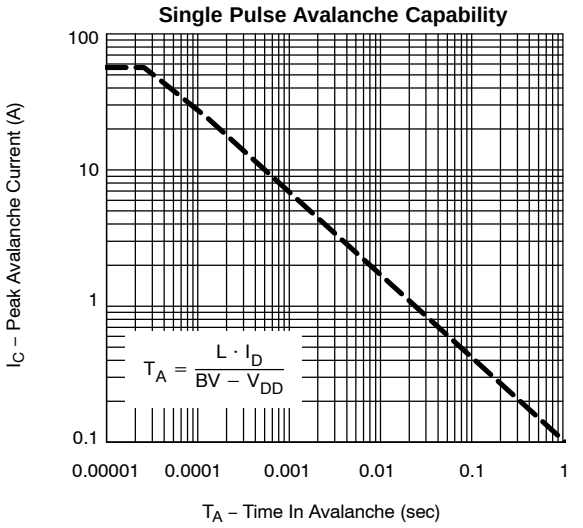
Safe Operating Area, Junction-to-Ambient

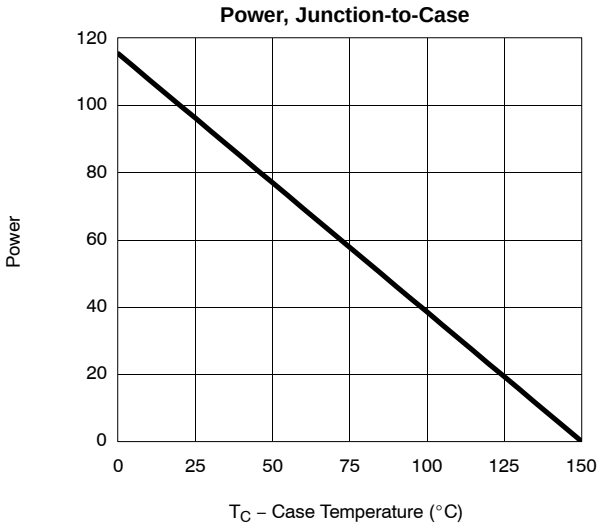


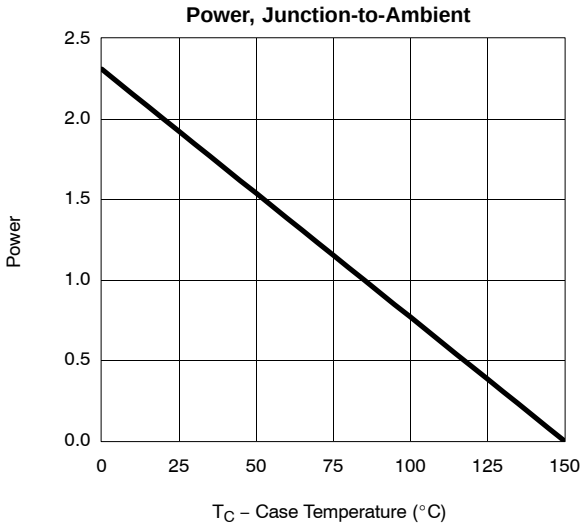
*V_{GS} > minimum V_{GS} at which $r_{DS(on)}$ is specified

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)



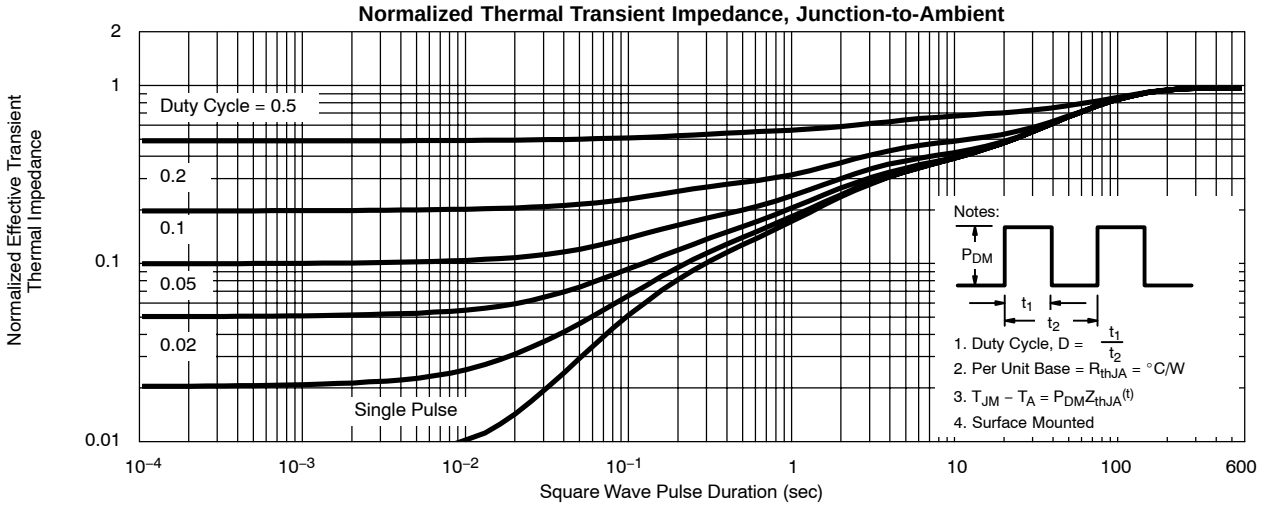


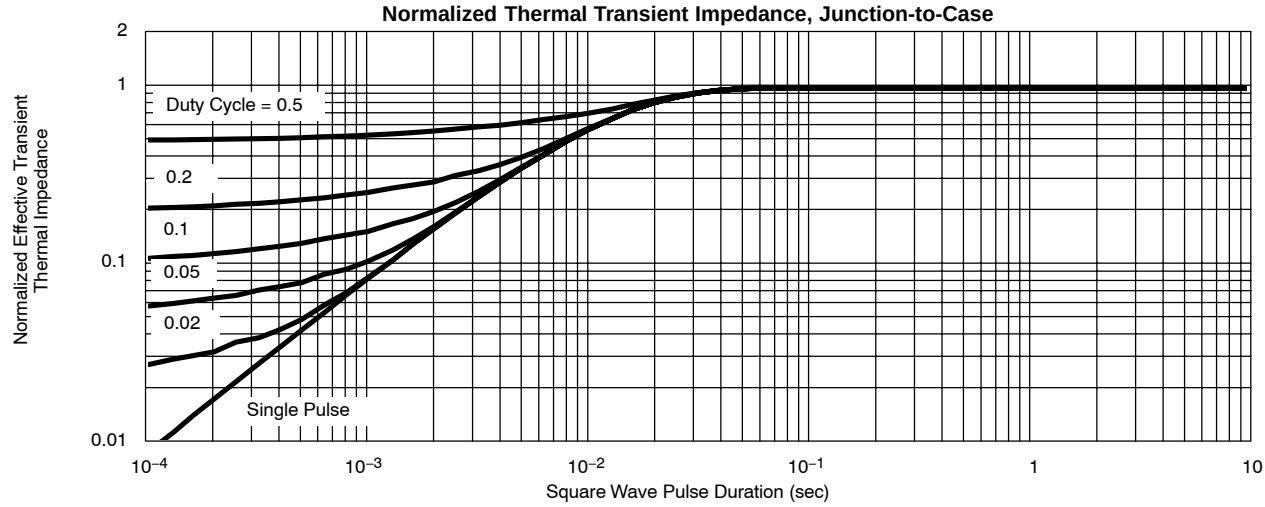




*The power dissipation P_D is based on $T_{J(max)}$ = 175°C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)





Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see http://www.vishay.com/ppg?73314.

Notice

Specifications of the products displayed herein are subject to change without notice. Vishay Intertechnology, Inc., or anyone on its behalf, assumes no responsibility or liability for any errors or inaccuracies.

Information contained herein is intended to provide a product description only. No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document. Except as provided in Vishay's terms and conditions of sale for such products, Vishay assumes no liability whatsoever, and disclaims any express or implied warranty, relating to sale and/or use of Vishay products including liability or warranties relating to fitness for a particular purpose, merchantability, or infringement of any patent, copyright, or other intellectual property right.

The products shown herein are not designed for use in medical, life-saving, or life-sustaining applications. Customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Vishay for any damages resulting from such improper use or sale.