

2N7002KA

N-channel TrenchMOS FET

Rev. 02 — 25 September 2007

Product data sheet

1. Product profile

1.1 General description

N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology.

1.2 Features

- Logic level compatible
- Subminiature surface-mounted package
- Very fast switching
- Gate-source ESD protection diodes

1.3 Applications

- Relay driver
- High-speed line driver

1.4 Quick reference data

- $V_{DS} \leq 60 \text{ V}$
- $R_{DS(on)} \leq 4.4 \ \Omega$
- $I_D \leq 300 \text{ mA}$
- $P_{tot} \leq 0.83 \text{ W}$

2. Pinning information

Table 1. Pinning

Pin	Description	Simplified outline	Symbol
1	gate (G)	 SOT23 (TO-236AB)	 003aac036
2	source (S)		
3	drain (D)		

3. Ordering information

Table 2. Ordering information

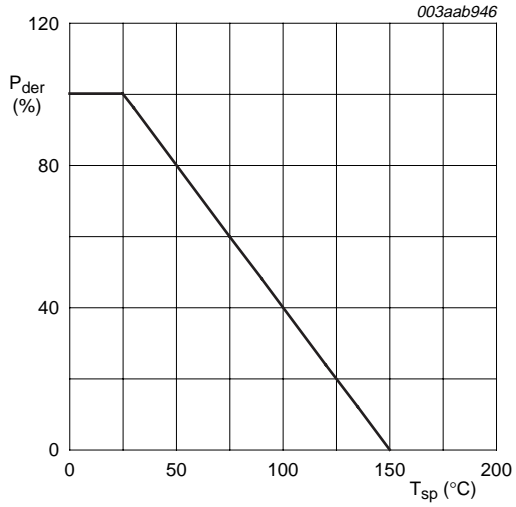
Type number	Package		Version
	Name	Description	
2N7002KA	TO-236AB	plastic surface-mounted package; 3 leads	SOT23

4. Limiting values

Table 3. Limiting values

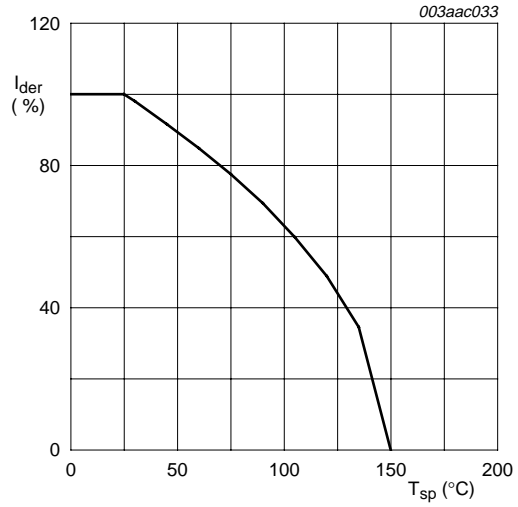
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	60	V
V_{DGR}	drain-gate voltage (DC)	$25\text{ °C} \leq T_j \leq 150\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	60	V
V_{GS}	gate-source voltage		-	± 15	V
V_{GSM}	peak gate-source voltage	$t_p \leq 50\text{ }\mu\text{s}$; pulsed; duty cycle = 25 %	-	± 40	V
I_D	drain current	$T_{sp} = 25\text{ °C}$; $V_{GS} = 10\text{ V}$; see Figure 2 and 3	-	320	mA
		$T_{sp} = 100\text{ °C}$; $V_{GS} = 10\text{ V}$; see Figure 2	-	200	mA
I_{DM}	peak drain current	$T_{sp} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$; see Figure 3	-	1.28	A
P_{tot}	total power dissipation	$T_{sp} = 25\text{ °C}$; see Figure 1	-	0.83	W
T_{stg}	storage temperature		-55	+150	°C
T_j	junction temperature		-55	+150	°C
Source-drain diode					
I_S	source current	$T_{sp} = 25\text{ °C}$	-	300	mA
I_{SM}	peak source current	$T_{sp} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$	-	1.2	A



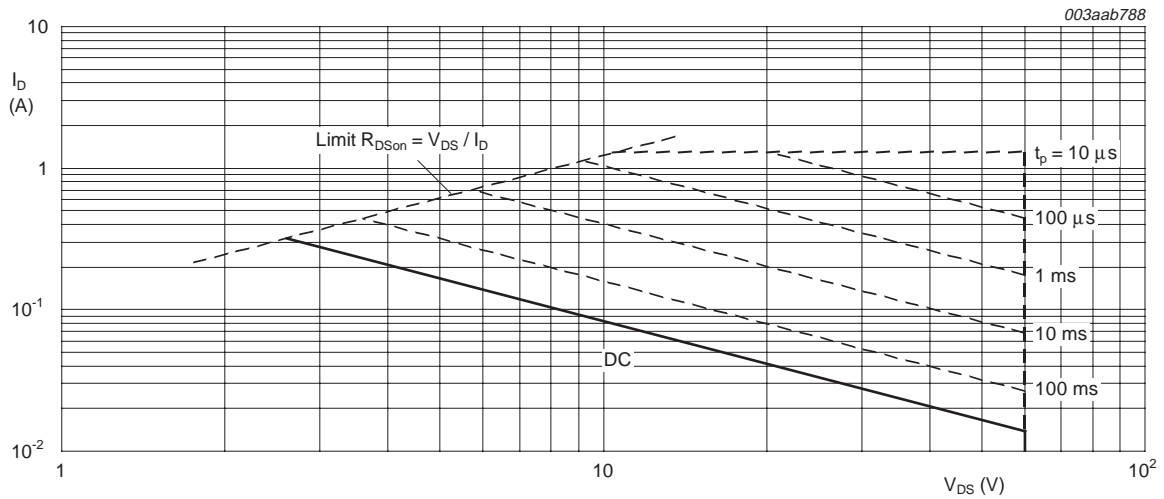
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of solder point temperature



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of solder point temperature



T_{sp} = 25 °C; I_{DM} is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	see Figure 4	-	-	150	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient		[1]	-	350	K/W

[1] Mounted on a printed-circuit board; minimum footprint; vertical in still air.

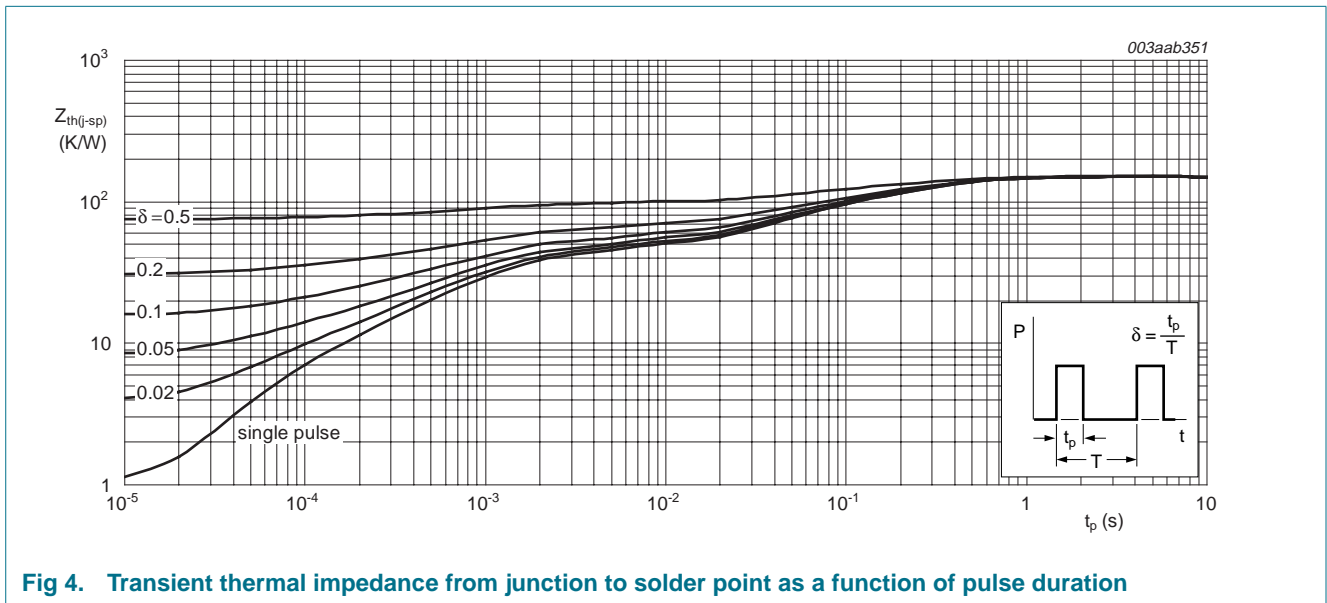


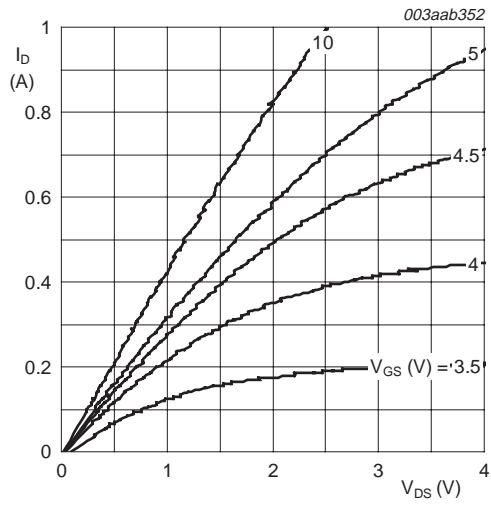
Fig 4. Transient thermal impedance from junction to solder point as a function of pulse duration

6. Characteristics

Table 5. Characteristics

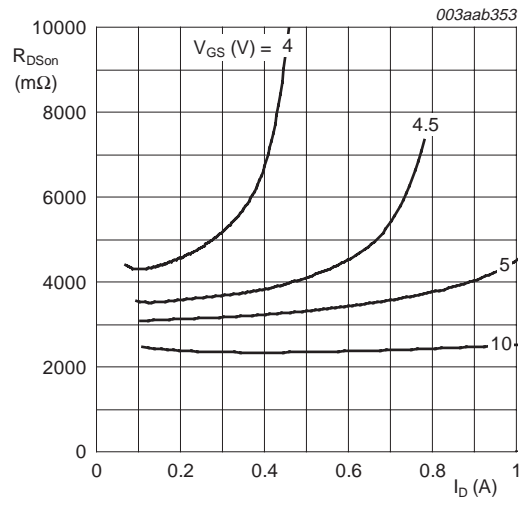
$T_j = 25\text{ }^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 10\text{ }\mu\text{A}$; $V_{GS} = 0\text{ V}$				
		$T_j = 25\text{ }^\circ\text{C}$	60	75	-	V
		$T_j = -55\text{ }^\circ\text{C}$	55	-	-	V
$V_{(BR)GSS}$	gate-source breakdown voltage	$I_G = \pm 1\text{ mA}$; $V_{DS} = 0\text{ V}$	16	22	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\text{ mA}$; $V_{DS} = V_{GS}$; see Figure 9 and 10				
		$T_j = 25\text{ }^\circ\text{C}$	1	2	-	V
		$T_j = 150\text{ }^\circ\text{C}$	0.6	-	-	V
		$T_j = -55\text{ }^\circ\text{C}$	-	-	3.5	V
I_{DSS}	drain leakage current	$V_{DS} = 48\text{ V}$; $V_{GS} = 0\text{ V}$				
		$T_j = 25\text{ }^\circ\text{C}$	-	0.01	1	μA
		$T_j = 150\text{ }^\circ\text{C}$	-	-	10	μA
I_{GSS}	gate leakage current	$V_{GS} = \pm 10\text{ V}$; $V_{DS} = 0\text{ V}$	-	50	500	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 500\text{ mA}$; see Figure 6 and 8				
		$T_j = 25\text{ }^\circ\text{C}$	-	2.8	4.4	Ω
		$T_j = 150\text{ }^\circ\text{C}$	-	-	8.14	Ω
		$V_{GS} = 4.5\text{ V}$; $I_D = 75\text{ mA}$; see Figure 6 and 8	-	3.8	5.3	Ω
Dynamic characteristics						
C_{iss}	input capacitance	$V_{GS} = 0\text{ V}$; $V_{DS} = 10\text{ V}$; $f = 1\text{ MHz}$; see Figure 12	-	13	40	pF
C_{oss}	output capacitance		-	8	30	pF
C_{rss}	reverse transfer capacitance		-	4	10	pF
t_{on}	turn-on time	$V_{DS} = 50\text{ V}$; $R_L = 250\text{ }\Omega$; $V_{GS} = 10\text{ V}$; $R_G = 50\text{ }\Omega$; $R_{GS} = 50\text{ }\Omega$	-	3	10	ns
t_{off}	turn-off time		-	9	15	ns
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 300\text{ mA}$; $V_{GS} = 0\text{ V}$; see Figure 11	-	0.85	1.5	V
t_{rr}	reverse recovery time	$I_S = 300\text{ mA}$; $di_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$;	-	30	-	ns
Q_r	recovered charge	$V_{DS} = 25\text{ V}$	-	30	-	nC



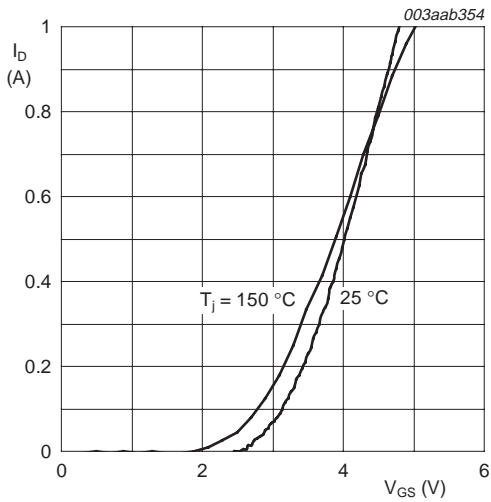
$T_j = 25^\circ\text{C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



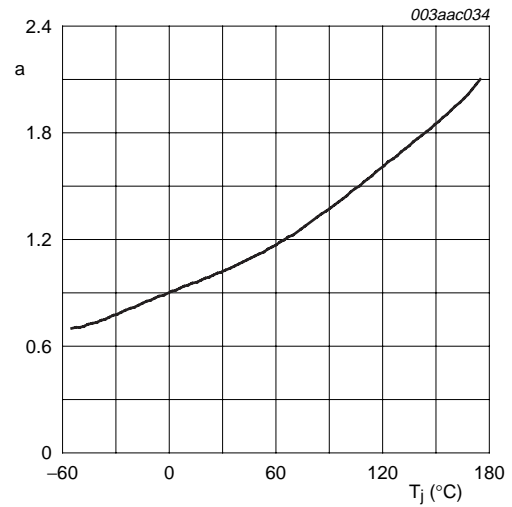
$T_j = 25^\circ\text{C}$

Fig 6. Drain-source on-state resistance as a function of drain current; typical values



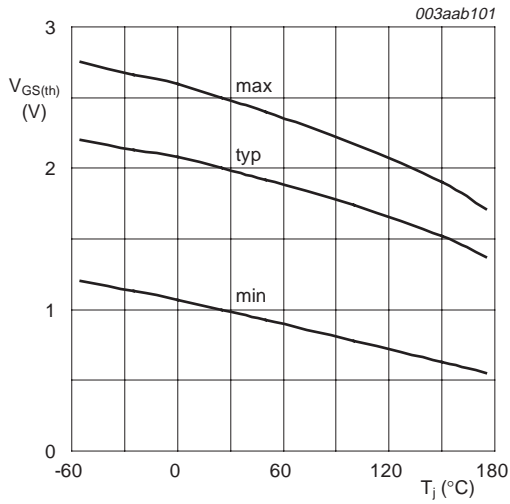
$T_j = 25^\circ\text{C}$ and 150°C ; $V_{DS} > I_D \times R_{DS(on)}$

Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values



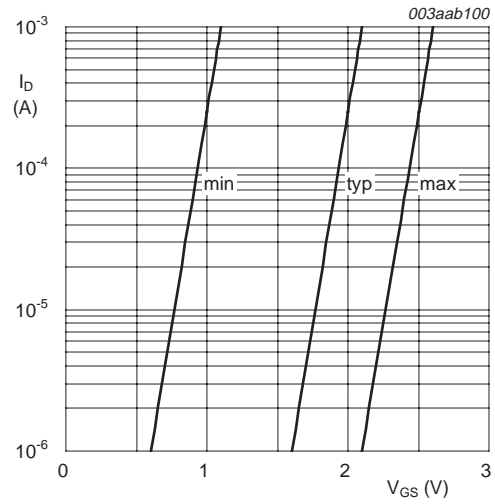
$$a = \frac{R_{DS(on)}}{R_{DS(on)(25^\circ\text{C})}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature



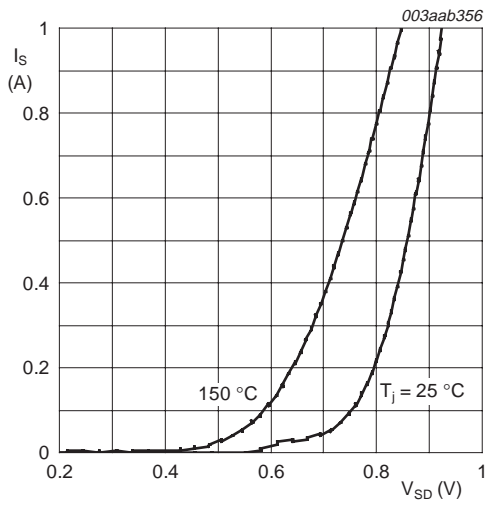
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature



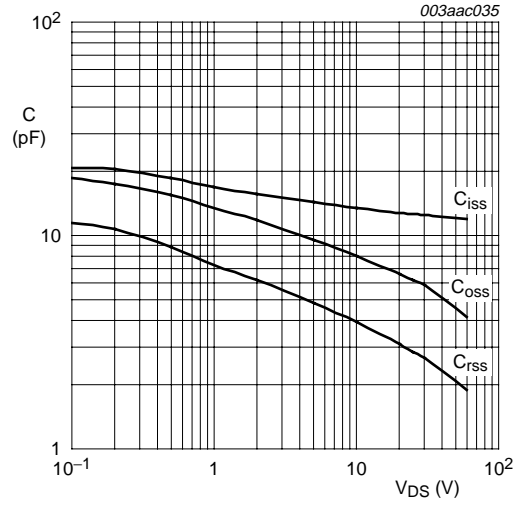
$T_j = 25 \text{ }^{\circ}C; V_{DS} = 5 \text{ V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage



$T_j = 25 \text{ }^{\circ}C \text{ and } 150 \text{ }^{\circ}C; V_{GS} = 0 \text{ V}$

Fig 11. Source current as a function of source-drain voltage; typical values



$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

7. Package outline

Plastic surface-mounted package; 3 leads

SOT23

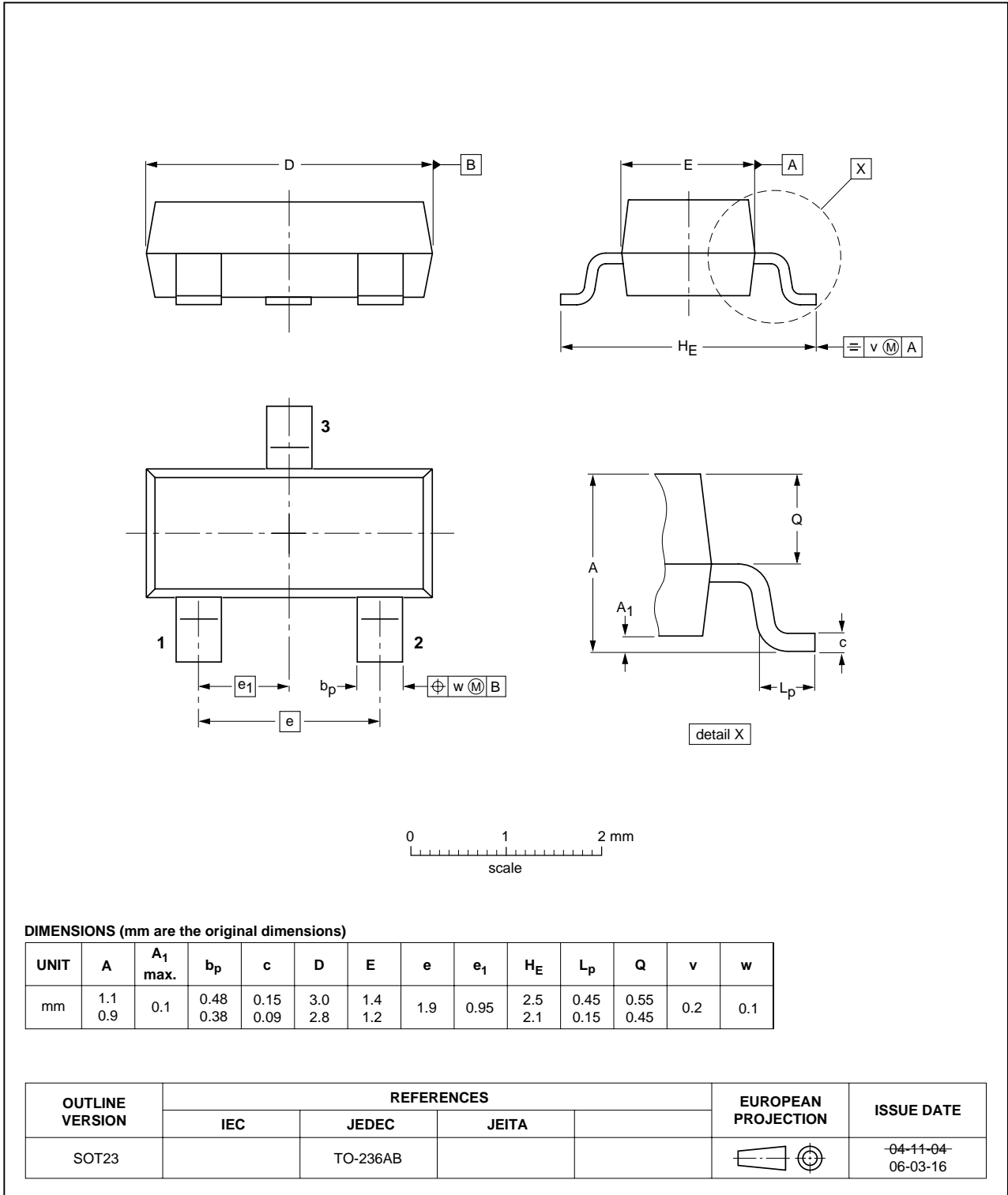


Fig 13. Package outline SOT23 (TO-236AB)

8. Revision history

Table 6. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
2N7002KA_2	20070925	Product data sheet		2N7002KA_1
Modifications:	• The Symbol graphic in Table 1 was updated.			
2N7002KA_1	20070605	Product data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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