

2SA1344, 2SC3398



2018A

PNP/NPN Epitaxial Planar
Silicon Transistors

T-37-13
T-35-11

Switching Applications (with Bias Resistances R1=10kΩ, R2=10kΩ)

©1286C

Applications

- Switching circuit, inverter circuit, interface circuit, driver circuit.

Features

- Built-in bias resistor (R1=10kΩ, R2=10kΩ).
- Small-sized package (CP).

() : 2SA1344

Absolute Maximum Ratings/Ta=25°C

			unit
Collector to Base Voltage	VCBO	(-)50	V
Collector to Emitter Voltage	VCEO	(-)50	V
Emitter to Base Voltage	VEBO	(-)10	V
Collector Current	IC	(-)100	mA
Peak Collector Current	icp	(-)200	mA
Collector Dissipation	PC	200	mW
Junction Temperature	Tj	150	°C
Storage Temperature	Tstg	-55 to +150	°C

Electrical Characteristics/Ta=25°C

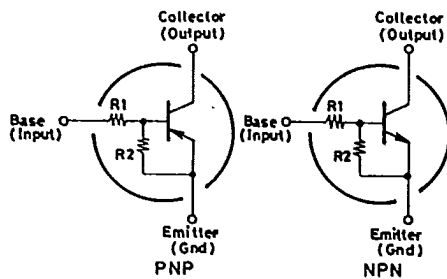
			min	typ	max	unit
Collector Cutoff Current	ICBO	VCB=(-)40V, IE=0			(-)0.1	μA
Collector Cutoff Current	ICEO	VCE=(-)40V, IB=0			(-)0.5	μA
Emitter Cutoff Current	IEBO	VEB=(-)5V, IC=0	(-)170	(-)250	(-)330	μA
DC Current Gain	hFE	VCE=(-)5V, IC=(-)10mA	50			
Gain Band-width product	fT	VCE=(-)10V, IC=(-)5mA		250 (200)		MHz
Output Capacitance	cob	VCB=(-)10V, f=1MHz		3.5 (5.3)		pF
Collector to Emitter Saturation Voltage	VCE(sat)	IC=(-)10mA, IB=(-)0.5mA	(-)0.1	(-)0.3		V

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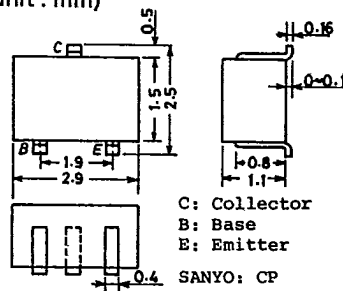
Marking

2SA1344: EL, 2SC3398: EY

Electrical Connection



Case Outline 2018A (unit : mm)



2SA1344/2SC3398

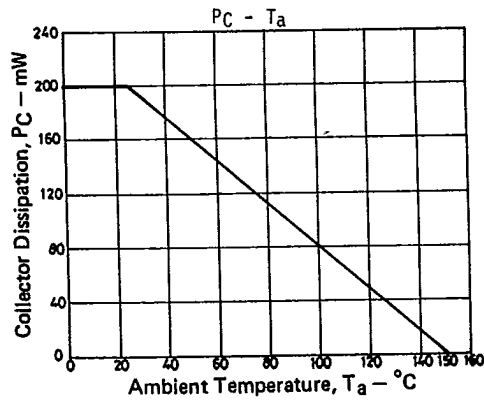
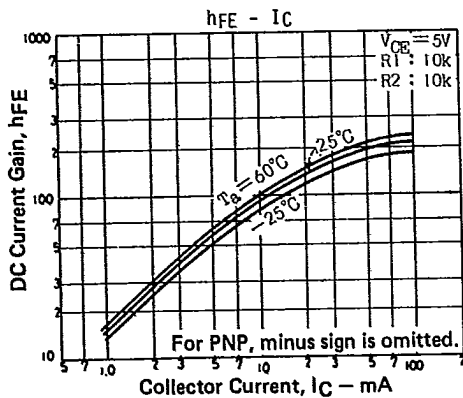
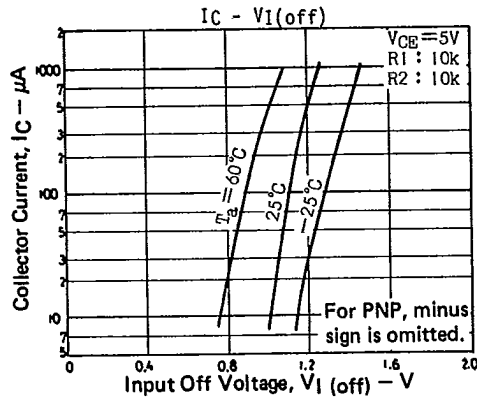
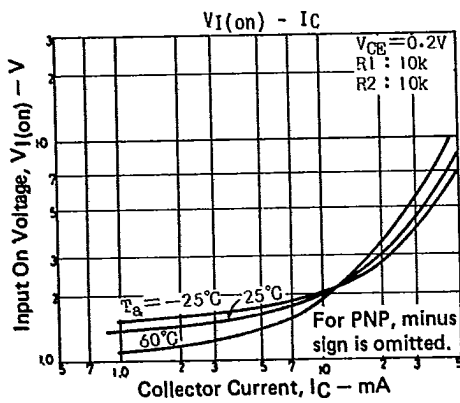
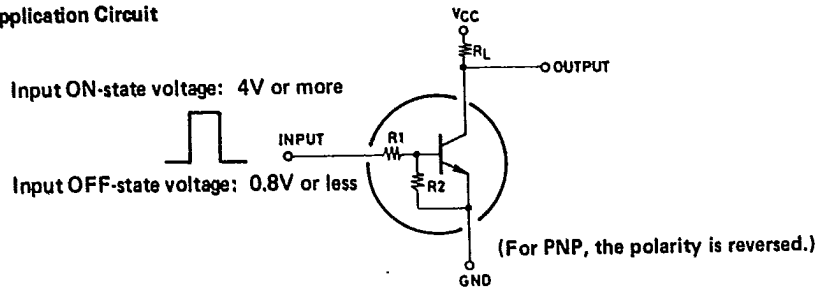
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			min	typ	max	unit
Collector to Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C=(-)10\mu A, I_E=0$	(-)50			V
Collector to Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C=(-)100\mu A, R_{BE}=\infty$	(-)50			V
Input Off Voltage	$V_{I(off)}$	$V_{CE}=(-)5V, I_C=(-)100\mu A$	(-)0.8	(-)1.1	(-)1.5	V
Input On Voltage	$V_{I(on)}$	$V_{CE}=(-)0.2V, I_C=(-)10mA$	(-)1.0	(-)2.0	(-)4.0	V
Input Resistance	R_1		7.0	10	13	k Ω
Input Resistance Ratio	R_1/R_2		0.9	1.0	1.1	-

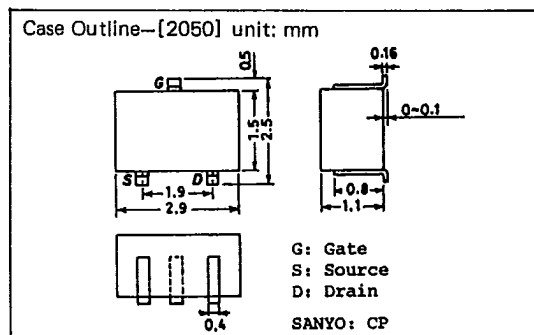
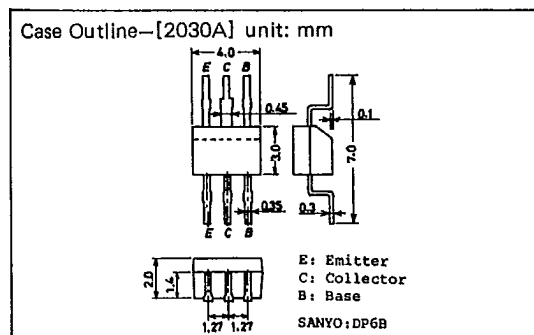
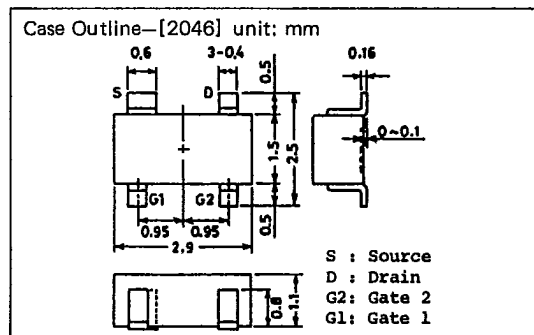
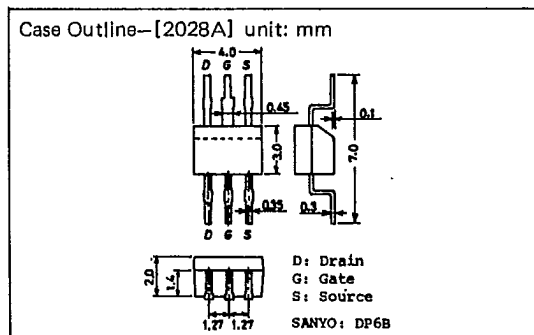
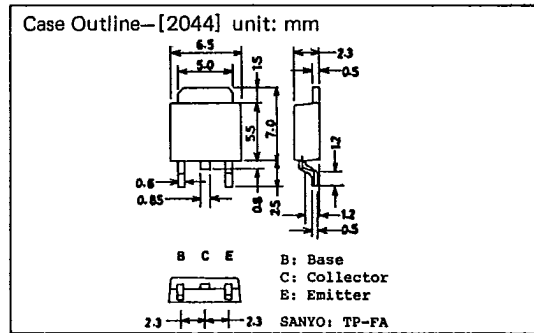
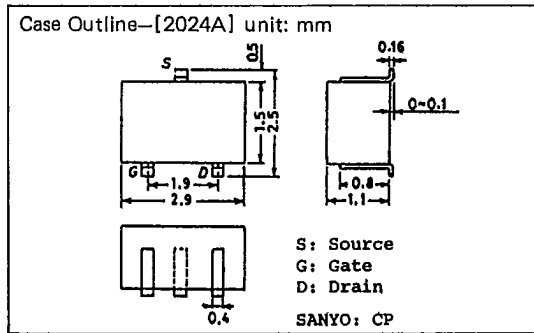
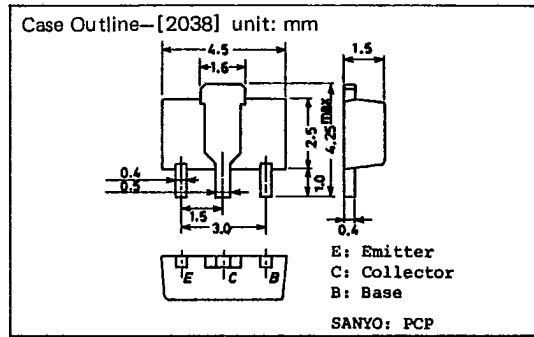
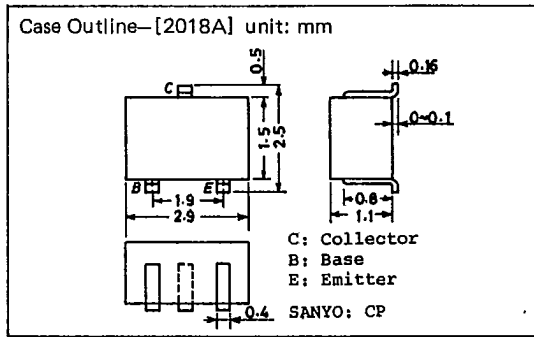
■ Sample Application Circuit



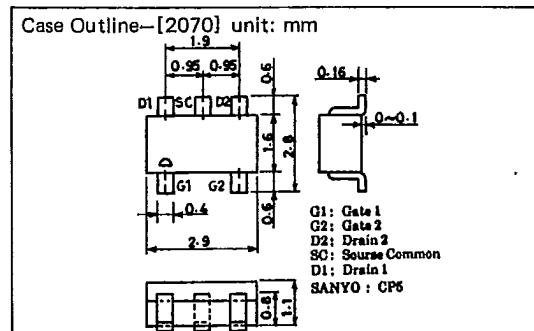
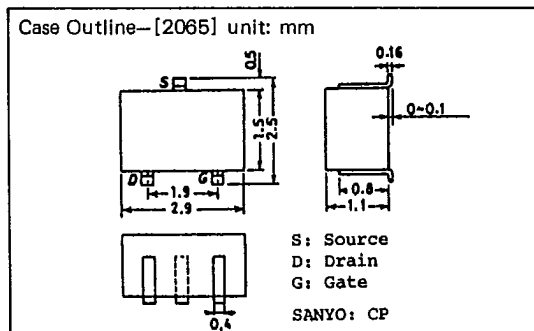
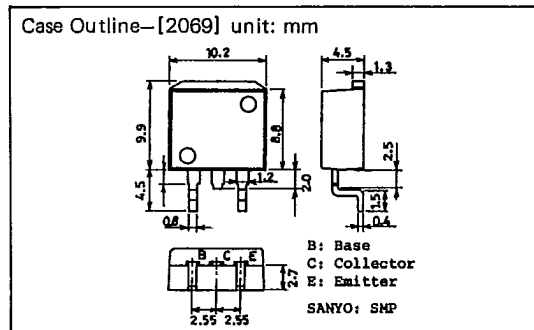
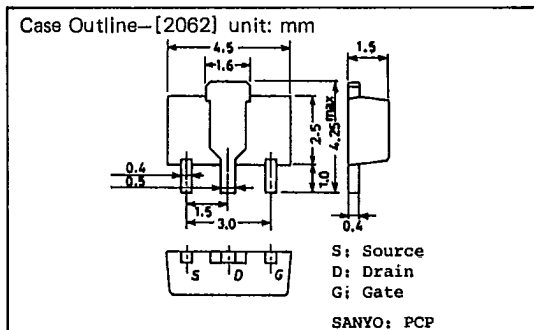
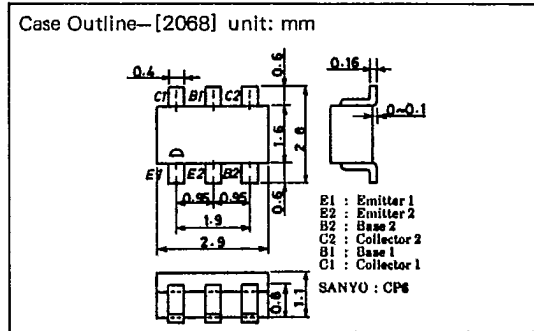
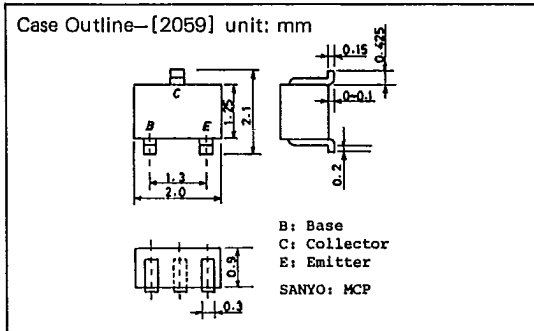
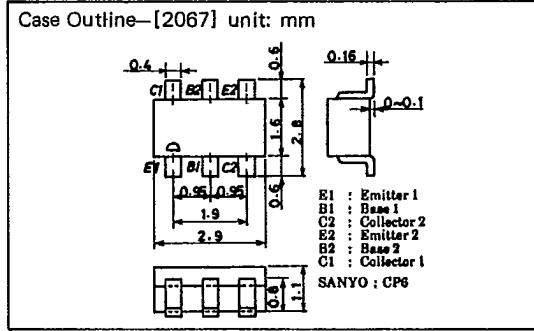
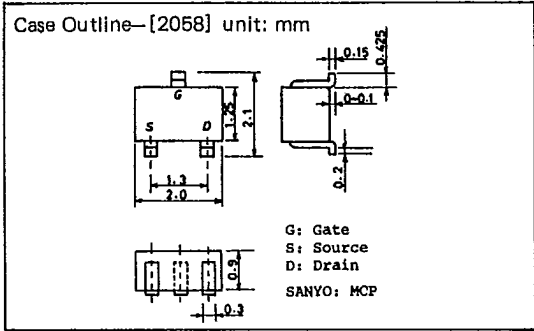
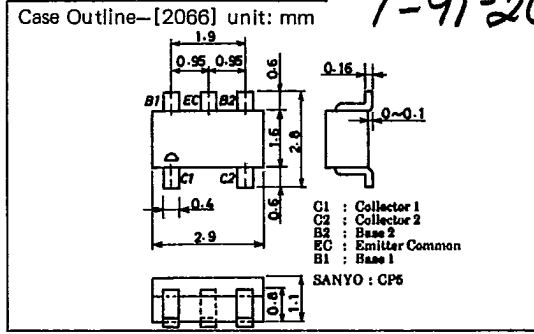
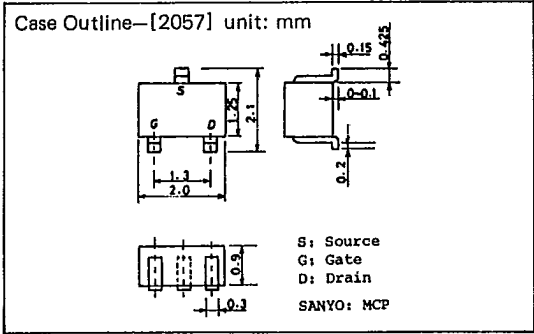
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CASE OUTLINES OF SURFACE MOUNT TRANSISTORS

- All of Sanyo surface mount transistor case outlines are illustrated below.
- All dimensions are in mm, and dimensions which are not followed by min. or max. are represented by typical values.
- No marking is indicated.



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