

2SA1572/2SC4067

PNP/ NPN Epitaxial Planar Silicon Transistors

Switching Applications (with Bias/Resistance)

Applications

. Switching circuit, inverter circuit, interface circuit, driver circuit

Features

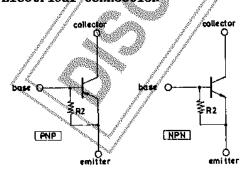
- . On-chip bias resistance: R1=0, R2=47k Ω
- . Small-sized package: SPA

(): PNP

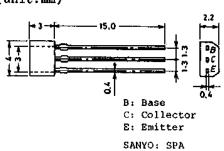
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Absolute Maximum Ratings at Ta-	±25°C	; // unit
Collector to Base Voltage	V_{CBO}	(-X50 V
Collector to Emitter Voltage	VCEO	
Emitter to Base Voltage	VEBO	
Collector Current	IC	(-)100 ma
Collector Current(Pulse)	I_{CP}	// (~)200 /mA
Collector Dissipation	$P_{\mathbf{C}}$	// 300//mW
Junction Temperature	Tj /	// 150/ °C
Storage Temperature	Tatg	/ -55 to +150 °C

Klectrical Characteristics at Ta=2500	min	typ	max	unit
Collector Cutoff Current Icoa Vass (-740V.Is=0		(-	-)0.1	μ A
$I_{OPO} = (-)40$ $I_{B}=0$		(-	-)0.5	μΑ
Emitter Cutoff Current /Irpa Vra (-)5V.1c=0	(-)81(-)	-)106(-	-)151	$\mu \mathbf{A}$
DC Current Gain h_{EE} $V_{CE}=(-)5V, I_{CE}=(-)10mA$	80			
Gain-Bandwidth Product f_T $\chi_{CE} = (-)10V, I_{CE} = (-)5mA$		250		MHz
		(200)		
Output Capacitance V _{CB} =(-)10V,f=1MHz		3.7		рF
		(5.5)		
C-E Saturation Voltage VCE(sat) 1c=(-)10mA, IB=(-)0.5mA	(-	-)0.1(-	-)0.3	٧
C-B Breakdown Voltage $(BR)CBO$ $I_{C}=(-)10\mu$ A, $I_{E}=0$	(-)50			V
C-E Breakdown Voltage $V_{(BR)CEO}^{(BR)CEO} I_{C}^{(-)} = (-)100 \mu A, R_{BE}^{(-)} = \infty$	(-)50			V
Resistance R2 R2	33	47	61	kΩ

Blectrical Connection



Case Outline 2033 (unit:mm)



Specifications and information herein are subject to change without notice.

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