

DATA SHEET



TZA1020; TZA1020A Pre-amplifiers for CD-RW systems

Product specification
File under Integrated Circuits, IC01

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Pre-amplifiers for CD-RW systems

TZA1020; TZA1020A

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1 FEATURES

- Data amplifier for read speed up to twelve times nominal data speed
- Normalized and filtered error signals for servo control
- Wobble pre-processor with switchable low-pass filter
- Calculation of signals for real-time laser power control for write speed up to four times
- Calculation of signals for optimum laser calibration for write speed up to four times
- Fast track count amplifier
- Spot position measurement for alignment of photo diodes
- Reference voltage for laser controller
- On-chip band gap and DACs for accurate and adjustable current/gain settings
- I²C-bus microcontroller interface for programmable gain, speed switching and function selection
- All functions available for CD-R and CD-RW systems.

**2 GENERAL DESCRIPTION**

TZA1020 (AEGER2) is an analog pre-processor IC for CD-R and CD-RW systems with 3-spots push-pull tracking system. The IC interfaces directly to the photo diodes. The device generates signals for laser power calibration and laser power control during disc writing. Normalized error signals are generated for servo control and wobble detection. An HF current amplifier is implemented to detect the actual HF data signal. The Fast Track Count (FTC) amplifier generates a radial error signal to allow fast track counting.

TZA1020A (AEGER2A) is similar to the TZA1020, except for non-clamped MIRR, which allows operation with IGUANA.

3 QUICK REFERENCE DATA

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|--------------------------|--|--|------|------|------|------|
| V _{DD} | positive supply voltage | | 4.5 | 5.0 | 5.5 | V |
| V _{SS} | negative supply voltage | | -5.5 | -5.0 | -4.5 | V |
| I _{i(cd)} | central diode input current range | | 0 | - | 4000 | μA |
| B _{-3dB(norm)} | -3 dB bandwidth normalized error signals (servo) | | 48 | 60 | - | kHz |
| B _{-3dB(CAHF)} | -3 dB bandwidth pin CAHF | C _i = 12 pF | 17 | - | - | MHz |
| Δt _{d(g)(CAHF)} | group delay variations pin CAHF | f = 0.1 to 12 MHz; C _i = 12 pF | - | - | 0.9 | ns |
| G _{I(CAHF)} | current gain pin CAHF | cdrwsel = 1 | - | 35 | - | |
| | | cdrwsel = 0 | - | 8.75 | - | |
| I _{RREF} | reference current | | - | -900 | - | μA |
| T _{amb} | ambient temperature | | 0 | - | 70 | °C |

4 ORDERING INFORMATION

| TYPE NUMBER | PACKAGE | | |
|---------------------------|---------|---|----------|
| | NAME | DESCRIPTION | VERSION |
| TZA1020HP; TZA1020HP/A | QFP44 | plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm | SOT307-2 |

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5 BLOCK DIAGRAM

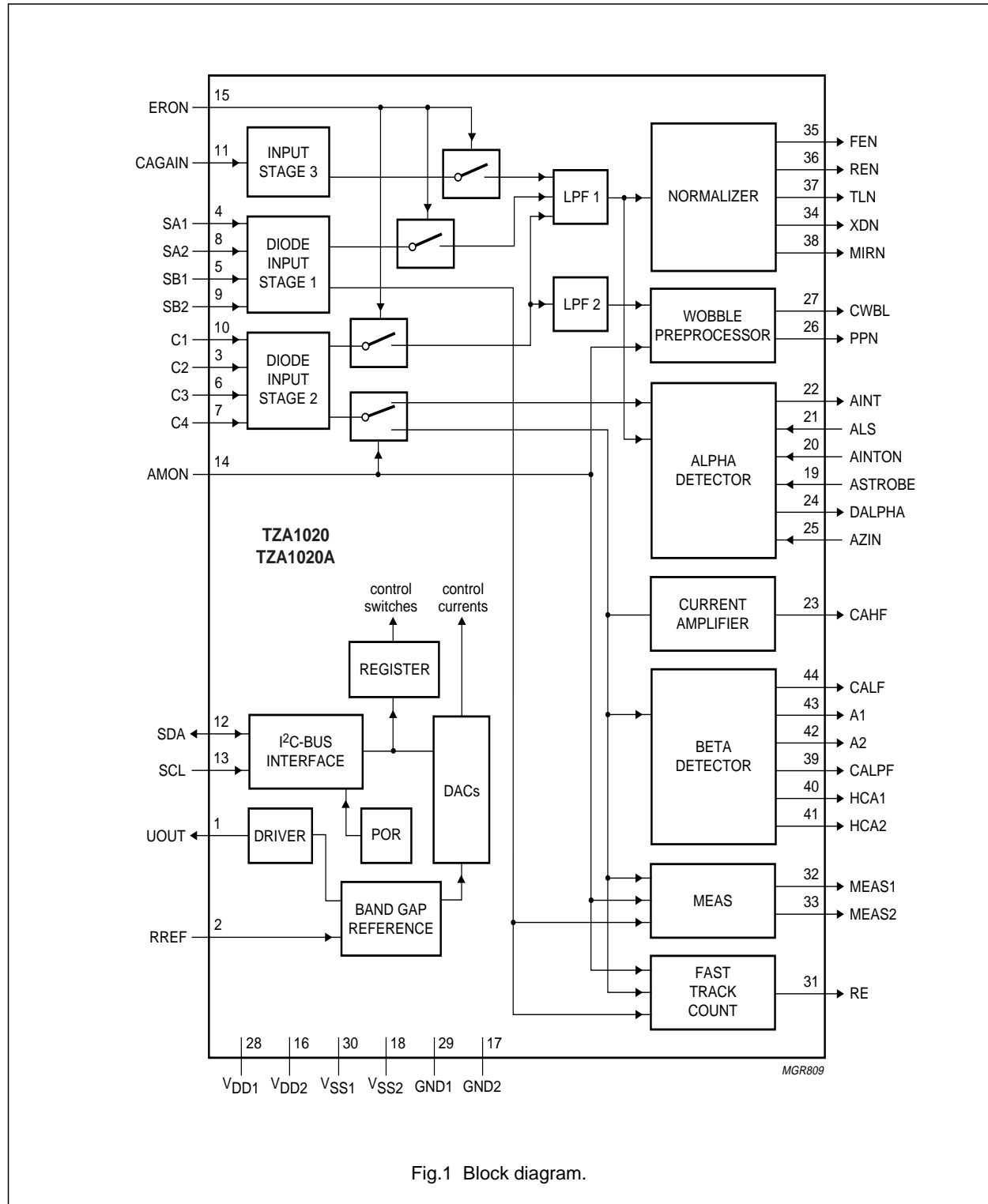


Fig.1 Block diagram.

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6 PINNING

| SYMBOL | PIN | DESCRIPTION |
|------------------|-----|---|
| UOUT | 1 | reference voltage output |
| RREF | 2 | reference current input |
| C2 | 3 | central photo diode current input |
| SA1 | 4 | satellite photo diode current input |
| SB1 | 5 | satellite photo diode current input |
| C3 | 6 | central photo diode current input |
| C4 | 7 | central photo diode current input |
| SA2 | 8 | satellite photo diode current input |
| SB2 | 9 | satellite photo diode current input |
| C1 | 10 | central photo diode current input |
| CAGAIN | 11 | set-point laser power on disc, current input |
| SDA | 12 | I ² C-bus data input/output |
| SCL | 13 | I ² C-bus clock input |
| AMON | 14 | alpha measurement on switch (write/read state) |
| ERON | 15 | normalized error signals on switch |
| V _{DD2} | 16 | positive supply voltage 2 |
| GND2 | 17 | ground 2 |
| V _{SS2} | 18 | negative supply voltage 2 |
| ASTROBE | 19 | control signal sample-and-hold in alpha measurement |
| AINTON | 20 | control signal integrator in alpha measurement |
| ALS | 21 | DALPHA output enabled/disabled |
| AINT | 22 | integrator capacitor for alpha measurement |
| CAHF | 23 | central aperture high-frequency current output |
| DALPHA | 24 | alpha error signal for laser power control |
| AZIN | 25 | set-point alpha control |

| SYMBOL | PIN | DESCRIPTION |
|------------------|-----|--|
| PPN | 26 | normalized, balanced push-pull signal voltage |
| CWBL | 27 | capacitor for EFM noise reduction loop |
| V _{DD1} | 28 | positive supply voltage 1 |
| GND1 | 29 | ground 1 |
| V _{SS1} | 30 | negative supply voltage 1 |
| RE | 31 | fast track count signal voltage output |
| MEAS1 | 32 | combination of photo diode currents for adjustment 1 |
| MEAS2 | 33 | combination of photo diode currents for adjustment 2 |
| XDN | 34 | normalized spot position error current output |
| FEN | 35 | normalized focus error current output |
| REN | 36 | normalized radial error current output |
| TLN | 37 | normalized track-loss current output |
| MIRN | 38 | mirror output (disc reflection) current output |
| CALPF | 39 | capacitor to define CALF bandwidth |
| HCA1 | 40 | capacitor to define time constant peak detector A1 |
| HCA2 | 41 | capacitor to define time constant peak detector A2 |
| A2 | 42 | pit amplitude relative to CALF, voltage output |
| A1 | 43 | land amplitude relative to CALF, voltage output |
| CALF | 44 | low-pass filtered aperture signal, voltage output |

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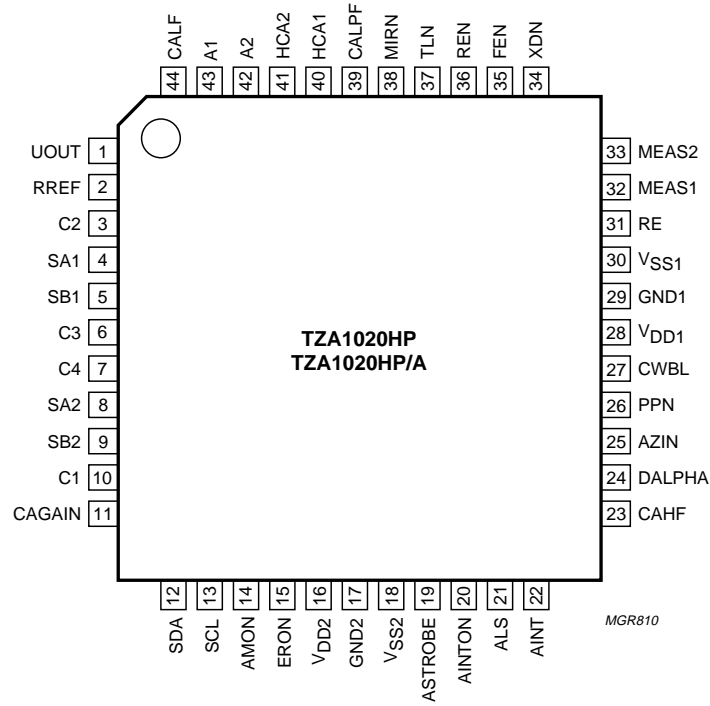


Fig.2 Pin configuration.

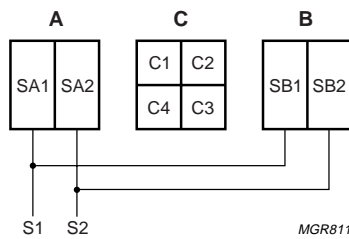


Fig.3 Quadrant diode configuration.

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7 FUNCTIONAL DESCRIPTION

All functions are designed in such a way that a read speed up to twelve times nominal speed is possible ($N = 1, 2, 4, 8$ or 12). Recording speed up to four is possible ($N = 1, 2$ or 4). The maximum recording speed must be determined.

7.1 Data amplifier

The central diodes currents (C1 to C4) are fed to a high bandwidth current amplifier. The gain of the current amplifier can be switched by means of the I²C-bus microcontroller interface to compensate for differences in CD-R and CD-RW disc reflection. Data signals up to twelve times nominal data speed can be read.

7.2 Normalizer

The currents from the central diodes (C1 to C4), the current from the satellite diodes (SA1, SA2, SB1 and SB2) and the laser set-point current (CAGAIN) are (optionally sampled) fed to the first low-pass filters with a bandwidth of 60 kHz. The normalizing circuit generates error signals for servo control that are independent of the diode current level. The gain of the error signals is controlled by the I²C-bus microcontroller interface. A dropout concealment becomes active if the input current level is below a certain threshold value. This threshold value is also controlled by the I²C-bus.

7.3 Wobble pre-processor

The wobble signal of the pre-groove is detected by means of the PPN signal. The currents from inputs C1 to C4 are filtered and processed to provide optimal signal-to-noise ratio. The bandwidth of the filter may be adapted to the disc speed via the I²C-bus. The bandwidth of a noise reduction loop is controlled by an external capacitor, the I²C-bus interface controls the total operation of the processor.

7.4 Beta detector

The beta detector generates signals necessary for the symmetry detection of the HF signal. By measuring peak values (A1 and A2) and average value of the signal (CALF), an optimum laser writing power can be determined. The gain of the measured values is controlled by the I²C-bus. The time constant of the peak detectors and bandwidth of the low-pass filtered aperture signal can also be adapted to the disc speed by the I²C-bus.

7.5 Alpha detector

The alpha detector determines a parameter called 'alpha' during disc writing. Alpha must be kept constant to allow recording over a fingerprint or black dot. The definition of alpha is different for CD-R and CD-RW; for CD-R the light absorption of the disc is measured, for CD-RW alpha is determined by actual laser power and disc reflection. The gain of the measured signals and the CD-R and CD-RW selection is performed by the I²C-bus.

7.6 Fast track count

The fast track count circuit generates a Radial Error (RE) signal for fast track counting. A gain switch compensates for difference in CD-R and CD-RW disc reflection.

7.7 Spot position measurement

To allow alignment of photo diodes via the TZA1020, a number of linear combinations of input currents can be realized (MEAS1 and MEAS2). Selection of the actual combination is performed by the I²C-bus.

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8 I²C-BUS PROTOCOL**8.1 Addressing and data bytes**

Full control of the TZA1020 is accomplished via the 2-wire I²C-bus. Up to 400 kbits/s bus speed can be used in accordance with the I²C-bus fast-mode specification.

For programming the device (write mode) eight data byte registers are available/addressable via eight subaddresses. Automatic subaddress incrementing enables the writing of successive data bytes in one transmission. During power-on, data byte registers are reset to a default state by use of a Power-On Reset (POR) circuit whose signal is derived from the internally generated I²C-bus supply voltage (V_{SS1}).

For reading from the device (read mode) one data byte register is available without subaddressing.

8.1.1 WRITE MODE

Table 1 Slave address; 34H

| | | | | | | | | |
|---------------|---|---|---|---|---|---|---|---|
| Slave address | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 |
|---------------|---|---|---|---|---|---|---|---|

Table 2 Subaddress 00H to 07H

| | | | | | | | | |
|------------|------------------|------------------|------------------|------------------|---|-----|-----|-----|
| Subaddress | 0 ⁽¹⁾ | 0 ⁽¹⁾ | 0 ⁽¹⁾ | 0 ⁽¹⁾ | 0 | 0/1 | 0/1 | 0/1 |
|------------|------------------|------------------|------------------|------------------|---|-----|-----|-----|

Note

- The use of subaddresses F0H to F7H (11110XXX) instead of 00H to 07H (00000XXX) disables the automatic subaddress incrementing allowing continuous writing to a single data byte register (e.g. DAC testing).

Table 3 Overview of subaddresses

| SUB ADDR | POR STATE | DATA BYTES | | | | | | | |
|----------|-----------|------------|-----------|-----------|------------|------------|------------|------------|------------|
| | | alphactr2 | alphactr1 | alphactr0 | alphagain4 | alphagain3 | alphagain2 | alphagain1 | alphagain0 |
| 00H | 00000000 | alphactr2 | alphactr1 | alphactr0 | alphagain4 | alphagain3 | alphagain2 | alphagain1 | alphagain0 |
| 01H | 00000000 | free | algctr6 | algctr5 | algctr4 | algctr3 | algctr2 | algctr1 | algctr0 |
| 02H | 00000000 | tlngain1 | tlngain0 | rengain | negain4 | negain3 | negain2 | negain1 | negain0 |
| 03H | 00000000 | tmdac | tlnim1 | tlnim0 | sumref4 | sumref3 | sumref2 | sumref1 | sumref0 |
| 04H | 00000000 | sdfine7 | sdfine6 | sdfine5 | sdfine4 | sdfine3 | sdfine2 | sdfine1 | sdfine0 |
| 05H | 00011111 | lexton | betactrl1 | betactrl0 | betascl4 | betascl3 | betascl2 | betascl1 | betascl0 |
| 06H | 01100000 | free | ppnctr1 | ppnctr0 | ppnscl4 | ppnscl3 | ppnscl2 | ppnscl1 | ppnscl0 |
| 07H | 00000000 | porr | free | urefsel | cdrwsel | lpsel1 | lpsel0 | meassel1 | meassel0 |

8.1.2 READ MODE

Table 4 Slave address; 35H

| | | | | | | | | |
|---------------|---|---|---|---|---|---|---|---|
| Slave address | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 |
|---------------|---|---|---|---|---|---|---|---|

Table 5 Read byte

| | | | | | | | | |
|-----------|--------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|
| Read byte | por ⁽¹⁾ | 0 ⁽²⁾ | 0 ⁽²⁾ | 0 ⁽²⁾ | 0 ⁽²⁾ | 0 ⁽²⁾ | 0 ⁽²⁾ | 0 ⁽²⁾ |
|-----------|--------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|

Notes

- In read mode the actual POR status can be read.
- The state of unused read bits should not be relied upon; their state may be changed during development.

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8.1.2.1 Examples of valid transmissions to and from the TZA1020

Write: START - 34H - 00H - Data_for_00 - STOP

Write with auto-increment: START - 34H - 00H - data_for_00 - data_for_01 - data_for_02 - STOP

Auto-increment 'wrap around': START - 34H - 07H - data_for_07 - data_for_00 - data_for_01 - STOP

Write without auto-increment: START - 34H - F5H - data_for_05 - data_for_05 - data_for_05 - STOP

Read: START - 35H - data_from_IC - STOP.

8.1.3 CONTROL BYTE SUBADDRESS 00

Table 6 Control bits for alphactrl

| alphactrl2 | alphactrl1 | alphactrl0 | GAIN INPUT CURRENT ALPHA DETECTOR |
|------------|------------|------------|-----------------------------------|
| 0 | 0 | 0 | 0.50 |
| 0 | 0 | 1 | 0.33 |
| 0 | 1 | 0 | 0.25 |
| 0 | 1 | 1 | 0.20 |
| 1 | 0 | 0 | 0.17 |
| 1 | 0 | 1 | 0.14 |
| 1 | 1 | 0 | 0.12 |
| 1 | 1 | 1 | 0.11 |

Table 7 Control bits for alphagain-DAC; note 1

| alphagain4 | alphagain3 | alphagain2 | alphagain1 | alphagain0 | CURRENT alphagain-DAC |
|------------|------------|------------|------------|------------|---------------------------|
| 0 | 0 | 0 | 0 | 0 | 3.125 μ A |
| 0 | 0 | 0 | 0 | 1 | 6.250 μ A |
| 0 | 0 | 0 | 1 | 0 | 9.375 μ A |
| : code | | | | | : |
| | | | | | 100 μ A (code + 1)/32 |
| 1 | 1 | 1 | 0 | 1 | 93.750 μ A |
| 1 | 1 | 1 | 1 | 0 | 96.900 μ A |
| 1 | 1 | 1 | 1 | 1 | 100 μ A |

Note

1. The currents of all DACs is controlled by reference current (I_{RREF}). The given currents are valid at $I_{\text{RREF}} = -900 \mu\text{A}$.

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8.1.4 CONTROL BYTE SUBADDRESS 01

Table 8 Control byte for algctrl switch functions

| algctr6 | algctr5 | algctr4 | algctr3 | algctr2 | algctr1 | algctr0 | DESCRIPTION |
|---------|---------|---------|---------|---------|---------|---------|--|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | POR state |
| 0 | – | 0 | – | – | – | – | current gain alpha CD-R Aoc = 0alpha CD-R circuit power-off |
| 0 | – | 1 | – | – | – | – | current gain alpha CD-R Aoc = 1alpha CD-R circuit power-on |
| 1 | – | 0 | – | – | – | – | current gain alpha CD-R Aoc = 3alpha CD-R circuit power-off |
| 1 | – | 1 | – | – | – | – | current gain alpha CD-R Aoc = 4alpha CD-R circuit power-on |
| – | 0 | – | – | – | – | – | alpha peak detector normal mode |
| – | 1 | – | – | – | – | – | alpha peak detector to level (test) |
| – | – | – | 0 | – | – | – | CD-RW mode 1 |
| – | – | – | 1 | – | – | – | CD-RW mode 2 |
| – | – | – | – | 0 | – | – | alpha CD-R |
| – | – | – | – | 1 | – | – | alpha CD-RW |
| – | – | – | – | – | 0 | 0 | DALPHA gain = 0.25 |
| – | – | – | – | – | 0 | 1 | DALPHA gain = 0.50 |
| – | – | – | – | – | 1 | 0 | DALPHA gain = 0.75 |
| – | – | – | – | – | 1 | 1 | DALPHA gain = 1.00 |

8.1.5 CONTROL BYTE SUBADDRESS 02

Table 9 Control bits for tlngain

| tlngain1 | tlngain0 | GAIN TLN SIGNAL |
|----------|----------|-----------------|
| 0 | 0 | 1.5 |
| 0 | 1 | 3.0 |
| 1 | 0 | 4.5 |
| 1 | 1 | 6.0 |

Table 10 Control bits for rengain

| rengain | DESCRIPTION |
|---------|---------------|
| 0 | 1 normal |
| 1 | 1.3 self test |

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Table 11 Control bits for current negain-DAC; note 1

| negain4 | negain3 | negain2 | negain1 | negain0 | CURRENT negain-DAC |
|---------|---------|---------|---------|---------|---------------------------|
| 0 | 0 | 0 | 0 | 0 | 3.125 μ A |
| 0 | 0 | 0 | 0 | 1 | 6.250 μ A |
| 0 | 0 | 0 | 1 | 0 | 9.375 μ A |
| : | | | | | : |
| code | | | | | 100 μ A (code + 1)/32 |
| 1 | 1 | 1 | 0 | 1 | 93.750 μ A |
| 1 | 1 | 1 | 1 | 0 | 96.900 μ A |
| 1 | 1 | 1 | 1 | 1 | 100 μ A |

Note

1. The currents of all DACs is controlled by reference current (I_{REF}). The given currents are valid at $I_{\text{REF}} = -900 \mu\text{A}$.

8.1.6 CONTROL BYTE SUBADDRESS 03

Table 12 Control bit for tmdac

| tmdac | DESCRIPTION |
|-------|--------------|
| 0 | DAC test off |
| 1 | DAC test on |

Table 13 Control bits for tlnlimit

| tlnlim1 | tlnlim0 | DESCRIPTION |
|---------|---------|--|
| 0 | 0 | clamp off |
| X | 1 | clamp on 1 (0.6 V; $T_{\text{amb}} = 25^\circ\text{C}$) |
| 1 | 0 | clamp on 2 (1.2 V; $T_{\text{amb}} = 25^\circ\text{C}$) |

Table 14 Control bits for current sumref-DAC; note 1

| sumref4 | sumref3 | sumref2 | sumref1 | sumref0 | CURRENT sumref-DAC |
|---------|---------|---------|---------|---------|--------------------------|
| 0 | 0 | 0 | 0 | 0 | 0.468 μ A |
| 0 | 0 | 0 | 0 | 1 | 0.937 μ A |
| 0 | 0 | 0 | 1 | 0 | 1.40 μ A |
| : | | | | | : |
| code | | | | | 15 μ A (code + 1)/32 |
| 1 | 1 | 1 | 0 | 1 | 14.06 μ A |
| 1 | 1 | 1 | 1 | 0 | 14.53 μ A |
| 1 | 1 | 1 | 1 | 1 | 15.00 μ A |

Note

1. The currents of all DACs is controlled by reference current (I_{REF}). The given currents are valid at $I_{\text{REF}} = -900 \mu\text{A}$.

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8.1.7 CONTROL BYTE SUBADDRESS 04

Table 15 Control byte for 8-bit sdfine-DAC; note 1

| sdfine7 | sdfine6 | sdfine5 | sdfine4 | sdfine3 | sdfine2 | sdfine1 | sdfine0 | CURRENT sdfine-DAC |
|---------|---------|---------|---------|---------|---------|---------|---------|---------------------------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0.117 μ A |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0.234 μ A |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0.352 μ A |
| : | | | | | | | | : |
| code | | | | | | | | 30 μ A (code + 1)/256 |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 29.76 μ A |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 29.88 μ A |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 30.0 μ A |

Note

1. The currents of all DACs is controlled by reference current (I_{RREF}). The given currents are valid at $I_{\text{RREF}} = -900 \mu\text{A}$.

8.1.8 CONTROL BYTE SUBADDRESS 05

Table 16 Control bits for betactrl control via 5-bit DAC

| betactrl1 | betactrl0 | CALF BANDWIDTH (Hz) |
|-----------|-----------|---------------------|
| 0 | 0 | 500 |
| 0 | 1 | 1000 |
| 1 | 0 | 2000 |
| 1 | 1 | 4000 |

Table 17 Control bits for betascl control via 5-bit DAC; note 1

| betascl4 | betascl3 | betascl2 | betascl1 | betascl0 | CURRENT betascl-DAC |
|----------|----------|----------|----------|----------|---------------------------|
| 0 | 0 | 0 | 0 | 0 | 3.125 μ A |
| 0 | 0 | 0 | 0 | 1 | 6.250 μ A |
| 0 | 0 | 0 | 1 | 0 | 9.375 μ A |
| : | | | | | : |
| code | | | | | 100 μ A (code + 1)/32 |
| 1 | 1 | 1 | 0 | 1 | 93.750 μ A |
| 1 | 1 | 1 | 1 | 0 | 96.900 μ A |
| 1 | 1 | 1 | 1 | 1 | 100 μ A |

Note

1. The currents of all DACs is controlled by reference current (I_{RREF}). The given currents are valid at $I_{\text{RREF}} = -900 \mu\text{A}$.

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8.1.9 CONTROL BYTE SUBADDRESS 06

Table 18 Control bits for ppnctrl control via 5-bit DAC

| ppnctrl1 | ppnctrl0 | DESCRIPTION |
|----------|----------|--------------------------|
| 1 | 1 | POR state |
| – | 0 | integrator slow disabled |
| – | 1 | integrator slow enabled |
| 0 | – | integrator fast disabled |
| 1 | – | integrator fast enabled |

Table 19 Control bits for ppnscl control via 5-bit DAC; note 1

| ppnscl4 | ppnscl3 | ppnscl2 | ppnscl1 | ppnscl0 | CURRENT ppnscl-DAC |
|---------|---------|---------|---------|---------|---------------------------|
| 0 | 0 | 0 | 0 | 0 | 3.125 μ A |
| 0 | 0 | 0 | 0 | 1 | 6.250 μ A |
| 0 | 0 | 0 | 1 | 0 | 9.375 μ A |
| : | | | | | : |
| code | | | | | 100 μ A (code + 1)/32 |
| 1 | 1 | 1 | 0 | 1 | 93.750 μ A |
| 1 | 1 | 1 | 1 | 0 | 96.900 μ A |
| 1 | 1 | 1 | 1 | 1 | 100 μ A |

Note

- The currents of all DACs is controlled by reference current (I_{RREF}). The given currents are valid at $I_{RREF} = -900 \mu$ A.

8.1.10 CONTROL BYTE SUBADDRESS 07

Table 20 Control bits for porr

| porr | MODE | DESCRIPTION |
|------|-----------|-------------------------|
| 0 | note 1 | |
| 1 | POR reset | reset of POR signal bit |

Note

- When porr is set to logic 1 it ensures that the POR read bit is reset to logic 0. This way a reading of POR is always at logic 1 with the occurrence of an actual power-on I²C-bus register reset and cannot accidentally be caused by other I²C-bus control bits. Bit porr has no control function; it is an 'unused' bit dedicated by name to change the I²C-bus register content from the POR state. Bit POR of the read byte is a wired NOR function that checks all I²C-bus register bits: when the I²C-bus register contents equals the Power-on reset default state POR will read logic 1, also when this state is set via the I²C-bus control. Because a setting of porr = 1 differs from the POR default state it forces a reset to logic 0 of the POR bit independent of other bit settings.

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Table 21 Control bits for meassel

| meassel1 | meassel0 | MEAS1 | MEAS2 |
|----------|----------|----------------------------------|----------------------------------|
| 0 | 0 | $Gc [(Ic1 + Ic4) - (Ic2 + Ic3)]$ | $Gc [(Ic1 + Ic2) - (Ic3 + Ic4)]$ |
| 0 | 1 | $Gs (Ia1 - Ia2)$ | $Gs (Ib2 - Ib1)$ |
| 1 | 0 | $Gs (Ia1 + Ib1)$ | $Gs (Ia2 + Ib2)$ |
| 1 | 1 | $Gs (Ia1 + Ia2)$ | $Gs (Ib2 + Ib1)$ |

Table 22 Control bits for lpsel

| lpsel1 | lpsel0 | BANDWIDTH |
|--------|--------|-----------|
| 0 | 0 | 40 kHz |
| 0 | 1 | 80 kHz |
| 1 | 0 | 160 kHz |
| 1 | 1 | 320 kHz |

Table 23 Control bit for cdrwsel

| cdrwsel | DESCRIPTION |
|---------|-------------|
| 0 | CD-R mode |
| 1 | CD-RW mode |

Table 24 Control bits for urefsel

| urefsel | REFERENCE OUTPUT VOLTAGE |
|---------|--------------------------|
| 0 | 2.9 V |
| 1 | 3.5 V |

Table 25 Read byte

| POR | DESCRIPTION |
|-----|--|
| 0 | I ² C-bus bit state differs from power-on reset state |
| 1 | I ² C-bus bit state equals power-on reset state; note 1 |

Note

1. At power-on, an internal power-on reset signal is generated which resets the I²C-bus data bits to a pre-defined state. When the internal data bits are found to be in a POR state (due to an actual power-on reset but also when set via the I²C-bus) bit POR signals logic 1. Using the POR bit to detect occurrence of a power-on reset requires bit PORR to be set to logic 1 after power-up. Setting bit PORR forces the POR bit to logic 0 independent of other I²C-bus bit settings.

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8.2 Characteristics of the I²C-bus

| SYMBOL | PARAMETER | FAST-MODE I ² C-BUS | | UNIT |
|---------------------|---|---------------------------------------|------|------|
| | | MIN. | MAX. | |
| f _{SCL} | SCL clock frequency | 0 | 400 | kHz |
| t _{BUF} | bus free time between a STOP and START condition | 1.3 | – | μs |
| t _{HD;STA} | hold time (repeated) START condition; after this period, the first clock pulses are generated | 0.6 | – | μs |
| t _{LOW} | LOW period of the SCL clock | 1.3 | – | μs |
| t _{HIGH} | HIGH period of the SCL clock | 0.6 | – | μs |
| t _{SU;STA} | set-up time for a repeated START condition | 0.6 | – | μs |
| t _{HD;DAT} | data hold time | 0 | 0.9 | μs |
| t _{SU;DAT} | data set-up time | 100 | – | ns |
| t _r | rise time of both SDA and SCL signals | 20 + 0.1C _b ⁽¹⁾ | 300 | ns |
| t _f | fall time of both SDA and SCL signals | 20 + 0.1C _b ⁽¹⁾ | 300 | ns |
| t _{SU;STO} | set-up time for STOP condition | 0.6 | – | μs |
| C _b | capacitive load for each bus line; note 1 | – | 400 | pF |

Note

1. C_b = total capacitance of one bus line in pF.

For more information on "The I²C-bus and how to use it" see home page <http://www.semiconductors.philips.com>.

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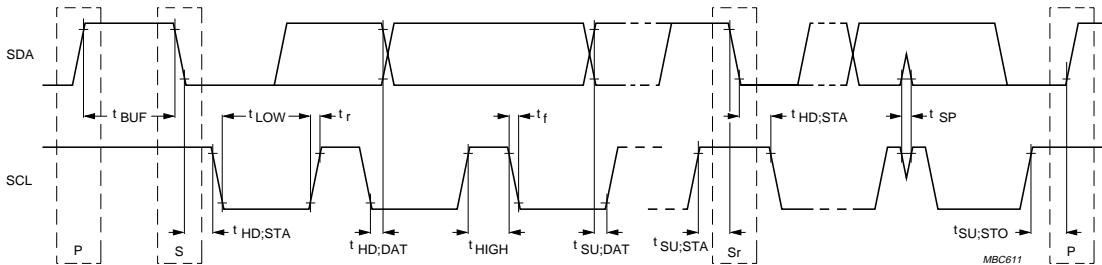


Fig.4 Definition of timing on the I²C-bus.

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Table 26 Scale factors controlled by the I²C-bus interface

| SCALE FACTOR | CONTROL SIGNAL | BINARY VALUE CONTROL SIGNAL | VALUE SCALE FACTOR |
|----------------------|-----------------------|--------------------------------|--------------------|
| RE _{scale} | rengain | 0 | 1 |
| | | 1 | 1.3 |
| TL _{scale} | tlngain1 and tlngain0 | 00 | 1.5 |
| | | 01 | 3.0 |
| | | 10 | 4.5 |
| | | 11 | 6.0 |
| MIR _{scale} | cdrwsel | 0 | 0.05 |
| | | 1 | 0.2 |

Table 27 Currents controlled by the I²C-bus interface; note 1

| NORMALIZER CURRENTS | CONTROL SIGNAL | BINARY VALUE CONTROL SIGNAL | VALUE CURRENT (μA) |
|------------------------|--------------------|--------------------------------|--------------------|
| I _{negain} | negain4 to negain0 | 00000 | 3.125 |
| | | : | : |
| | | 01111 | 50 |
| | | : | : |
| I _{sumref} | sumref4 to sumref0 | 11111 | 100 |
| | | : | : |
| | | 00000 | 0.47 |
| | | : | : |
| I _{sdfine} | sdfine7 to sdfine0 | 01111 | 7.5 |
| | | : | : |
| | | 11111 | 15 |
| | | : | : |
| I _{sdfine} | sdfine7 to sdfine0 | 0000000 | 0.12 |
| | | : | : |
| | | 0111111 | 15 |
| | | : | : |
| I _{ref} | - | 1111111 | 30 |
| | | - | 20 |

Note

1. The currents are proportional to I_{RREF}. The given current values are valid at I_{RREF} = -900 μA.

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9 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

| SYMBOL | PARAMETER | MIN. | MAX. | UNIT |
|-----------|---------------------------------|-------|-------|------|
| V_{DD} | positive supply voltage | 0 | 13.2 | V |
| T_{stg} | storage temperature | -65 | +150 | °C |
| T_{amb} | ambient temperature | 0 | 70 | °C |
| V_{es} | electrostatic handling voltage: | | | |
| | Machine model | -200 | +200 | V |
| | Human body model | -1000 | +1000 | V |

10 THERMAL CHARACTERISTICS

| SYMBOL | PARAMETER | CONDITIONS | VALUE | UNIT |
|---------------|---|-------------|-------|------|
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | in free air | 60 | K/W |

11 CHARACTERISTICS

$V_{DD1} = V_{DD2} = 5$ V; $V_{SS1} = V_{SS2} = -5$ V; $T_{amb} = 25$ °C; $ERON = 1$; $AMON = 0$; $I_{RREF} = -900$ μ A; unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|-----------------|---|-------------------------------|------|------|------|------|
| Supplies | | | | | | |
| V_{DD1} | positive supply voltage 1 (pin 28) | | 4.5 | 5.0 | 5.5 | V |
| V_{SS1} | negative supply voltage 1 (pin 30) | | -5.5 | -5.0 | -4.5 | V |
| V_{DD2} | positive supply voltage 2 (pin 16) | | 4.5 | 5.0 | 5.5 | V |
| V_{SS2} | negative supply voltage 2 (pin 18) | | -5.5 | -5.0 | -4.5 | V |
| ΔV_{DD} | difference between V_{DD1} and V_{DD2} | | -0.5 | - | +0.5 | V |
| ΔV_{SS} | difference between V_{SS1} and V_{SS2} | | -0.5 | - | +0.5 | V |
| $I_{DD(tot)}$ | positive supply current $V_{DD1} + V_{DD2}$ | quiescent state | - | 12 | - | mA |
| | | maximum current | - | 26 | - | mA |
| | | maximum current at $AMON = 1$ | - | 49 | - | mA |
| $I_{SS(tot)}$ | negative supply current $V_{SS1} + V_{SS2}$ | quiescent state | - | 16 | - | mA |
| | | maximum current | - | 25 | - | mA |
| | | maximum current at $AMON = 1$ | - | 33 | - | mA |

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| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|--|---|-----------|-------------|-----------|---------------|
| Reference input current; pin RREF | | | | | | |
| $I_{i(RREF)}$ | input reference current | note 1 | – | –900 | – | μA |
| I_{RREF} | current range | | –1200 | – | –6500 | μA |
| $V_{i(RREF)}$ | input voltage on pin RREF | $I_{RREF} = -900 \mu\text{A}$ referenced to V_{SS} | 1.22 | 1.245 | 1.26 | V |
| Reference voltage buffer; pin UOUT | | | | | | |
| V_{UOUT} | LOW-level output reference voltage | urefsel = 0 | | | | |
| | | $I_{UOUT} = -6 \text{ mA}$ $I_{UOUT} = 0 \text{ mA}$ | 2.63 – | 2.77 2.9 | 2.90 – | V V |
| | HIGH-level output reference voltage | urefsel = 1 | | | | |
| | | $I_{UOUT} = -6 \text{ mA}$ $I_{UOUT} = 0 \text{ mA}$ | 3.23 – | 3.4 3.5 | 3.57 – | V V |
| I_{UOUT} | current range | | –10 | – | 0 | mA |
| C_{UOUT} | capacitance on pin UOUT (necessary for stability) | $I_{UOUT} = -6 \text{ mA}$ | 22 | – | – | nF |
| | | $I_{UOUT} = 0 \text{ mA}$ | 100 | – | – | nF |
| Detector inputs | | | | | | |
| INPUT CURRENT RANGE | | | | | | |
| $I_{i(Cn)}$ | central diode input current for C1 to C4 | AMON = 0 | 1.0 | – | 75 | μA |
| | | AMON = 1 | 0 | – | 4000 | μA |
| $I_{i(SA,SB)}$ | satellite diode input current for SA1/SA2 and SB1/SB2 | AMON = 0 | 0.6 | – | 9 | μA |
| | | AMON = 1 | 0 | – | 520 | μA |
| $I_{i(CAGAIN)}$ | input current for set-point laser power | | 30 | – | 1800 | μA |
| INPUT VOLTAGE LEVEL | | | | | | |
| $V_{i(Cn)}$ | central diode input voltage for C1 to C4 | AMON = 0 | – | 0 | – | V |
| | | AMON = 1 | – | 1.4 | – | V |
| $V_{i(SA,SB)}$ | satellite diode input voltage for SA1/SA2 and SB1/SB2 | AMON = 0 | – | 1.4 | – | V |
| | | AMON = 1 | – | 1.4 | – | V |
| $V_{i(CAGAIN)}$ | input current for set-point laser power | | – | 0.7 | – | V |
| INPUT RESISTANCE | | | | | | |
| $R_{i(Cn)}$ | central diode input resistance for C1 to C4 | AMON = 0 | – | 300 | – | Ω |
| | | AMON = 1; $I_{i(cd)} = 25 \mu\text{A}$ lexton = 1 | – | 600 | – | Ω |
| | | lexton = 0 | – | 1000 | – | Ω |
| $R_{i(SA,SB)}$ | satellite diode input resistance for SA1/SA2 and SB1/SB2 | $I_{i(SA,SB)} = 6.25 \mu\text{A}$ lexton = 1 | – | 1000 | – | Ω |
| | | lexton = 0 | – | 4000 | – | Ω |
| $R_{i(CAGAIN)}$ | input resistance for set-point laser power | $I_{i(CAGAIN)} = 35 \mu\text{A}$ | – | 700 | – | Ω |

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| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|--|----------------------------------|------------------------------------|------|------|------|---------------|
| Digital control signals | | | | | | |
| INPUT VOLTAGE LEVELS; PINS ERON, ASTROBE, AINTON, ALS, SDA, SCL AND AMON | | | | | | |
| V_{IL} | LOW-level input voltage | $V_{DD1} = V_{DD2} = 5.0\text{ V}$ | -0.3 | - | +0.9 | V |
| V_{IH} | HIGH-level input voltage | $V_{DD1} = V_{DD2} = 5.0\text{ V}$ | 2.3 | - | 5.3 | V |
| OUTPUT VOLTAGE LEVEL; PIN SDA | | | | | | |
| V_{OH} | LOW-level output voltage | $V_{DD1} = 5.0\text{ V}$ | 4.5 | - | 5.0 | V |
| V_{OL} | HIGH-level output voltage | | 0 | - | 0.5 | V |
| INPUT CURRENT | | | | | | |
| I_{LI} | input leakage current | | | | | |
| | pins SDA, SCL, AMON and ALS | | -1.5 | - | 0 | μA |
| | pin ERON | | -15 | - | 0 | μA |
| | pins AINTON and ASTROBE | | -100 | 0 | +100 | nA |
| DELAY TIMES | | | | | | |
| t_d | delay time | | | | | |
| | pins ASTROBE and AINTON | | - | 15 | - | ns |
| | pins SDA, SCL, AMON and ALS | | - | 36 | 50 | ns |
| | pin ERON | | - | 2.5 | 3.5 | ns |
| Normalized servo signals; note 2 and Section 11.1 | | | | | | |
| GAIN SETTINGS | | | | | | |
| G_{fe} | gain focus error signal | ERON = 1 | 0.22 | 0.24 | 0.26 | |
| | | ERON = 0 | - | 0 | - | |
| G_{re} | gain radial error signal | ERON = 1 | 0.87 | 0.95 | 1.03 | |
| | | ERON = 0 | - | 0 | - | |
| G_{tl} | gain track loss signal | ERON = 1 | 0.87 | 0.95 | 1.03 | |
| | | ERON = 0 | - | 0 | - | |
| G_{xd} | gain radial beam landing | ERON = 1 | 0.87 | 0.95 | 1.03 | |
| | | ERON = 0 | - | 0 | - | |
| G_{gr} | gain in grating ratio correction | ERON = 1 | 0.94 | 1 | 1.06 | |
| G_{mir} | gain in mirror signal | ERON = 1 | 0.90 | 1.03 | 1.15 | |

Pre-amplifiers for CD-RW systems

TZA1020; TZA1020A

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|--|-------------------------|------|------|------|------------------|
| OFFSET CURRENTS | | | | | | |
| $I_{\text{offset(fe)}}$ | offset current focus error | | -550 | 0 | +550 | nA |
| $I_{\text{offset(re)}}$ | offset current radial error | rengain = 0 | -1.5 | 0 | +1.5 | μA |
| $I_{\text{offset(tl)}}$ | offset current track loss | tlngain(1,0) = 00 | -4 | 0 | +4 | μA |
| $I_{\text{offset(xd)}}$ | offset radial beam landing | | -1.5 | 0 | +1.5 | μA |
| $\Delta I_{\text{offset(re)}}$ | variation in offset current radial error | AMON 0 \rightarrow 1 | -0.8 | 0 | +0.8 | μA |
| $\Delta I_{\text{offset(tl)}}$ | variation in offset current track loss | AMON 0 \rightarrow 1 | -1.4 | -0.2 | +1.2 | μA |
| OUTPUT IMPEDANCE | | | | | | |
| $Z_{\text{o(FEN)}}$ | output impedance pin FEN | | - | 40 | - | $\text{M}\Omega$ |
| $Z_{\text{o(REN)}}$ | output impedance pin REN | | - | 21 | - | $\text{M}\Omega$ |
| $Z_{\text{o(XDN)}}$ | output impedance pin XDN | | - | 21 | - | $\text{M}\Omega$ |
| $Z_{\text{o(TLN)}}$ | output impedance pin TLN | | - | 15 | - | $\text{M}\Omega$ |
| $Z_{\text{o(MIRN)}}$ | output impedance pin MIRN | | - | 80 | - | $\text{M}\Omega$ |
| VOLTAGE RANGE OF OUTPUT SIGNALS | | | | | | |
| $V_{\text{o(FEN)}}$ | output voltage pin FEN | | -4 | - | +4 | V |
| $V_{\text{o(REN)}}$ | output voltage pin REN | | -4 | - | +4 | V |
| $V_{\text{o(XDN)}}$ | output voltage pin XDN | | -4 | - | +4 | V |
| $V_{\text{o(l)(TLN)}}$ | output voltage pin TLN | tlnlm(1,0) = 00; note 3 | -4 | - | +3 | V |
| | | tlnlm(1,0) = X1; note 3 | -1 | - | +1 | V |
| | | tlnlm(1,0) = 10; note 3 | -2 | - | +2 | V |
| $V_{\text{o(l)(MIRN)}}$ | output voltage linear range pin MIRN; TZA1020 | note 4 | 0.2 | - | 1.0 | V |
| $V_{\text{o(l)(MIRN)}}$ | output voltage linear range pin MIRN; TZA1020A | note 4 | 0.2 | - | 4.0 | V |
| BANDWIDTH | | | | | | |
| $B_{-3\text{dB}}$ | -3 dB bandwidth | | 48 | 60 | 72 | kHz |
| $\Delta B_{-3\text{dB}}$ | relative variation of $B_{-3\text{dB}}$ over total input current range | | - | - | 4 | % |
| Fast track count; see Table 28 and notes 5 and 6 | | | | | | |
| GAIN SETTINGS | | | | | | |
| $Z_{\text{tr(FTC)}}$ | transimpedance of fast track circuit | cdrwsel = 0 | 4 | 5 | 6 | k Ω |
| | | cdrwsel = 1 | 16 | 20 | 24 | k Ω |
| | | AMON = 1 | - | 0 | - | k Ω |
| G_{gr} | gain in grating ratio correction | | 0.94 | 1.00 | 1.06 | |
| $\Delta V_{\text{RE-NOM(p-p)}}$ | nominal signal swing (peak-to-peak value) | | - | 1 | - | V |

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| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|--|--|---|------|------|------|----------|
| $TS_{Ztr(FTC)}$ | temperature sensitivity for transimpedance of fast track circuit | | – | 0.2 | – | %/K |
| FAST TRACK COUNT SIGNAL VOLTAGE OUTPUT; PIN RE | | | | | | |
| $V_{o(RE)}$ | output voltage range | | –3.5 | – | +2.5 | V |
| $V_{offset(RE)}$ | output offset voltage | cdrwsel = 0 | –40 | 0 | +40 | mV |
| | | cdrwsel = 1 | –100 | +25 | +150 | mV |
| $R_{o(RE)}$ | output resistance | minimum diode currents | – | 125 | – | Ω |
| | | | – | 580 | – | Ω |
| $B_{-3dB(RE)}$ | bandwidth of RE signal | $C_L = 20$ pF; valid for complete input current range | 800 | – | – | kHz |
| Spot position measurements; see Table 29 and note 7 | | | | | | |
| GAIN SETTINGS | | | | | | |
| G_{cd} | gain central diode current combination | AMON = 0 | 0.45 | 0.50 | 0.55 | |
| | | AMON = 1 | – | 0 | – | |
| G_{sd} | gain satellite diode current combinations | AMON = 0 | 0.9 | 1.00 | 1.1 | |
| | | AMON = 1 | – | 0 | – | |
| OFFSET CURRENTS | | | | | | |
| $I_{offset(MEAS)}$ | offset of MEAS1 current | meassel = 00 | –1.6 | 0 | +1.6 | μ A |
| | | meassel = 01 | –1.6 | 0 | +1.6 | μ A |
| | offset of MEAS2 current | meassel = 00 | –1.6 | 0 | +1.6 | μ A |
| | | meassel = 01 | –1.6 | 0 | +1.6 | μ A |
| Central aperture high frequency output | | | | | | |
| $G_{I(CAHF)}$ | current gain | cdrwsel = 0; $\Sigma I_{C1} = 180$ μ A | 7.5 | 8.25 | 9.0 | |
| | | cdrwsel = 1; $\Sigma I_{C1} = 50$ μ A | 30 | 35 | 38 | |
| $I_{offset(CAHF)}$ | offset current at zero input current | cdrwsel = 0; $\Sigma I_{C1} = 0$ μ A | – | 100 | | μ A |
| f_{-3dB} | bandwidth (–3 dB), valid for total current range | $C_i = 12$ pF; note 8 | 17 | – | – | MHz |
| | | $C_i = 5$ pF | 19 | – | – | MHz |
| Δt_d | delay variations valid for total current range | f = 0.1 to 12 MHz | | | | |
| | | $C_i = 12$ pF | – | – | 0.9 | ns |
| | | $C_i = 5$ pF | – | – | 1.1 | ns |

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| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|--|-------|-------|------|---------------------------|
| Laser power calibration signals (beta circuit); see Fig.5 and Table 30 | | | | | | |
| $I_{p1} = I_{p2} = 10 \text{ TO } 90 \mu\text{A}; 2.1 \times I_{p1}; I_{\text{betascl}} = I_{p1}$ | | | | | | |
| $V_{\text{ref(beta)}}$ | reference voltage for beta detector | AMON = 0 | 1.1 | 1.25 | 1.4 | V |
| | | AMON = 1 | – | 0 | – | V |
| V_{A1}/V_{A2} | ratio between A1 and A2 | | 0.9 | 1 | 1.1 | – |
| V_{A1}/V_{CALF} | ratio between CALF and A1 | | 0.8 | 1 | 1.2 | – |
| $\Sigma I_{C1} = 100 \mu\text{A}; I_{\text{betascale}} = I_{p1}$ | | | | | | |
| $B_{-3\text{dB}}$ | bandwidth (–3 dB) of CALF and CALFI signal | $C_{\text{CALPF}} = 15 \text{ nF}$ betactrl = 00 | – | 500 | – | Hz |
| | | betactrl = 01 | – | 1000 | – | Hz |
| | | betactrl = 10 | – | 2000 | – | Hz |
| | | betactrl = 11 | – | 4000 | – | Hz |
| t_{cpeak} | time constant peak detector | $C_{\text{HCA1}} = C_{\text{HCA2}} = 10 \text{ nF}$ betactrl = 00 | – | 500 | – | μs |
| | | betactrl = 01 | – | 250 | – | μs |
| | | betactrl = 10 | – | 125 | – | μs |
| | | betactrl = 11 | – | 60 | – | μs |
| R_o | output resistance pins A1, A2 and CALF | | – | 250 | – | Ω |
| V_o | output voltage pins A1, A2 and CALF | $V_{\text{DD1}} = 5.0 \text{ V}$ | 0 | – | 4.5 | V |
| Laser power calibration signals (alpha circuit); see note 9 and Tables 31 and 32 | | | | | | |
| GAIN SETTINGS | | | | | | |
| $G_{\text{alpha(}CD\text{-RW)}}$ | gain in alpha CD-RW circuit | ERON = 1 | 0.88 | 1 | 1.12 | |
| | | ERON = 0 | – | 0 | – | |
| $G_{\text{CD-R(i)}}$ | gain in CD-R input circuit | AINTON = 1 | 0.53 | 0.62 | 0.72 | |
| $G_{\text{CD-R(norm)}}$ | gain in CD-R normalizer | ASTROBE = 1 | 38126 | 48158 | 6190 | $\mu\text{A/V}$ |
| G_{sub} | subtractor gain | ALS = 1 | 0.94 | 0.97 | 1.0 | |
| | | ALS = 0 | – | 0 | – | |
| $\Delta V_{\text{AINT-ASTROBE}}$ | change in voltage measured behind ASTROBE switch | ASTROBE 1 \rightarrow 0 | – | 130 | – | mV |
| V_{AINT} | voltage range pin AINT | | 0.5 | – | 3 | V |
| B_{lpf} | bandwidth of low-pass filter | ERON = 1 | 48 | 60 | 72 | kHz |
| I_{peak} | current to peak detector | | 0.3 | – | 2 | mA |
| $I_{\text{L(peak)}}$ | leakage current of peak detector | algctr6 = 1; algctr4 = 0 | – | 100 | – | $\mu\text{A}/\mu\text{s}$ |
| t_{cpeak} | time constant peak detector time discrete to time continues | switching AINTON at realistic data speed = N | – | 5/N | – | μs |

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| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|--|--|-------|-------|-------|-------------------|
| V_{AZIN} | voltage on AZIN input node | $I_{AZIN} = 100 \mu A$ | – | 0 | – | mV |
| | | $I_{AZIN} = 10 \mu A$ | – | –60 | – | mV |
| $V_{O(DALPHA)}$ | output voltage pin DALPHA | | –3.5 | – | +3.5 | V |
| $R_{SW(AINTON)}$ | resistance AINTON switch | | – | 50 | – | Ω |
| Wobble pre-processor; see note 10 and Table 33 | | | | | | |
| LPF2 | | | | | | |
| $B_{-3dB(LPF2)}$ | bandwidth (–3 dB) of LPF2 | $lp sel = 00$ | 32 | 40 | 48 | kHz |
| | | $lp sel = 01$ | 64 | 80 | 96 | kHz |
| | | $lp sel = 10$ | 120 | 150 | 180 | kHz |
| | | $lp sel = 11$ | 240 | 300 | 360 | kHz |
| ΔB_{LPF2} | relative variation B_{LPF2} over input current range | note 10 | – | – | 6 | % |
| VARIABLE GAIN LOOP | | | | | | |
| k_{bal} | sensitivity balance circuit | | – | 1 | – | V^{-1} |
| G_{bal} | gain balancing circuit | $cdrw sel = 0$ | 0.758 | 0.889 | 0.951 | |
| | | $cdrw sel = 1$ | 3.0 | 3.5 | 3.84 | |
| I_l/I_r | input current range of balancing circuit | | 0.5 | – | 2 | |
| SR_{loop} | slew rate loop | $ppnctr1 = 0$ | – | 6200 | – | V/s |
| | | | – | 0 | – | V/s |
| $B_{-3dB(bal)}$ | bandwidth variable gain loop | $I_{op} = I_{on} = 0 \mu A$; note 11 | 800 | 1000 | 1250 | kHz |
| | | $ppnctr1 = 0$; note 11 | – | 0 | – | kHz |
| MULTIPLIER LOOP | | | | | | |
| $V_{PPN(norm)}$ | normalize voltage pin PPN | | – | 3.14 | – | V |
| R_{ca} | resistance ca | $AMON = 0$ | – | 8 | – | k Ω |
| | | $AMON = 1$ | – | – | 1 | k Ω |
| $B_{-3dB(HPF)}$ | bandwidth (–3 dB) of HPF | | 40 | 50 | 60 | kHz |
| k_{mult} | sensitivity multiplier | | – | 0.19 | – | mA/V ² |
| $g_{m(V-I)}$ | transconductance $V \rightarrow I$ | $ V_p - V_{ref(V-I)} < 0.354 V$; note 12 | – | 340 | – | $\mu A/V$ |
| | | $ppnctr2 = 0$ | – | 0 | – | $\mu A/V$ |
| $V_{ref(V-I)}$ | reference voltage $V \rightarrow I$ | | 3.25 | 3.5 | 3.75 | V |

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| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|--------------------------|---|--|---------------|-----------|---------------|----------|
| OUTPUT STAGE; note 13 | | | | | | |
| V _{PPN} | voltage range | | -3.5 | - | +2.5 | V |
| R _(I-V) | I → V conversion resistance | | 244 | 320 | 400 | kΩ |
| V _{offset(PPN)} | offset voltage of PPN signal | I _{ppnscl} = 3.125 μA | -38 | +6 | +50 | mV |
| | | I _{ppnscl} = 100 μA | -1 165 | +80 | +1 325 | mV |
| | | ppnctrl1 = 0 I _{ppnscl} = 3.125 μA I _{ppnscl} = 100 μA | -115 -3800 | +6 +80 | +130 +4000 | mV mV |
| R _{O(PPN)} | output resistance PPN signal | I _{ppnscl} = 3.125 μA | - | 2200 | - | Ω |
| | | I _{ppnscl} = 20 μA | - | 400 | - | Ω |
| TS _{R(I-V)} | temperature sensitivity of offset voltage of PPN signal | | - | 0.2 | - | %/°C |
| B _{-3dB(PPN)} | internal signal bandwidth of PPN circuit | | - | 1 | - | MHz |

Notes

- In the application, the reference current will be generated by means of a resistor. The given current can be realized by a resistor of 1.3844 kΩ. As these are not available, the actual reference current will be slightly different. This means that all derived signal currents will be scaled in the same way.
- I_{C1} = I_{C2} = I_{C3} = I_{C4} = 10 μA; I_{SA1} = I_{SA2} = I_{SB1} = I_{SB2} = 1.25 μA; I_{ngain} = 50 μA; I_{sdfine} = 20 μA; I_{RREF} = -900 μA; I_{cagain} = 35 μA; ERON = 1.
- The voltage on TLN can be clamped with respect to GND (positive and negative) with one or two diodes. The clamp has an internal resistance of approximately 900 Ω.
- In the TZA1020A, pin MIRN is clamped with respect to GND (positive) by means of one diode.
- I_{C1} = I_{C2} = I_{C3} = I_{C4} = 25 μA; I_{SA1} = I_{SA2} = I_{SB1} = I_{SB2} = 3.125 μA; I_{sdfine} = 20 μA; I_{RREF} = -900 μA.
- $$V_{RE} = -T_{rre} \times \left[(I_{C1} + I_{C4}) - (I_{C2} + I_{C3}) - \frac{4 \times G_{gr} \times (I_{ref} + I_{sdfine})}{I_{ref}} \times ((I_{SA1} + I_{SB1}) - (I_{SA2} + I_{SB2})) \right]$$
- I_{C1} = I_{C2} = I_{C3} = I_{C4} = 25 μA; I_{SA1} = I_{SA2} = I_{SB1} = I_{SB2} = 3.125 μA.
- C_i = total capacitance connected to all input pins C1 to C4 (between pin and ground).
- ΣI_{C1} = 2e-3 · (1 + 0.7 sin(12π · 3e6 · t)) μA; I_{SA1} = I_{SB1} = I_{SA2} = I_{SB2} = 25 μA; I_{MIRN} = 15 μA; I_{alphagain} = 50 μA; I_{sumref} = 15 μA; I_{AZIN} = 100 μA; AMON = 1; alphactrl(2 to 0) = 000; algctr4 = 00; algctr6 = 1; algctr5 = 0; I_{CAGAIN} = 200 μA.
- I_{C1} = I_{C2} = I_{C3} = I_{C4} = 25 μA; I_{ppnscl} = 50 μA; ppnctrl1 = 1, ppnctrl2 = 1.
- Bandwidth = $\frac{S_{floop} \times k_{bal}}{2\pi}$.
- I_{op} and I_{on} are limited to 12 μA ± 3 μA.
- $$V_{PPN} = \left(\frac{L-R}{L+R} \right) \times R_{(I-V)} \times I_{ppnscl}$$

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Table 28 Fast track count; note 1

| FTC CURRENTS | CONTROL SIGNAL | BINARY VALUE CONTROL SIGNAL | VALUE CURRENT (μA) |
|----------------------|--------------------|--------------------------------|---------------------------------|
| $I_{\text{sd-fine}}$ | sdfine7 to sdfine0 | 0000000 | 0.12 |
| | | : | : |
| | | 0111111 | 15 |
| | | : | : |
| | | 1111111 | 30 |
| I_{ref} | – | – | 20 |

Note

- The currents are proportional to I_{RREF} . The given current values are valid at $I_{\text{RREF}} = -900 \mu\text{A}$.

Table 29 Spot position measurements

| meassel CODE | I_{MEAS1} | I_{MEAS2} |
|--------------|---|---|
| 00 (POR) | $G_{\text{cd}} [(I_{\text{C1}} + I_{\text{C4}}) - (I_{\text{C2}} + I_{\text{C3}})]$ | $G_{\text{cd}} [(I_{\text{C1}} + I_{\text{C2}}) - (I_{\text{C3}} + I_{\text{C4}})]$ |
| 01 | $G_{\text{sd}} (I_{\text{SA1}} - I_{\text{SA2}})$ | $G_{\text{sd}} (I_{\text{SB2}} - I_{\text{SB1}})$ |
| 10 | $G_{\text{sd}} (I_{\text{SA1}} + I_{\text{SB1}})$ | $G_{\text{sd}} (I_{\text{SA2}} + I_{\text{SB2}})$ |
| 11 | $G_{\text{sd}} (I_{\text{SA1}} + I_{\text{SA2}})$ | $G_{\text{sd}} (I_{\text{SB1}} + I_{\text{SB2}})$ |

Table 30 Laser power calibration (beta circuit); note 1

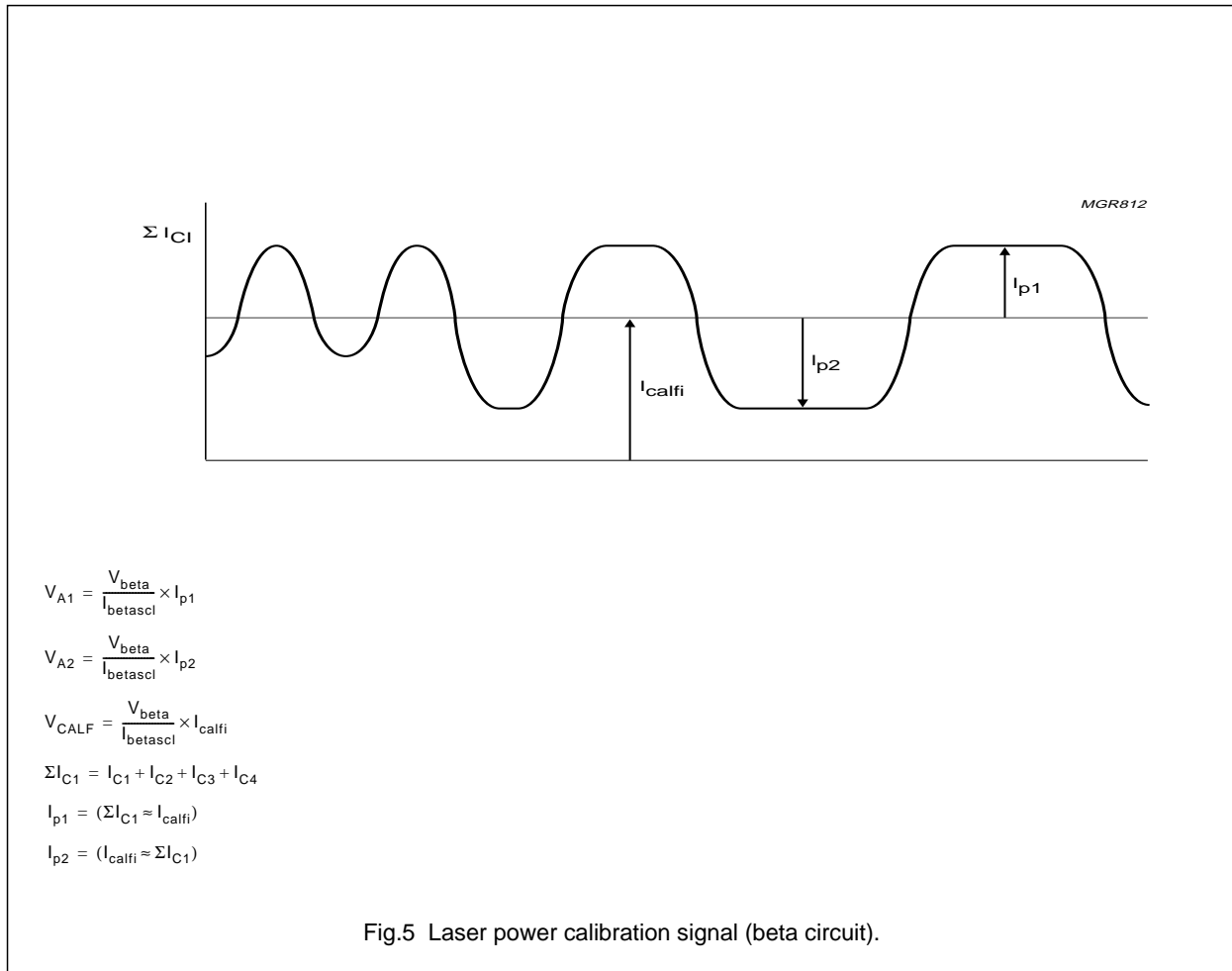
| BETA CIRCUIT CURRENTS | CONTROL SIGNAL | BINARY VALUE CONTROL SIGNAL | VALUE CURRENT (μA) |
|--------------------------|----------------------|--------------------------------|---------------------------------|
| I_{betascl} | betascl4 to betascl0 | 00000 | 3.125 |
| | | : | : |
| | | 01111 | 50 |
| | | : | : |
| | | 11111 | 100 |

Note

- The currents are proportional to I_{RREF} . The given current values are valid $I_{\text{RREF}} = -900 \mu\text{A}$.

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11.1 Transfer functions for normalized servo signals

$$I_{FEN} = G_{fe} \times \left(\frac{I_{C1} - I_{C4}}{I_{C1} + I_{C4}} + \frac{I_{C3} - I_{C2}}{I_{C3} + I_{C2}} \right) \times I_{negdoc}$$

$$I_{XDN} = G_{xd} \times \left(\frac{(I_{C1} + I_{C4}) - (I_{C2} + I_{C3}) - G_{sat} \times (I_{S1} - I_{S2})}{I_{C1} + I_{C2} + I_{C3} + I_{C4} + G_{sat} \times (I_{S1} + I_{S2})} \right) \times I_{negdoc}$$

$$I_{REN} = G_{re} \times RE_{scale} \times \left(\frac{(I_{C1} + I_{C4}) - (I_{C2} + I_{C3}) - G_{sat} \times (I_{S1} - I_{S2})}{I_{C1} + I_{C2} + I_{C3} + I_{C4} + G_{sat} \times (I_{S1} + I_{S2})} \right) \times I_{negdoc}$$

$$I_{TLN} = G_{tl} \times TL_{scale} \times \left(\frac{(I_{C1} + I_{C4}) - (I_{C2} + I_{C3}) - G_{sat} \times (I_{S1} - I_{S2})}{I_{C1} + I_{C2} + I_{C3} + I_{C4} + G_{sat} \times (I_{S1} + I_{S2})} \right) \times I_{negdoc}$$

$$I_{MIRN} = -G_{mir} \times MIR_{scale} \times \left(\frac{(I_{C1} + I_{C4}) - (I_{C2} + I_{C3}) - G_{sat} \times (I_{S1} - I_{S2})}{I_{CAGAIN}} \right) \times I_{negain}$$

$$I_{negdoc} = I_{negain} \times \left(\frac{I_{C1} + I_{C2} + I_{C3} + I_{C4}}{I_{sumref}} \right) \quad \text{at } I_{C1} + I_{C2} + I_{C3} + I_{C4} < 0.9 I_{sumref}$$

$$I_{negdoc} = I_{negain} \times \left(\frac{I_{C1} + I_{C2} + I_{C3} + I_{C4}}{I_{sumref}} \right) \quad \text{at } I_{C1} + I_{C2} + I_{C3} + I_{C4} > 1.1 I_{sumref}$$

$$I_{negdoc} = I_{negain} \times \left(\frac{I_{C1} + I_{C2} + I_{C3} + I_{C4}}{I_{sumref}} \right) \quad \text{at } I_{C1} + I_{C2} + I_{C3} + I_{C4} > 1.1 I_{sumref}$$

$$I_{S1} = I_{SA1} + I_{SB1}, I_{S2} = I_{SA2} + I_{SB2}$$

$$G_{sat} = \frac{4 \times G_{gr} \times (I_{ref} + I_{sdfine})}{I_{ref}}$$

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11.2 Laser power control signals (alpha circuit)

The alpha circuit can be split into an alpha circuit for CD-RW, an alpha circuit for CD-R and a subtractor with additional gain switching. The alpha circuit is active only if AMON = 1.

Table 31 Alpha scale factors

| SCALE FACTOR | CONTROL SIGNAL | BINARY VALUE CONTROL SIGNAL | VALUE SCALE FACTOR |
|---------------------|--------------------------|--------------------------------|--------------------|
| gain input current | alphactrl2 to alphactrl0 | 000 | 0.50 |
| | | 001 | 0.33 |
| | | 010 | 0.25 |
| | | 011 | 0.20 |
| | | 100 | 0.17 |
| | | 101 | 0.14 |
| | | 110 | 0.12 |
| | | 111 | 0.11 |
| current gain output | algctrl4 and Algctrl6 | 00 | 0 |
| | | 01 | 1 |
| | | 10 | 3 |
| | | 11 | 4 |
| subtractor gain | algctrl1 and algctrl0 | 00 | 0.25 |
| | | 01 | 0.5 |
| | | 10 | 0.75 |
| | | 11 | 1.0 |

Table 32 Alpha currents; note 1

| ALPHA CIRCUIT CURRENTS | CONTROL SIGNAL | BINARY VALUE CONTROL SIGNAL | VALUE CURRENT (μA) |
|---------------------------|--------------------------|--------------------------------|---------------------------------|
| $I_{\text{alphagain}}$ | alphagain4 to alphagain0 | 00000 | 3.125 |
| | | 01111 | 50 |
| | | 11111 | 100 |
| I_{ref} | — | — | 20 |

Note

1. The currents and gain factor are proportional to I_{RREF} . The given current values are valid at $I_{\text{RREF}} = -900 \mu\text{A}$.

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11.3 Wobble pre-processor**Table 33** Wobble currents; note 1

| WOBBLE CURRENTS | CONTROL SIGNAL | BINARY VALUE CONTROL SIGNAL | VALUE CURRENT (μA) |
|---------------------|--------------------|--------------------------------|---------------------------------|
| I_{ppnsc1} | ppnsc14 to ppnsc10 | 00000 | 3.125 |
| | | : | : |
| | | 01111 | 50 |
| | | : | : |
| | | 11111 | 100 |

Note

1. The currents are proportional to I_{RREF} . The given current values are valid at $I_{\text{RREF}} = -900 \mu\text{A}$.

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12 APPLICATION AND TEST INFORMATION

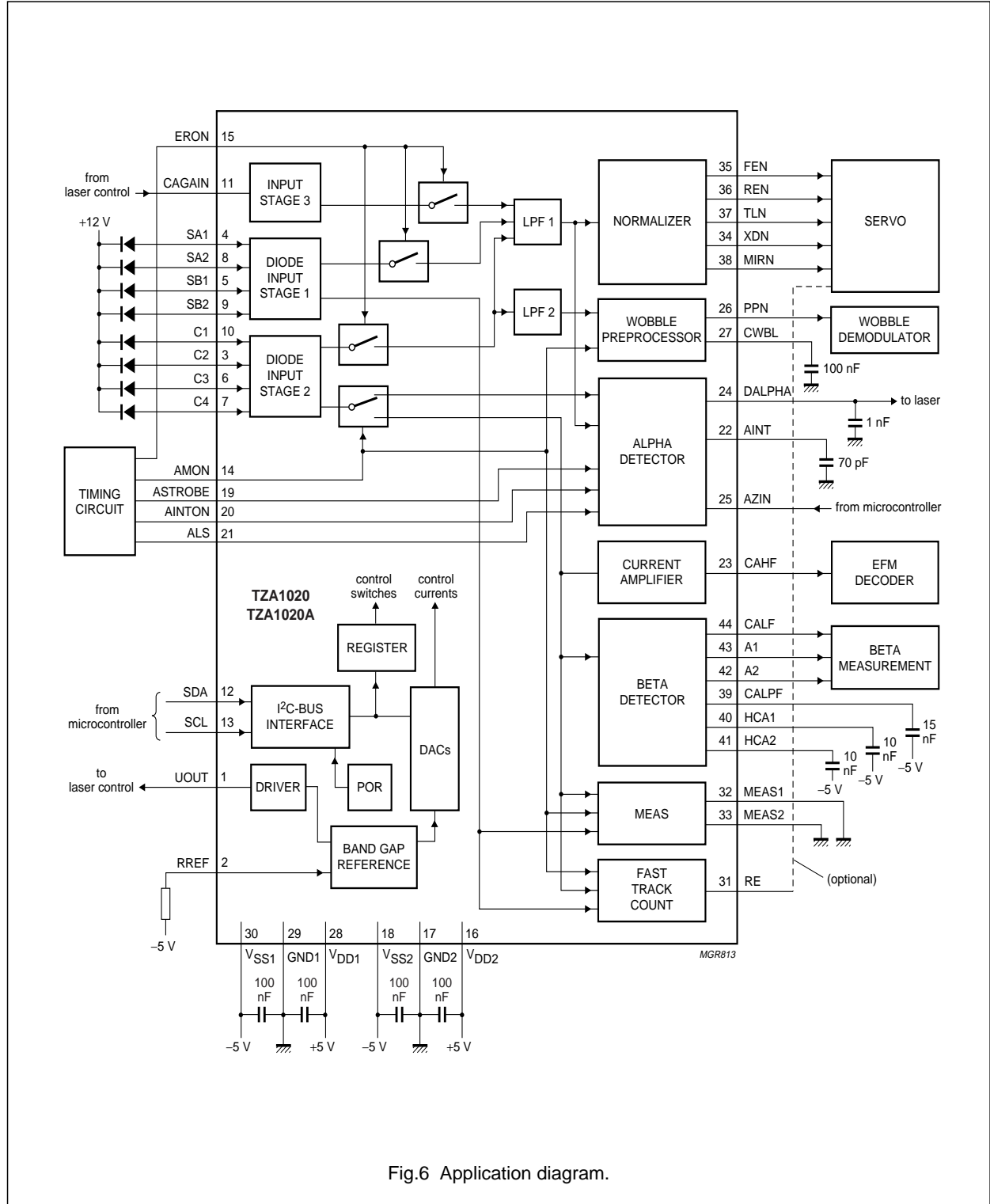


Fig.6 Application diagram.

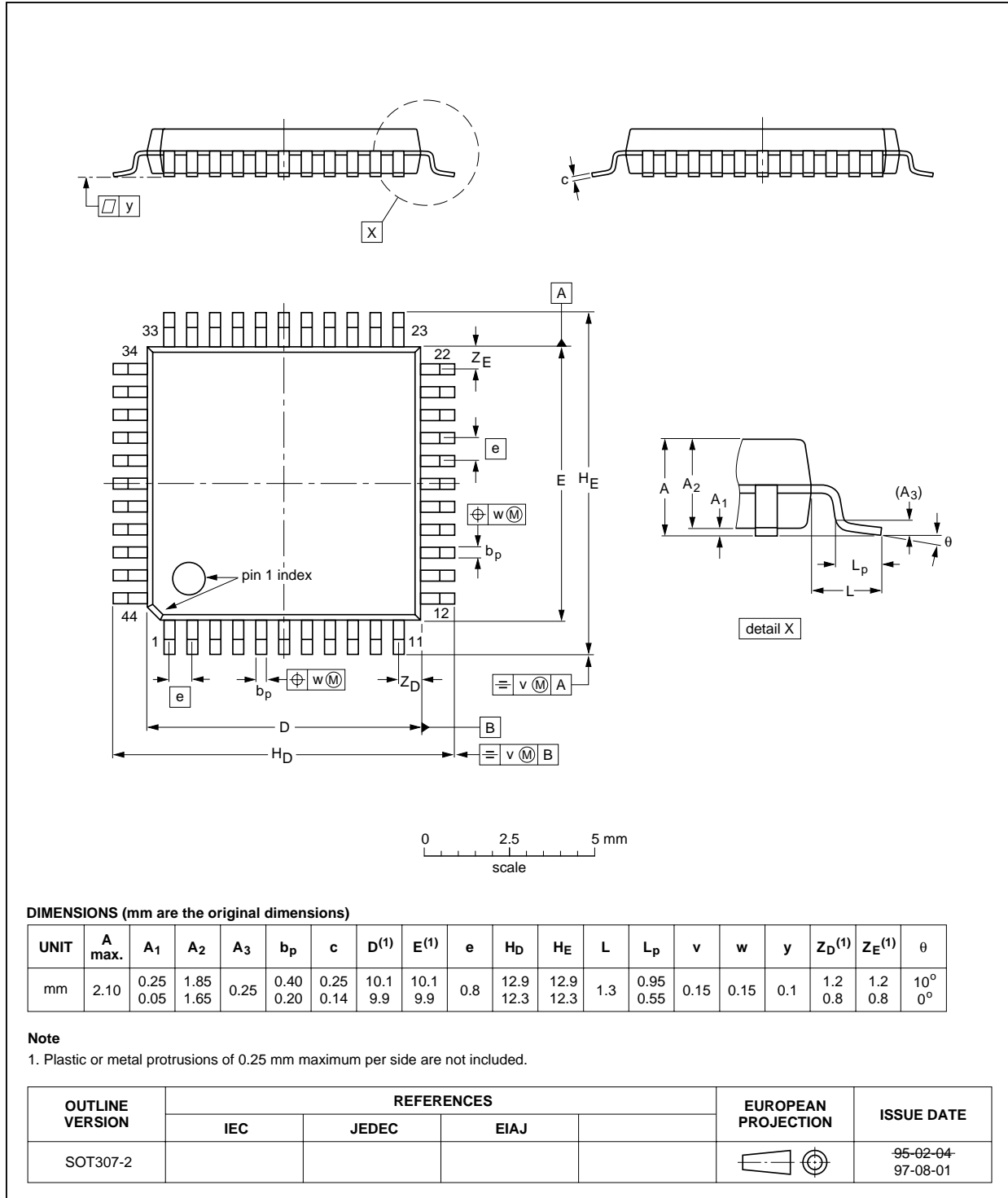
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13 PACKAGE OUTLINE

QFP44: plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 x 10 x 1.75 mm

SOT307-2



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14 SOLDERING

14.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

14.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferably be kept below 230 °C.

14.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
 - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
 - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

14.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Pre-amplifiers for CD-RW systems

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14.5 Suitability of surface mount IC packages for wave and reflow soldering methods

| PACKAGE | SOLDERING METHOD | |
|---------------------------------|-----------------------------------|-----------------------|
| | WAVE | REFLOW ⁽¹⁾ |
| BGA, SQFP | not suitable | suitable |
| HLQFP, HSQFP, HSOP, HTSSOP, SMS | not suitable ⁽²⁾ | suitable |
| PLCC ⁽³⁾ , SO, SOJ | suitable | suitable |
| LQFP, QFP, TQFP | not recommended ⁽³⁾⁽⁴⁾ | suitable |
| SSOP, TSSOP, VSO | not recommended ⁽⁵⁾ | suitable |

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

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15 DATA SHEET STATUS

| DATA SHEET STATUS | PRODUCT STATUS | DEFINITIONS ⁽¹⁾ |
|---------------------------|----------------|--|
| Objective specification | Development | This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice. |
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Note

1. Please consult the most recently issued data sheet before initiating or completing a design.

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