

Silicon NPN Power Transistors

2SC2815

DESCRIPTION

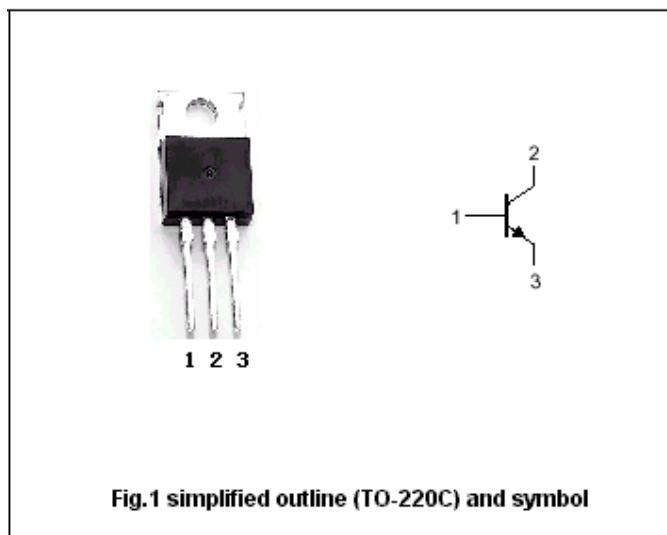
- With TO-220C package
- High voltage;high speed
- Low collector saturation voltage

APPLICATIONS

- For use in horizontal deflection output stages of TV's and CTV's circuits

PINNING

PIN	DESCRIPTION
1	Base
2	Collector;connected to mounting base
3	Emitter



Absolut maximum ratings (Ta=25°C)

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V_{CBO}	Collector-base voltage	Open emitter	300	V
V_{CEO}	Collector-emitter voltage	Open base	250	V
V_{EBO}	Emitter-base voltage	Open collector	6	V
I_C	Collector current		5	A
P_{tot}	Total power dissipation	$T_C=25^\circ\text{C}$	40	W
T_j	Junction temperature		150	$^\circ\text{C}$
T_{stg}	Storage temperature		-65~150	$^\circ\text{C}$

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CHARACTERISTICS

T_j=25°C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V _{CEO(SUS)}	Collector-emitter sustaining voltage	I _C =50mA ; I _B =0	250			V
V _{(BR)CBO}	Collector-base breakdown voltage	I _C =1mA ; I _E =0	300			V
V _{(BR)EBO}	Emitter-base breakdown voltage	I _E =1mA ; I _C =0	6			V
V _{CEsat}	Collector-emitter saturation voltage	I _C =4A ; I _B =0.4A			1.0	V
V _{BEsat}	Base-emitter saturation voltage	I _C =4A ; I _B =0.4A			1.2	V
I _{CBO}	Collector cut-off current	V _{CB} =300V ; I _E =0			0.1	mA
I _{EBO}	Emitter cut-off current	V _{EB} =6.0V ; I _C =0			0.1	mA
h _{FE}	DC current gain	I _C =2.5A ; V _{CE} =5V	40			

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PACKAGE OUTLINE

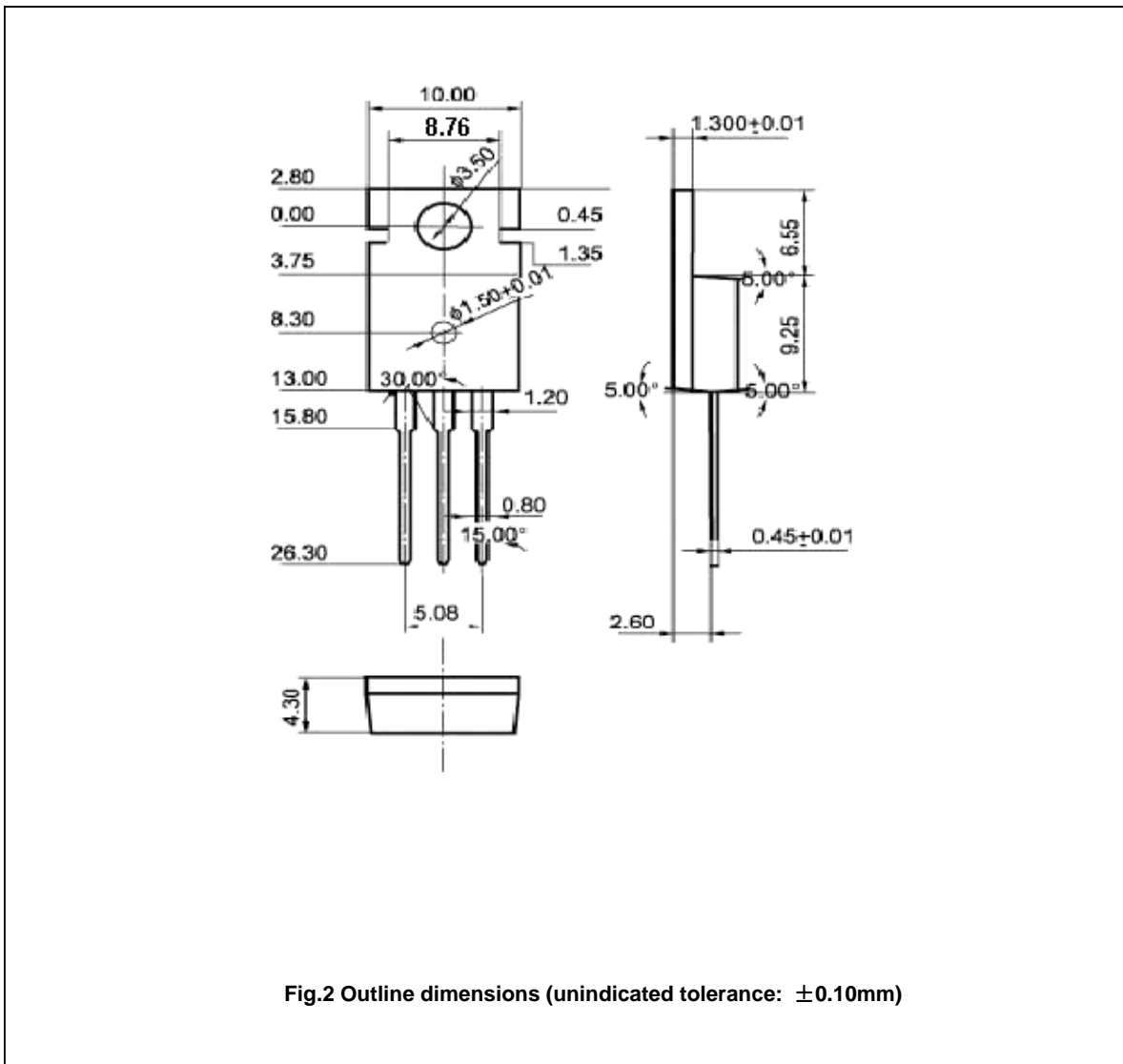


Fig.2 Outline dimensions (unindicated tolerance: $\pm 0.10\text{mm}$)